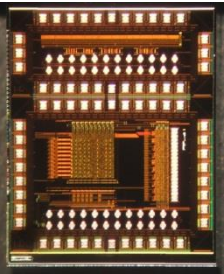# CLICPix/CCPD/Mu3e
(HVCMOS)

Ivan Peric

HV CMOS detectors

- 2005: Project proposal submitted to BW-Stiftung: "Monolithic Detector in High Voltage Technology"
- Project approved and funded with 40k€
- Two patent applications: *"Monolithic detector in high voltage technology"* and *"Hybrid pixel detector for high energy radiation made with two capacitive coupled chips"*
- First presentation of results: *Vertex 2006*
- First publication: I. Peric; *"A novel monolithic pixelated particle detector implemented in high-voltage CMOS technology," Nucl. Inst. Meth. A 582, pp. 876-885 (2007)*
- Since then 23 submitted chips
- AMS H35: 8 chips, AMS H18: 11 chips, UMC 180nm 2 chips, UMC 65nm 2 chips (OKI SOI 2 chips)
- Total cost of the chips ~ 209 k€
- >10 Publications
- ~56 Authorships
- Institutes using the chips: Bonn, CPPM, CERN, Geneva, Göttingen, Glasgow, Heidelberg, Mainz, PSI, Belgrade (planned), LBNL (Planned), RAL, Santa Cruz (planned)
- Experiments: Mu3e (basic technology), ATLAS (option), CLIC (option), Panda Luminosity Monitor
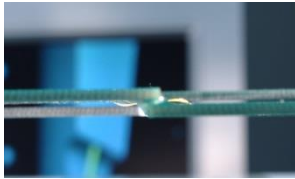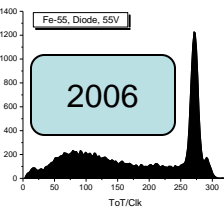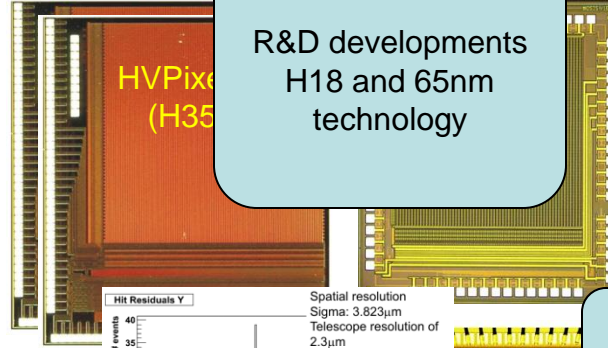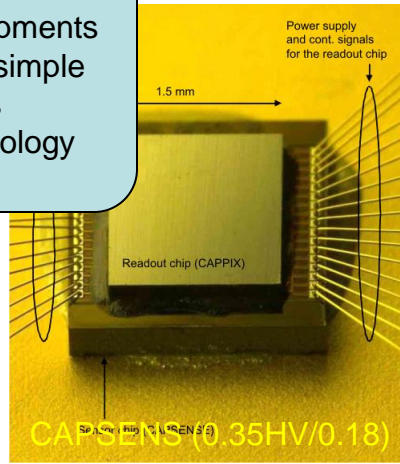
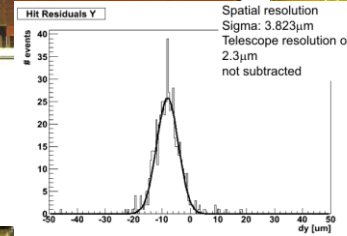# HV CMOS detectors (and 2 SOI)

R&D developments
Smart and simple pixels
H35 Technology

R&D developments
H18 and 65nm technology
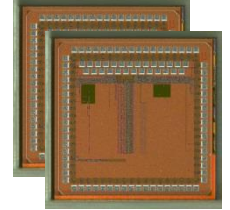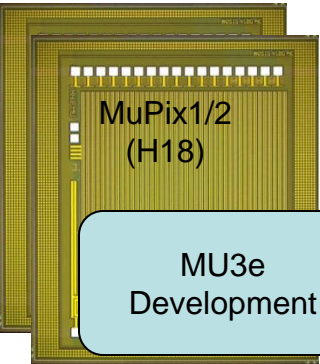
HVPixel1 (H35)

HVPixel2 (CCPD)

CAPSENS (0.35HV/0.18)

2006

SDS (65nm)

OKI SOI

OKI (300nm SOI)

Spatial resolution
Sigma: 3.823μm
Telescope resolution of 2.3μm
not subtracted

MuPix1/2 (H18)

MuPix3-6 (H18)
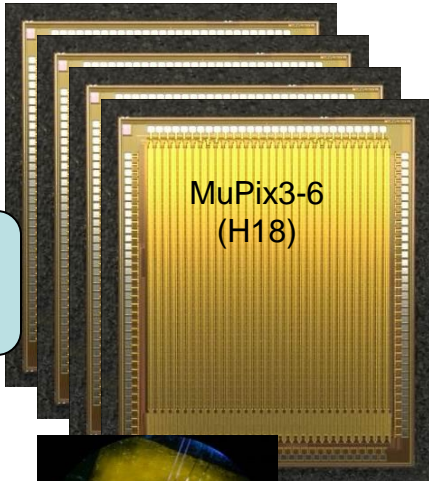
CCPD1-4 (H18)
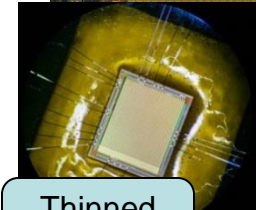
CLIICPIXS (H18)
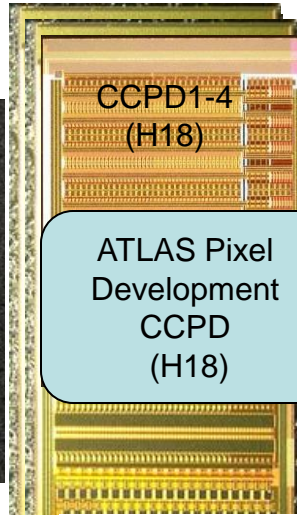
HVStrip (H35)

MU3e Development

ATLAS Pixel Development CCPD (H18)
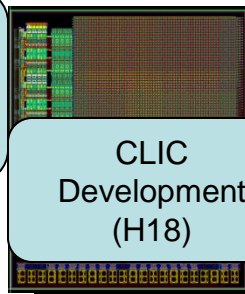
CLIC Development (H18)
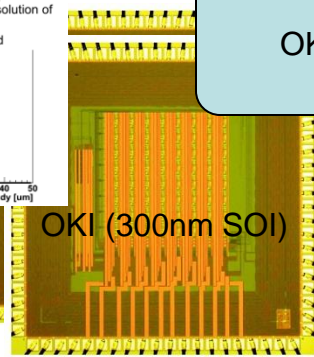
H35CCPD (H35)
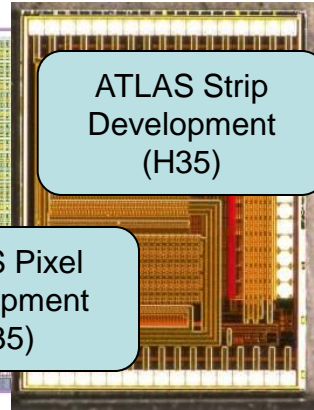
ATLAS Strip Development (H35)

ATLAS Pixel Development (H35)

99% efficiency

Thinned chips

Irradiated chip

eff. ~97%   80V
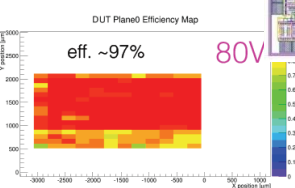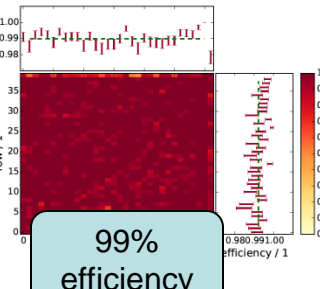
HV CMOS detectors

- 2005: State of the art CMOS sensors are based on diffusion (MAPS)
- Motivation: Develop a CMOS sensor structure that is:
- Compatible with the standard CMOS (cheap and fast prototyping/large scale production)
- Based on fast and efficient charge signal collection by drift (HV needed to deplete sensor)
- Radiation tolerant
- With high time resolution
- Suitable for particle physics at LHC

- HVCMOS detector structure
- PMOS and NMOS transistors are placed inside their shallow wells (fully CMOS possible!!!)

PMOS NMOS

Shallow n-well

Shallow p-well
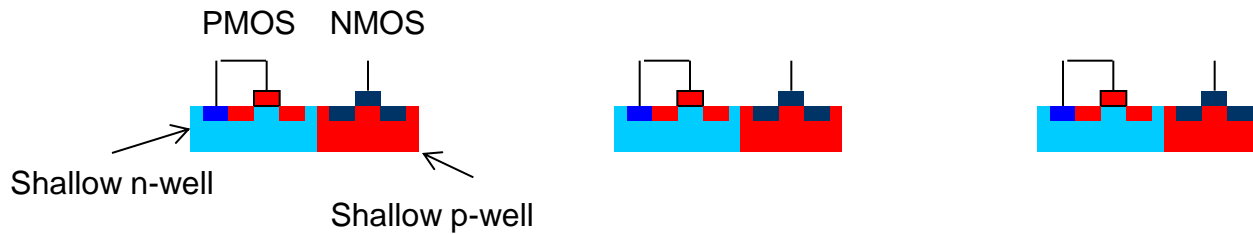
- A deep n-well surrounds the electronics of every pixel

PMOS   NMOS

deep n-well

- The deep n-wells isolate the pixel electronics from the p-type substrate

PMOS NMOS

deep n-well
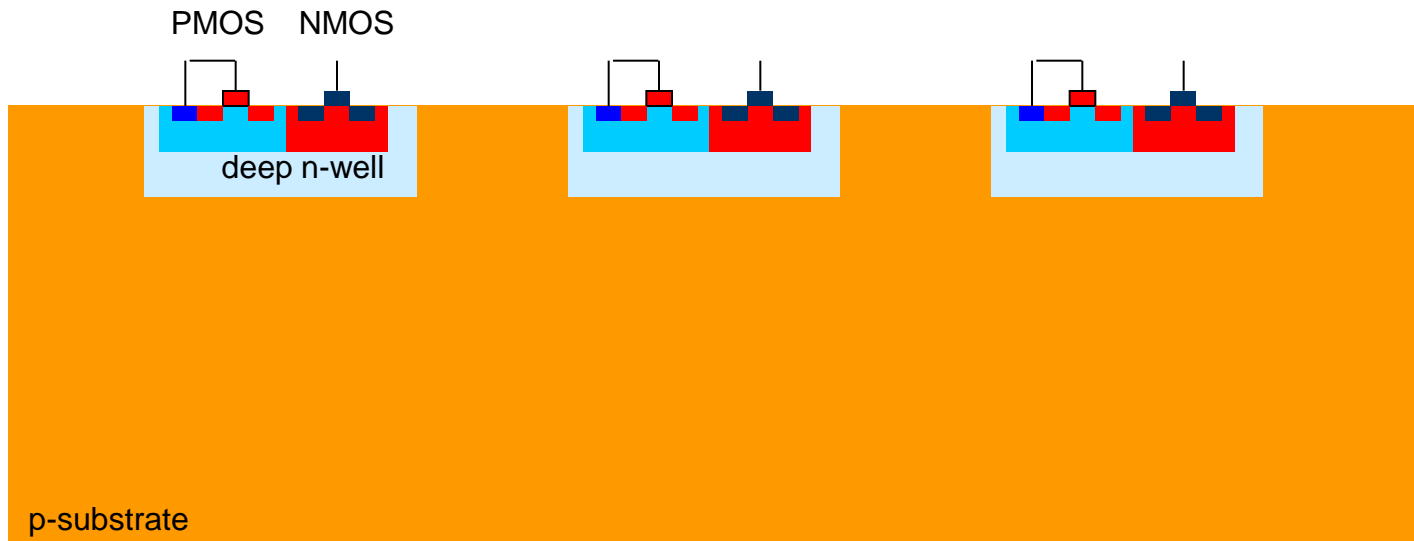
p-substrate

- The substrate can be biased low without damaging the transistors
- In this way the depletion zones in the volume around the n-wells are formed
- => Potential minima for electrons
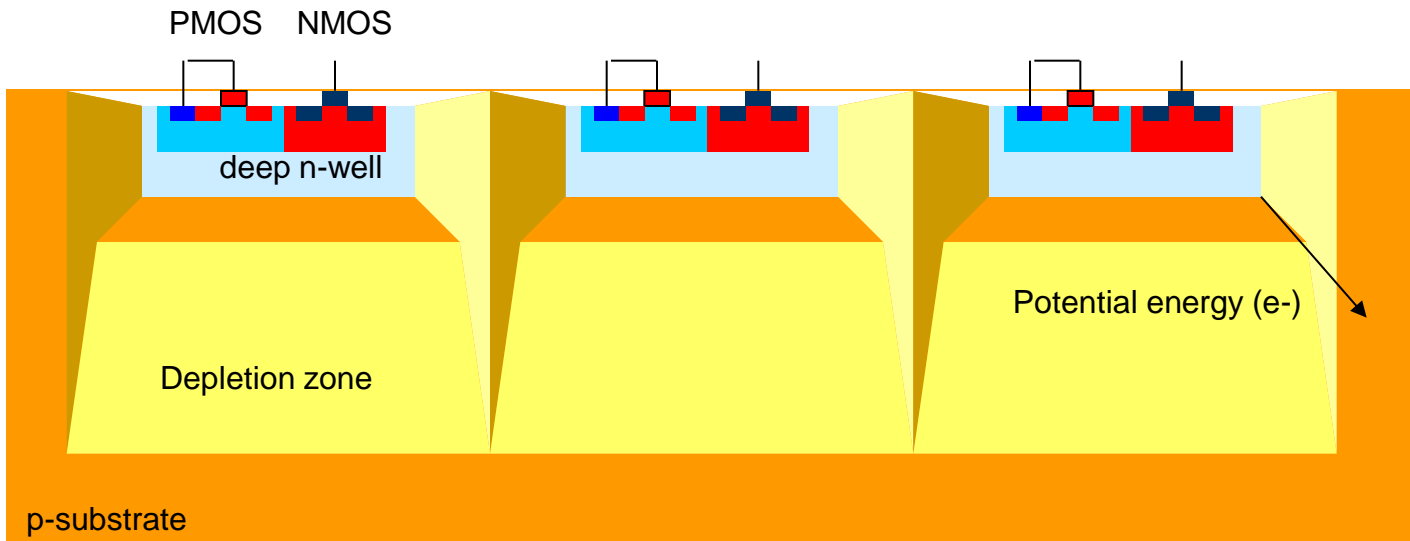
PMOS   NMOS

deep n-well

Potential energy (e-)

Depletion zone

p-substrate

- Charge collection occurs by drift. (main part of the signal)

PMOS   NMOS

deep n-well

Drift

Potential energy (e-)

Depletion zone

p-substrate
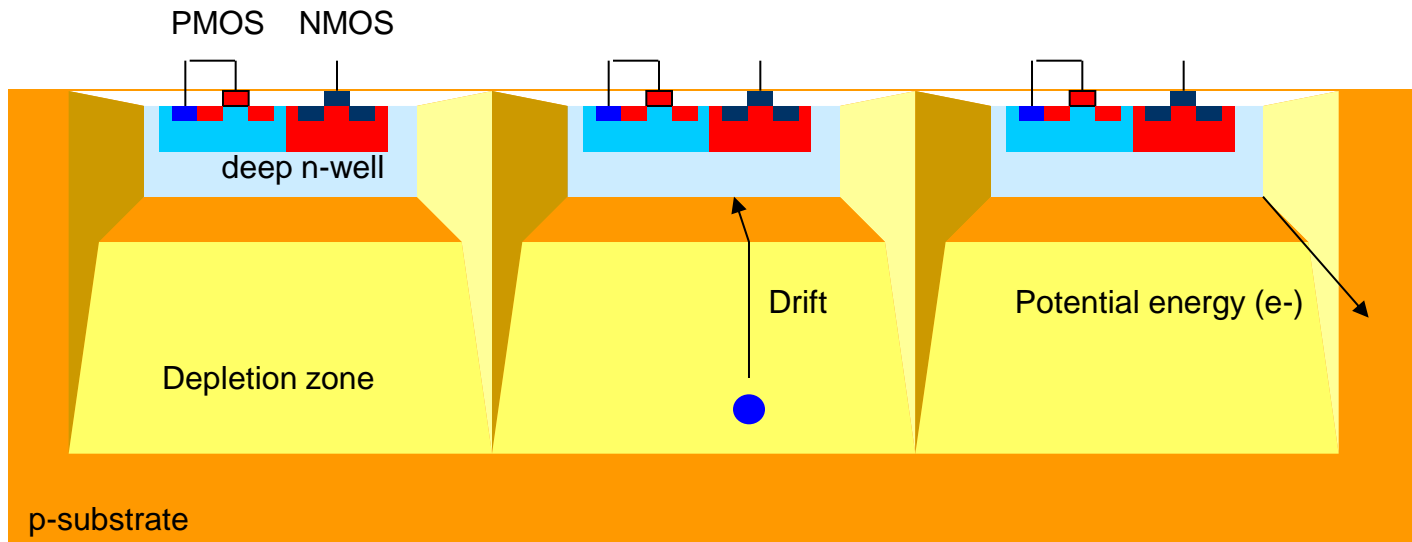
- Charge collection occurs by drift. (main part of the signal)
- *Additional charge collection by diffusion*

PMOS   NMOS

deep n-well

Drift

Potential energy (e-)

Depletion zone

p-substrate

Diffusion
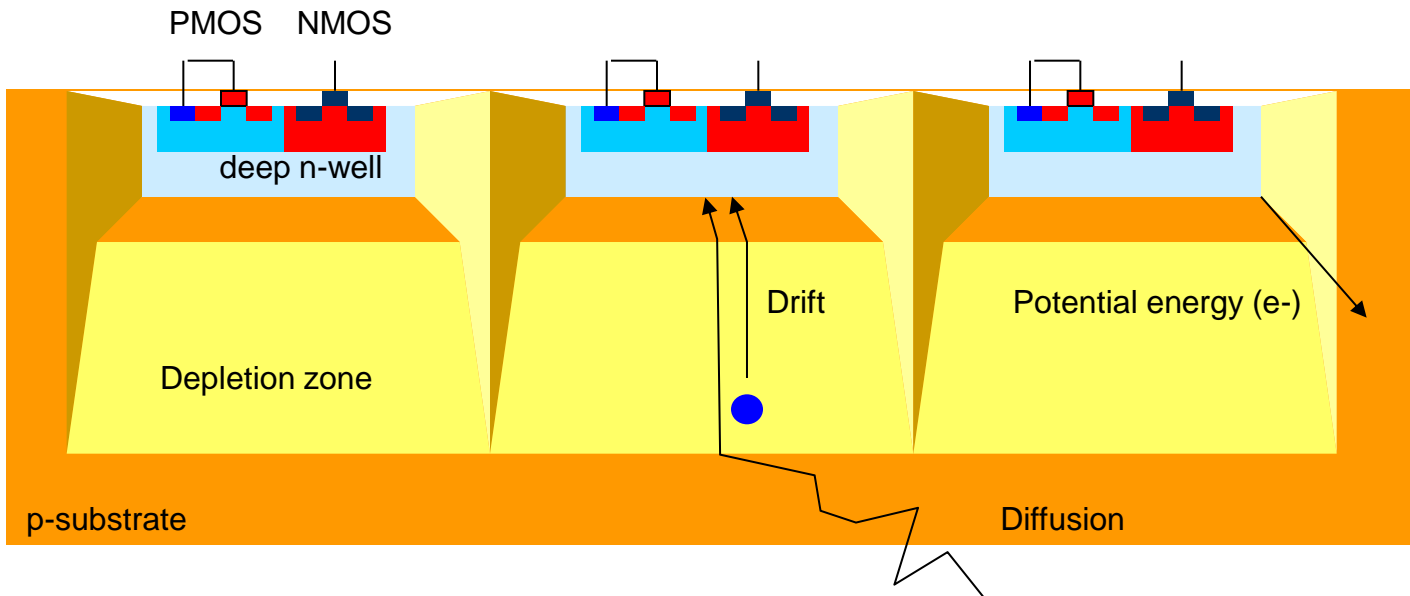
HV CMOS detectors

- The deep n-wells are biased using high ohmic devices
- Charge collection leads to a voltage signal that can be amplified
- The use of charge sensitive amplifiers improves signal to noise ratio

deep n-well

Drift

Potential energy (e-)

Depletion zone

p-substrate

Diffusion
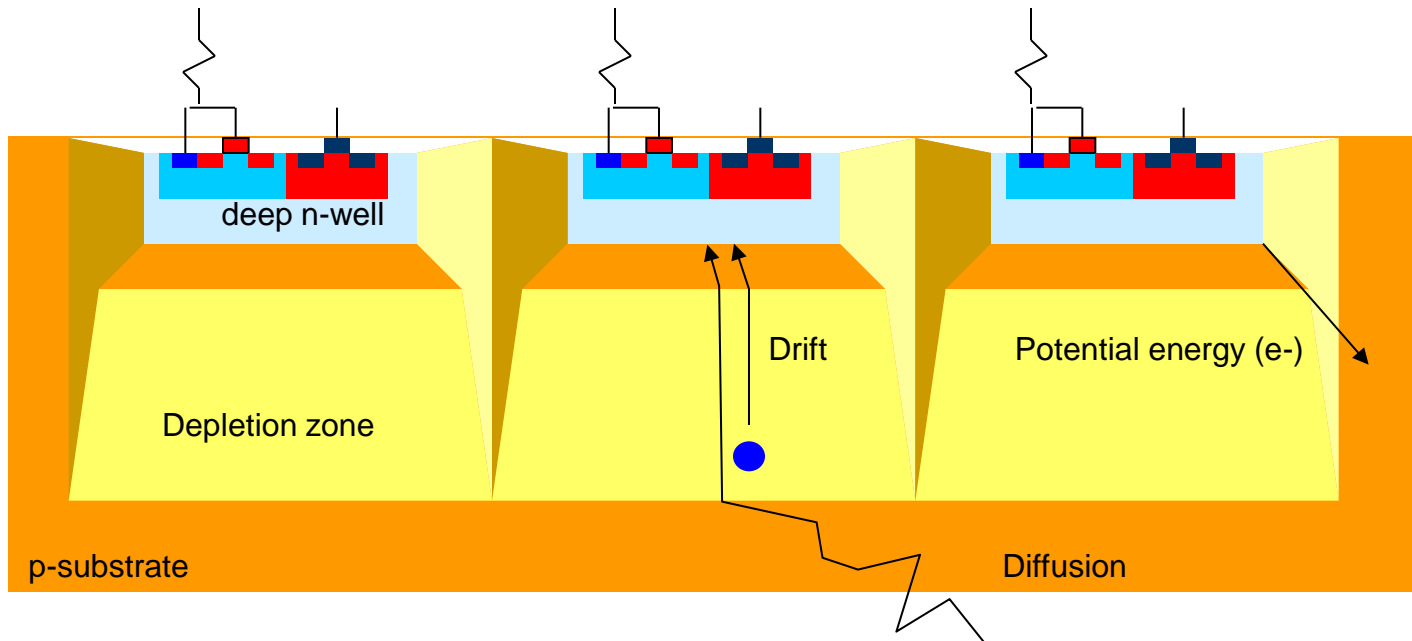
- HVCMOS sensors can be implemented in *any CMOS technology* that has a deep-n-well surrounding low voltage p-wells

deep n-well

Potential energy (e-)

Depletion zone

p-substrate

- CMOS pixel flavors (five years ago)

Standard MAPS
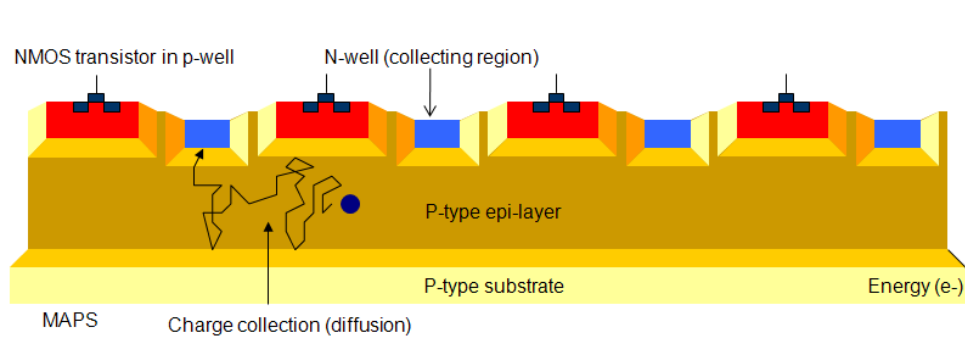
INMAPS
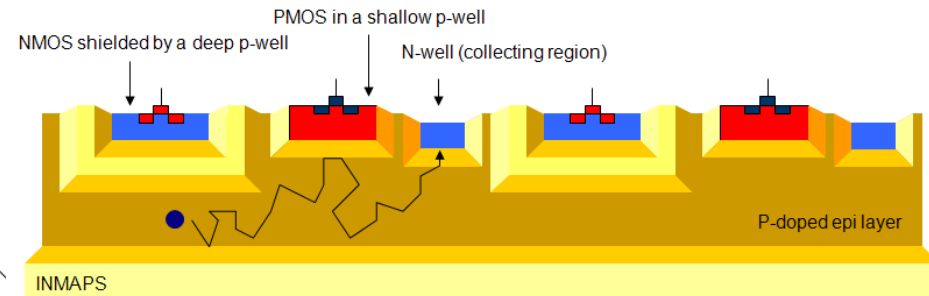
HVCMOS
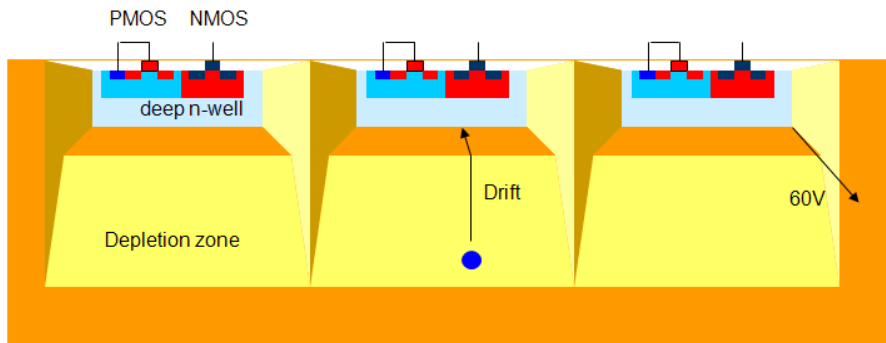
TWELL MAPS

High-voltage monolithic detectors

0V

<-60V

drift

Tcoll < 1ns

diffusion

MAPS (as comparison)

High-voltage monolithic detectors

drift
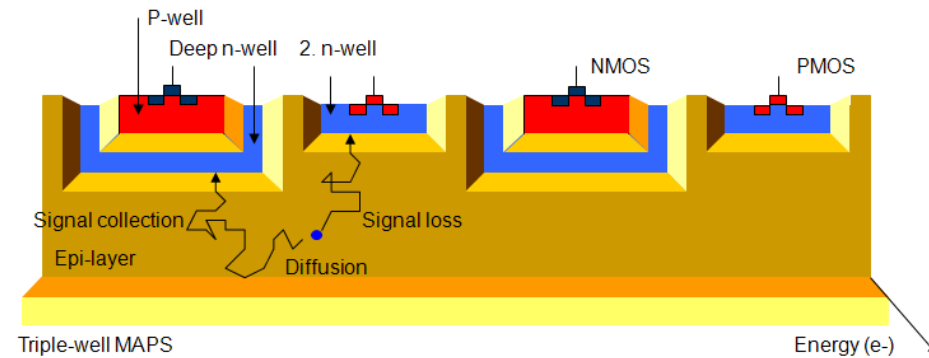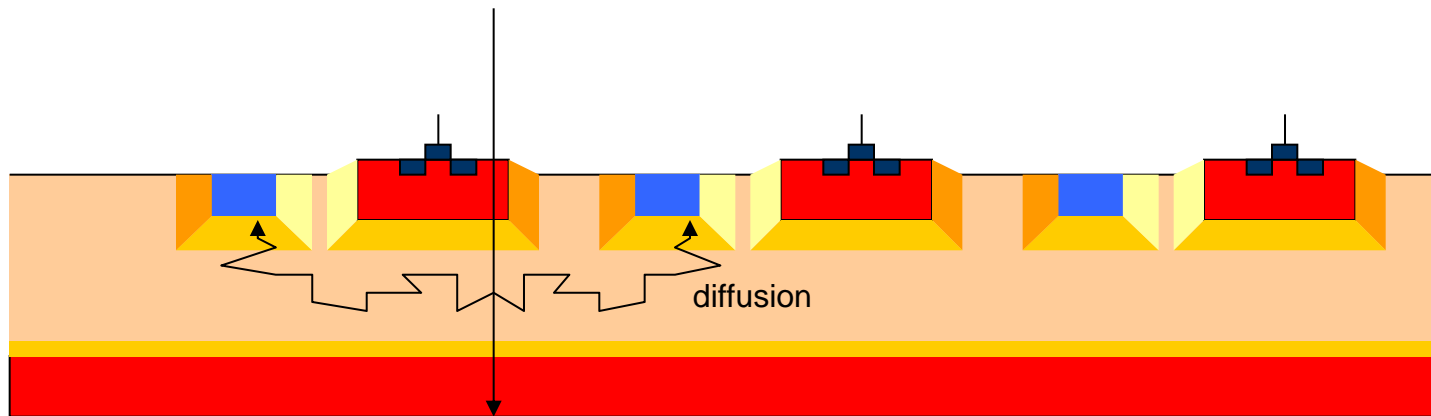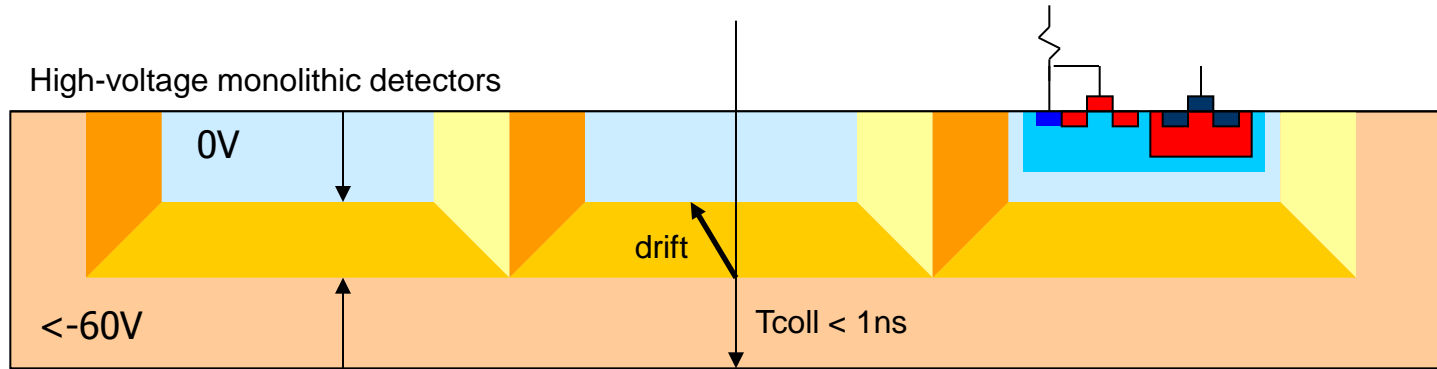
Rad. damage

MAPS (as comparison)

Rad. damage
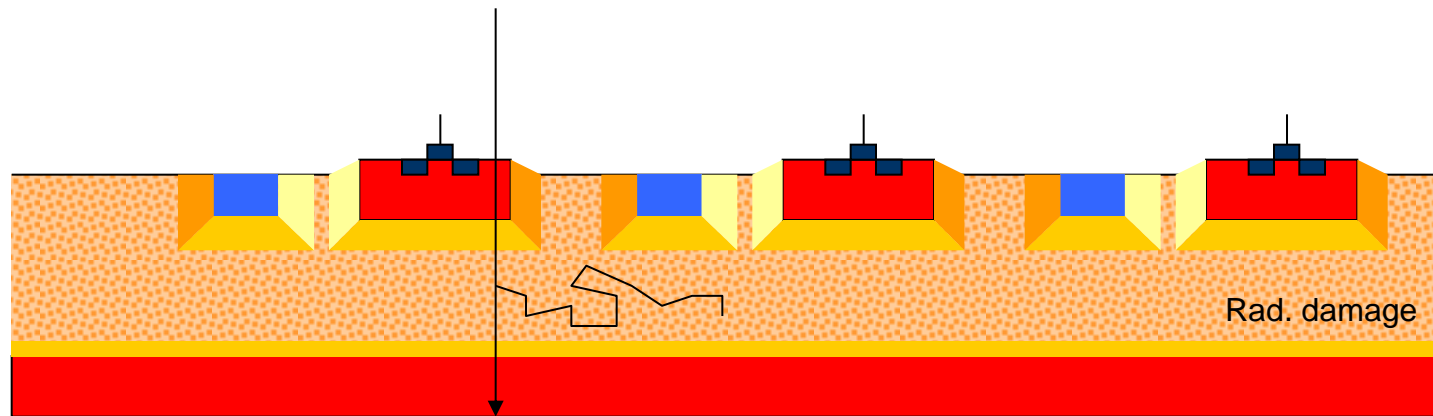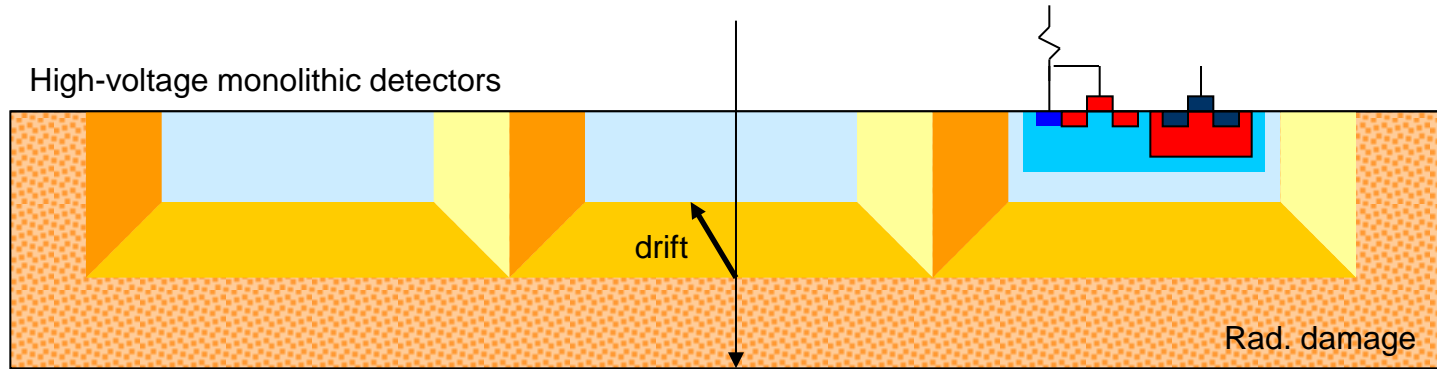
CMOS pixel flavors

- CMOS pixel flavors (now)

NMOS shielded by a deep p-well

PMOS in a shallow p-well

N-well (collecting region)

HRCMOS

HVCMOS

PMOS   NMOS

deep n-well

Drift

60V

Depletion zone

Ivan Peric: CPIX14, Bonn, 2014

16

Pixel

Readout chip

Active CMOS sensor

Signal charge

Ivan Peric: CPIX14, Bonn, 2014
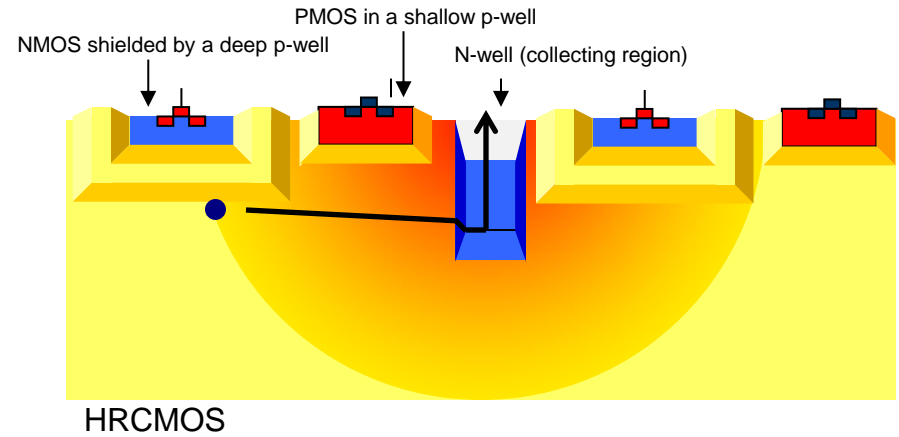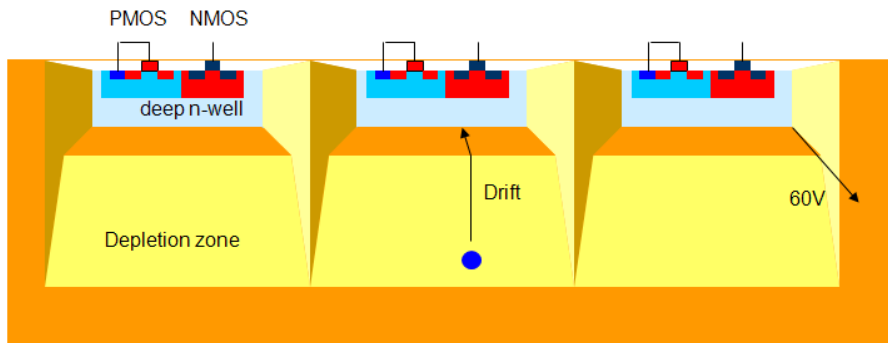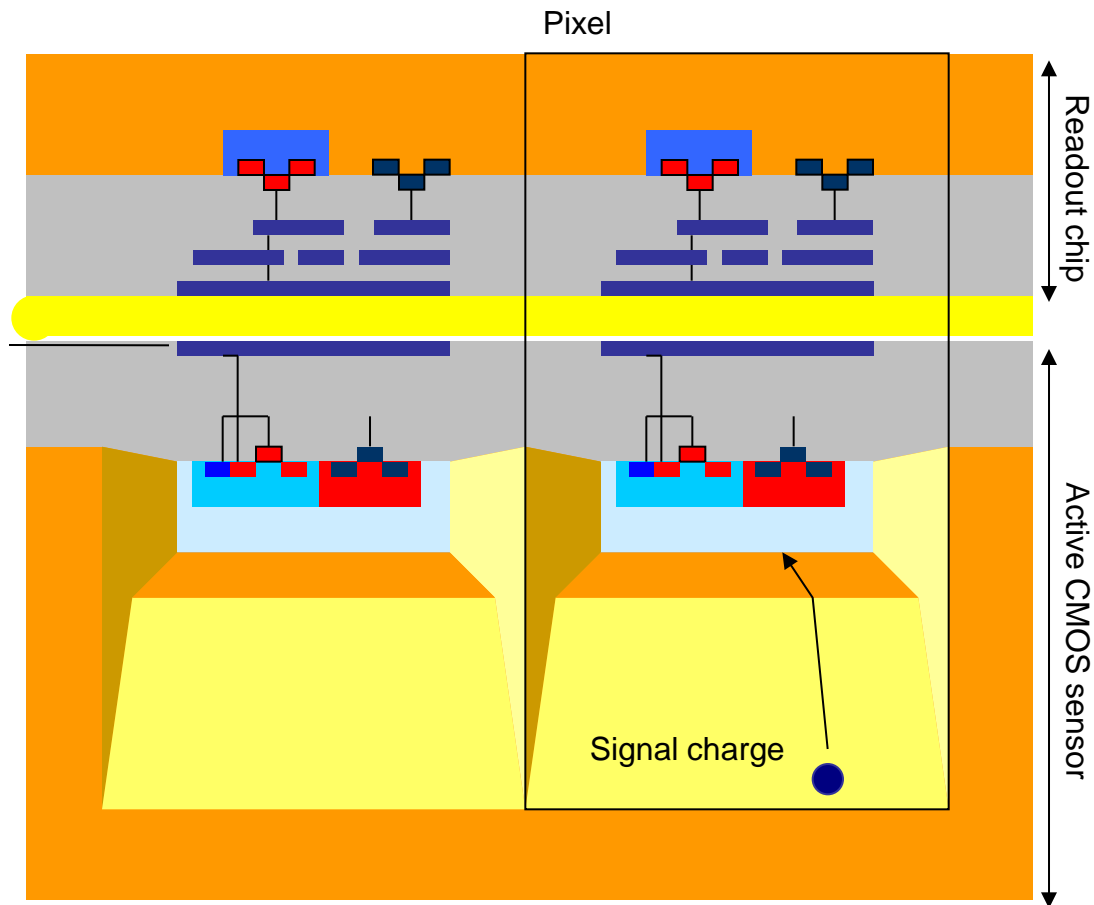
-HVCMOS proof of principle
-First SNR measurements
-Smart pixels (ZS)

HVPixel1 (H35)

2006
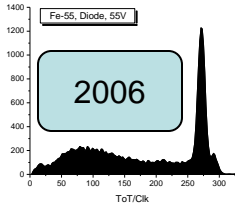
-CCPD demonstration
-Smart pixels with analog trigger delay
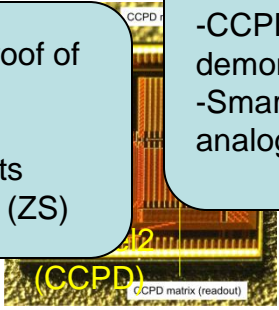
-Edgeless CCPD demonstration
-Smart pixels with analog trigger delay
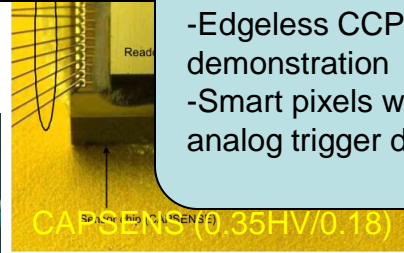
Rolling shutter HVCMOS with 4T pixels

Rolling shutter HVCMOS with in-pixel CDS

Rolling shutter with 2.5µm pixels

Hpixel (H18)

SDS (65nm)

High dynamic range sensor for FEL

OKI (300nm SOI)
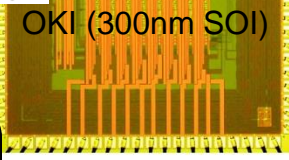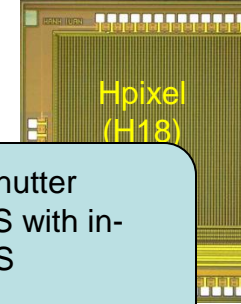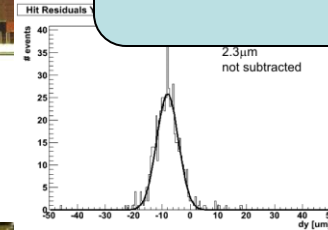
MuPix1/2 (H18)

MU3e detector concept demonstration

MU3e prototypes with ZS and digital time measurement

CCPD1-4 (H18)

CCPD readout by FEI4

CCPD readout by CLICPIX 25x25um pixels

CCPD in H35

HVStrip (H35)

H35CCPD (H35)

Strip readout with modified ABCN chip

99% efficiency

Thinned chips

Irradiated chip

eff. ~97%   80V

18

Ivan Peric, CPix14, Bonn, 2014
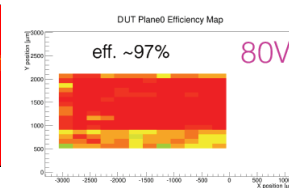
Ideal Detector for LHC

Fully depleted sensor

- State of the art: Fully depleted hybrid pixel detectors (or strip detectors) based on a passive sensor on high quality substrate
- Fully depleted detectors work good but have some drawbacks
- Drawbacks – high price, scientific: small pixels not possible, thickness
- If we propose a new technology, it must be better for science

ROC

Need for readout chips separated from the sensor

Low pitch bump bonding required
Wafers are required - expensive
Difficult prototyping
Bump bond pitch reduces the spatial resolution

~500um

High capacitance

Fully depleted sensor
Based on expensive high quality substrate
Small wafer size

250um

Thinner would be better

Backside processing

2 kOhm cm

HV 250V

HVCMOS sensor

- HVCMOS for LHC: possibly smaller pixels and thinner
- Ideal pixel size ~ 25µm
- Ideal thickness = ?

ROC

HV~100V

25um

25um

Reduced pixel size for better experimental performance Better spatial resolution, recognition of near tracks (jets)

50um

20 Ohm cm

One side processing only (cheaper, faster prototyping)

Thin sensor – little deflecting of particles

- Ideal thickness = ?
- If depleted layer thickness > pixel size reduces spatial resolution, adds redundant information
- Ideal thickness ~ 25-50µm

HV~100V

25um

Lower capacitance

100um

Ionization along the track

- Ideal thickness ~ 25-50μm
- Drawback: reduced signal

ROC

HV~100V

25um

25um

50um

Thin depleted layer
Reduced signal
Idea: compensate smaller
signal with smaller detector
capacitance

20 Ohm cm

- Idea: compensate smaller signal with smaller detector capacitance
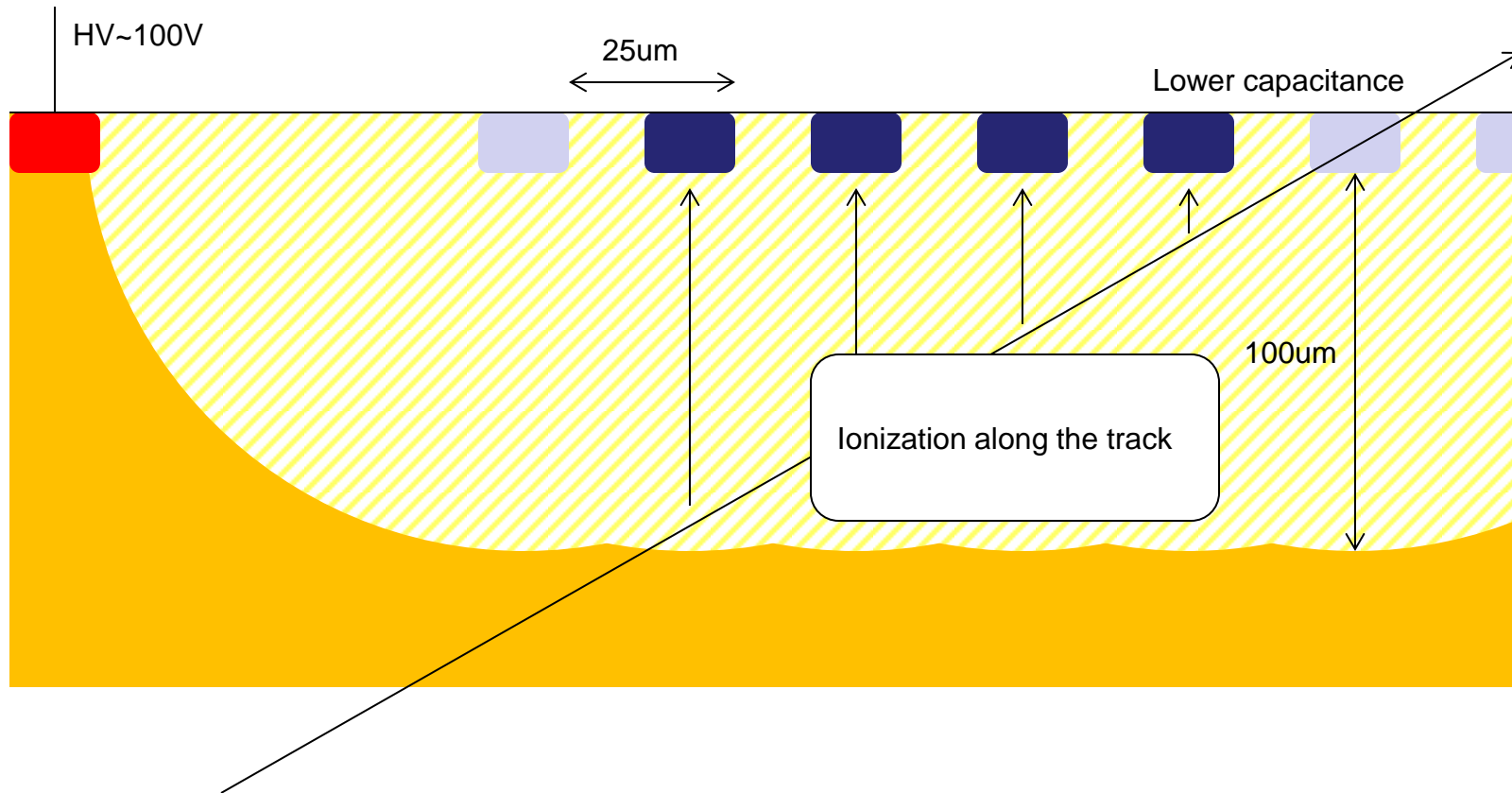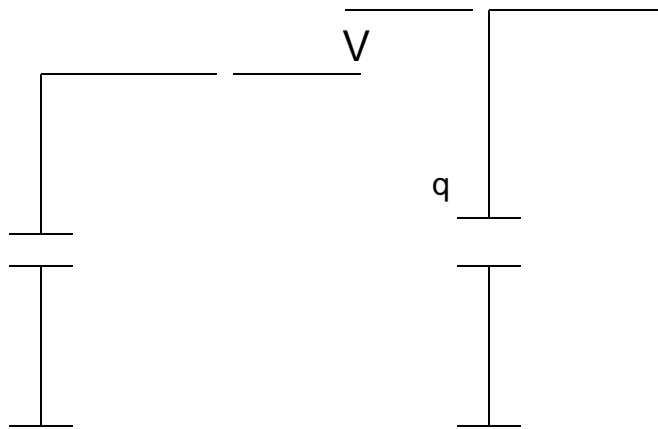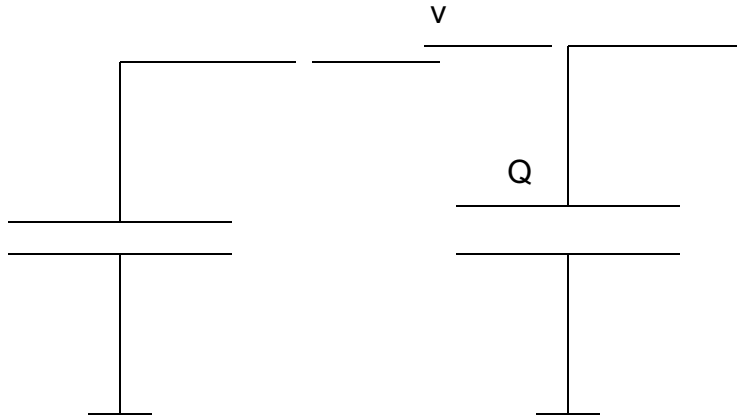
HVCMOS sensor

- Ideal thickness ~ 25-50μm
- Reduced signal
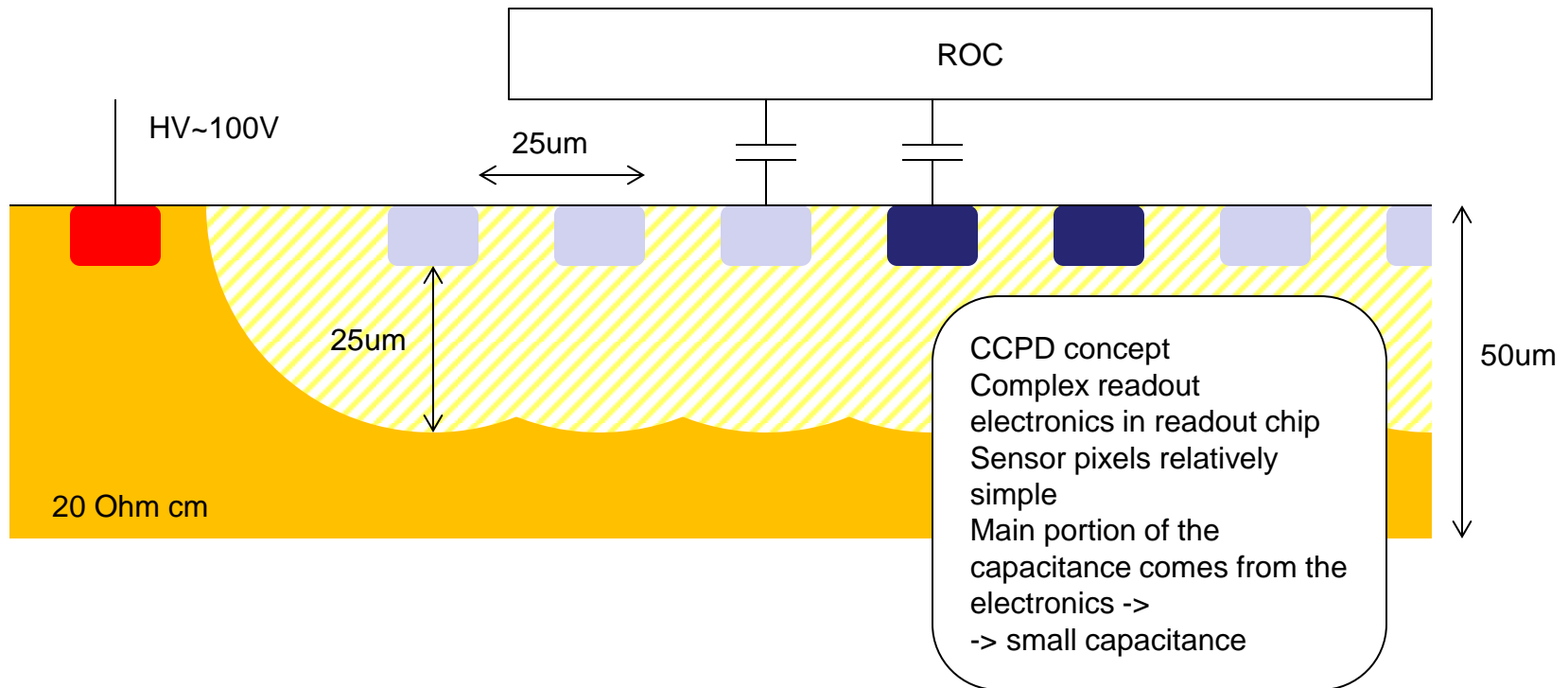
ROC

HV~100V

25um

25um

50um

20 Ohm cm

CCPD concept
Complex readout electronics in readout chip
Sensor pixels relatively simple
Main portion of the capacitance comes from the electronics ->
-> small capacitance

Optimal substrate resistivity

- In order to achieve a high radiation tolerance, we would prefer highest possible electric field
- High drift speed -> small probability for charge trapping
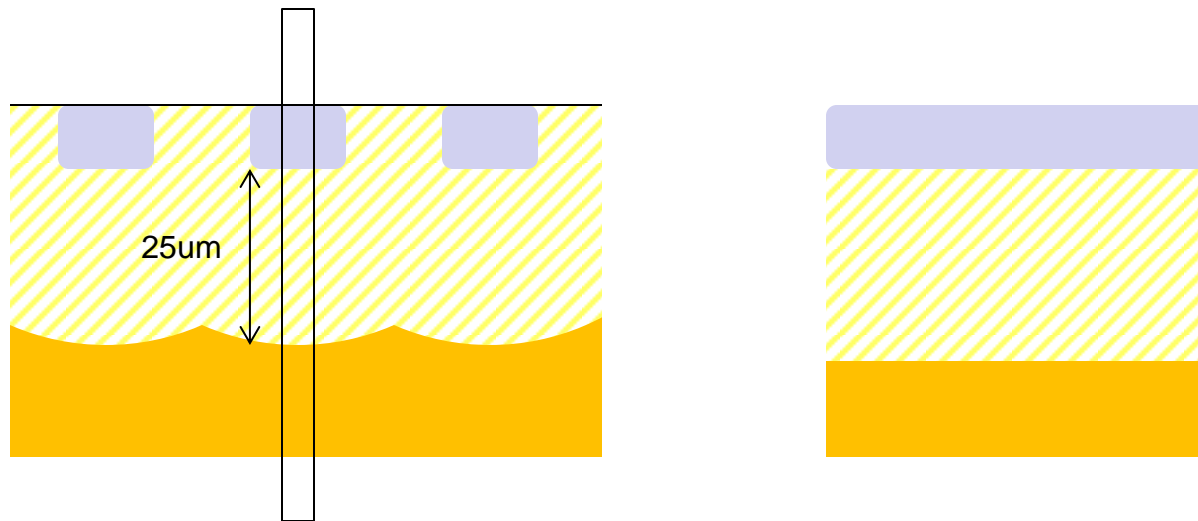
- In order to achieve a high radiation tolerance, we would prefer highest possible electric field
- High E-field -> high drift speed -> small probability for charge trapping

$$V = \frac{eN_a}{\varepsilon} \frac{x^2}{2}$$

$$divE = \rho / \varepsilon \qquad \frac{dE}{dx} = eN_a / \varepsilon \qquad E = \frac{eN_a}{\varepsilon} x$$
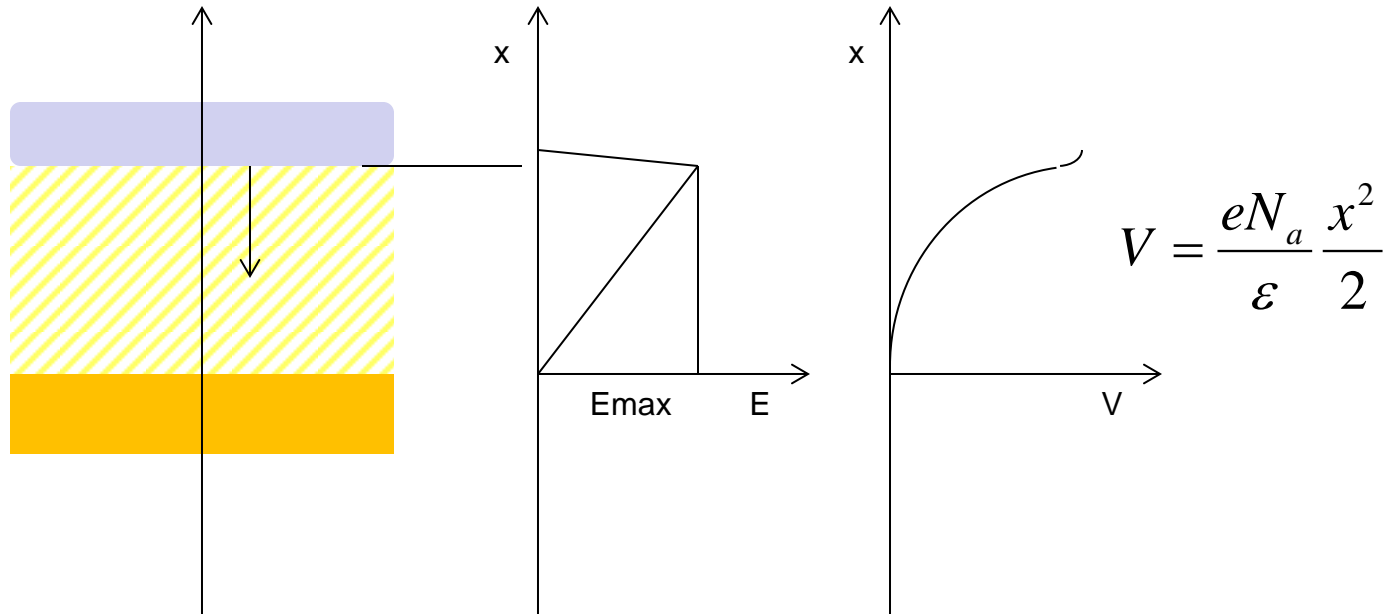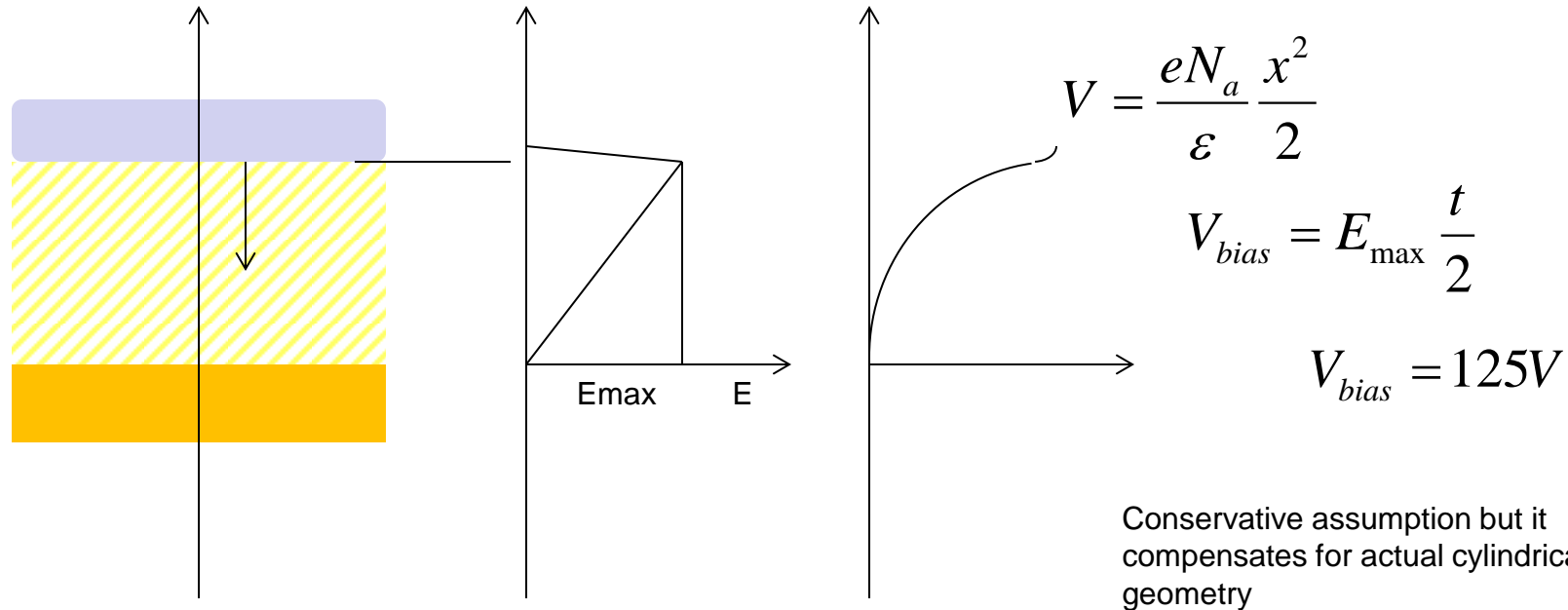
- In order to achieve a high radiation tolerance, we would prefer highest possible electric field
- High E-field -> high drift speed -> small probability for charge trapping
- Let us assume Emax ~ 10 V/μm (Conservative assumption but it compensates for actual cylindrical geometry)

$$V = \frac{eN_a}{\varepsilon} \frac{x^2}{2}$$

$$V_{bias} = E_{max} \frac{t}{2}$$

$$V_{bias} = 125V$$

Emax   E

Conservative assumption but it compensates for actual cylindrical geometry
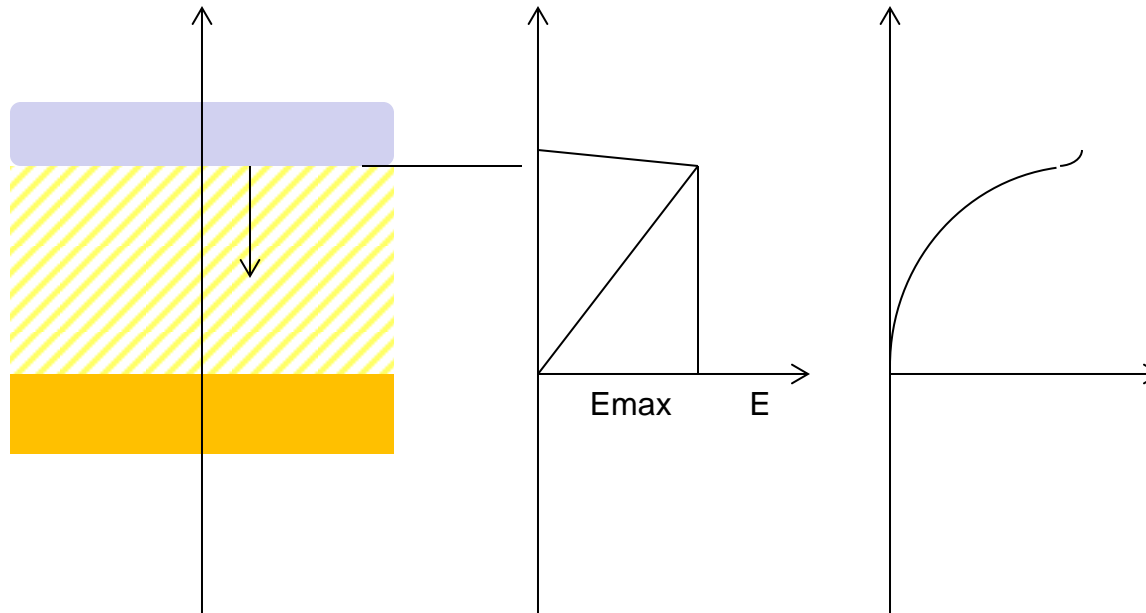
$$E = \frac{eN_a}{\varepsilon} x \qquad E_{max} = \frac{eN_a}{\varepsilon} t \qquad N_a = \frac{E_{max}\varepsilon}{et} \qquad E_{max} \approx 10V/\mu m$$

$$N_a = \frac{10V}{1\mu m} \frac{11 \cdot 8.854 \cdot 10^{-12} F/m}{1.602 \cdot 10^{-19} C \cdot 25\mu m} = 24 \cdot 10^{19} m^{-3} = 2.4 \cdot 10^{14} cm^{-3}$$

- In order to achieve a high radiation tolerance, we would prefer highest possible electric field
- High E-field -> high drift speed -> small probability for charge trapping
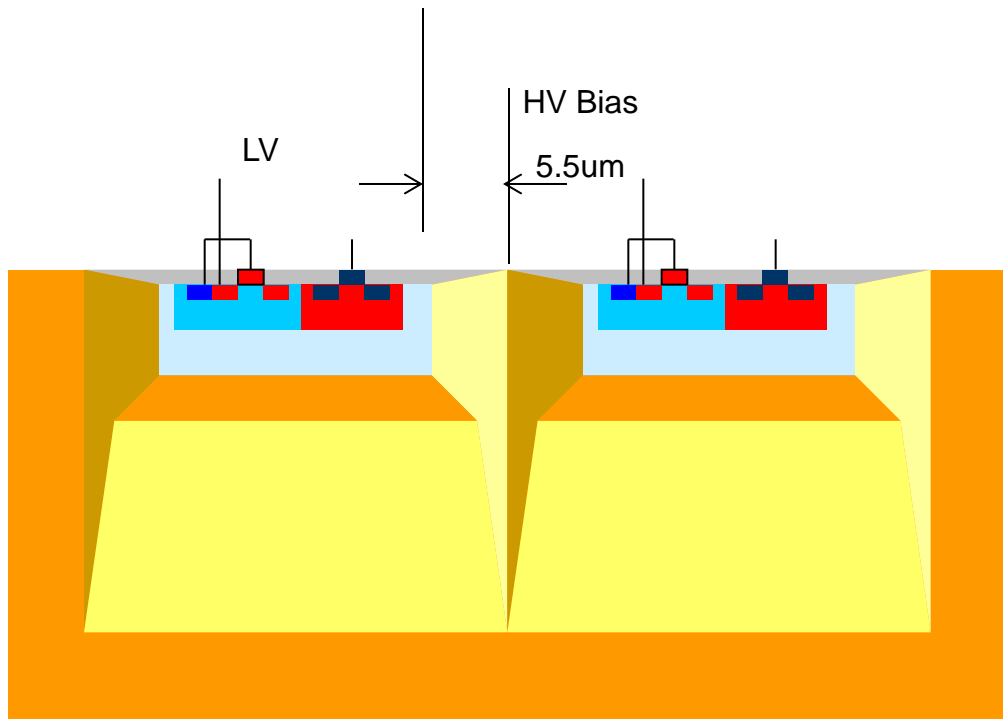- Let us assume Emax ~ 10 V/μm
- Optimal substrate resistivity ~ 55 Ωcm

$$V_{bias} = 125V$$

$$N_a = 2.4 \cdot 10^{14} cm^{-3} \Rightarrow R = 55\Omega cm$$

- Edge effects or cylindrical/radial geometry can reduce the maximal voltage
- Problem: biasing of guard rings
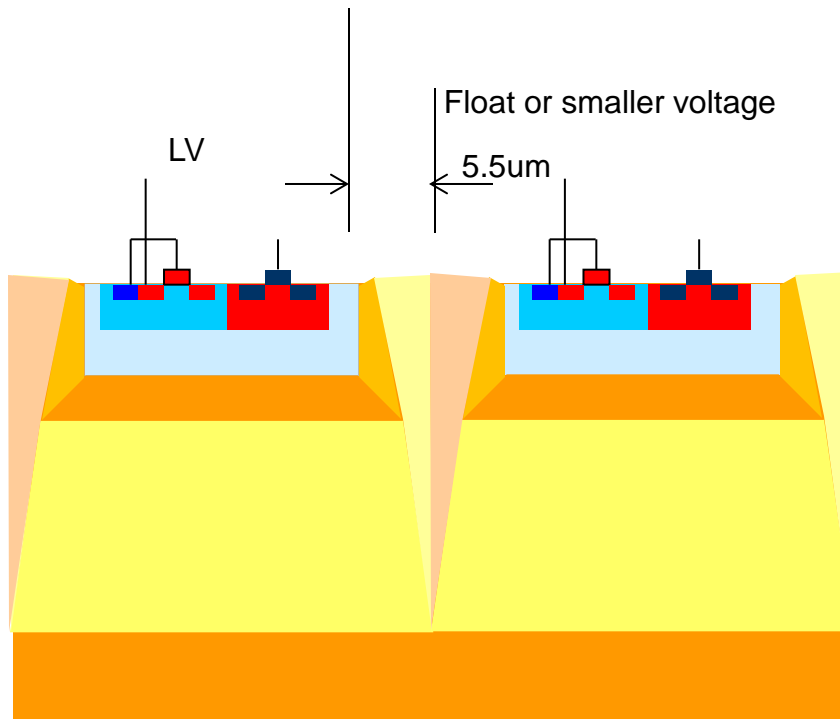
- Edge effects or cylindrical/radial geometry can reduce the maximal voltage
- Problem: biasing of guard rings – can be left floating to relax field – TCAD simulations should be done

LV

Float or smaller voltage

5.5um

HRCMOS sensor

- HRCMOS structure: voltage difference at the surface
- HVCMOS structure: voltage difference in vertical direction, less at the surface

XXum

PMOS in a shallow p-well

NMOS shielded by a deep p-well

N-well (collecting region)
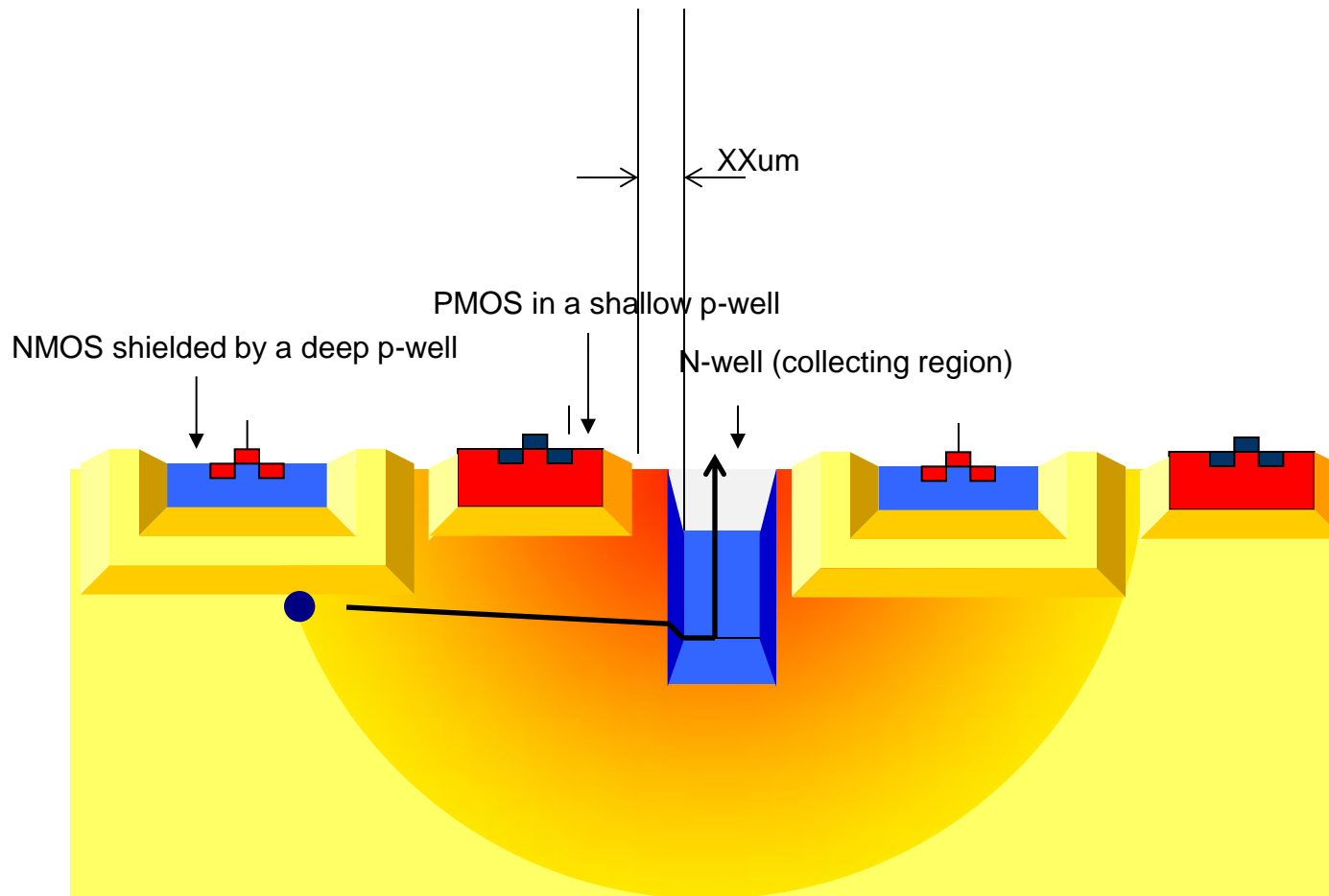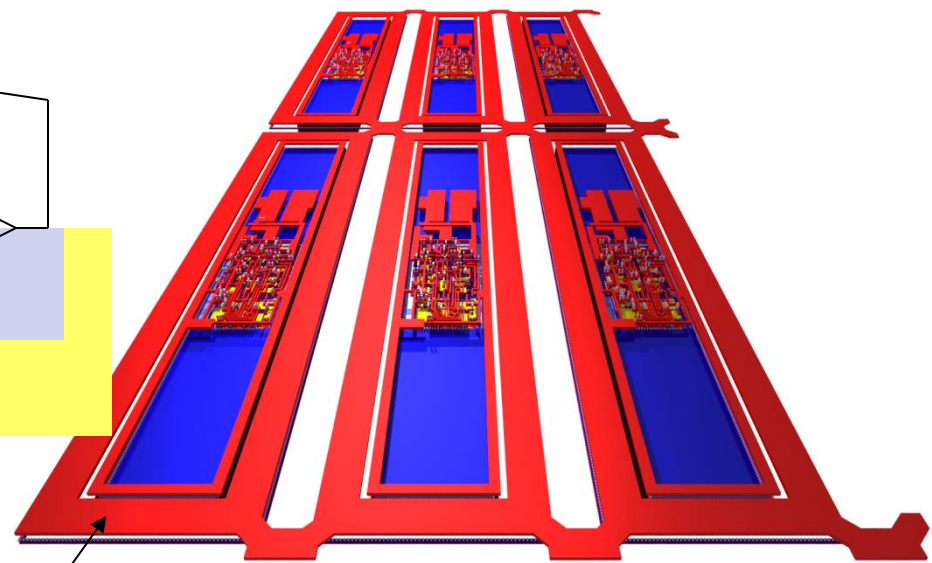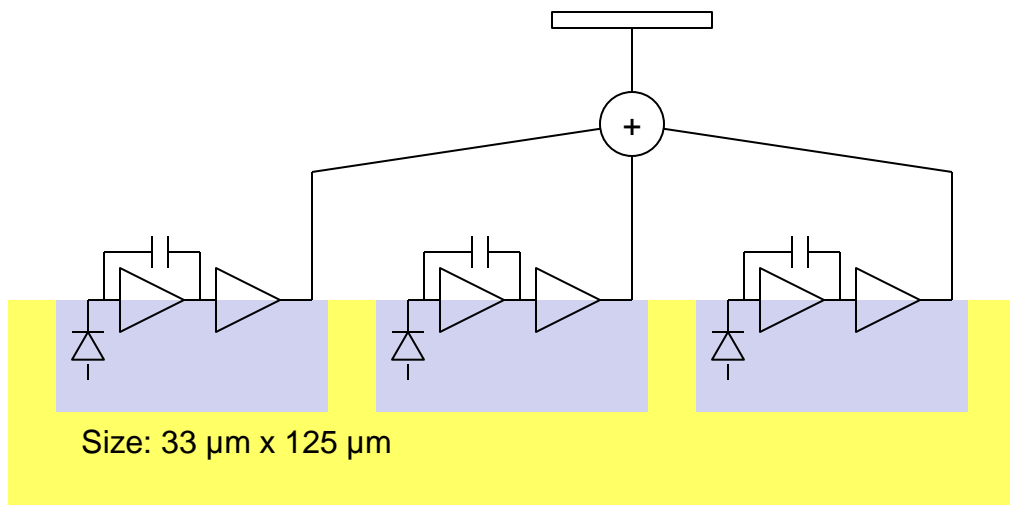
Results

ATLAS Pixels

Ivan Peric: CPIX14, Bonn, 2014

- CCPD
- Digital outputs of three pixels are multiplexed to one pixel readout cell
- HVCMOS pixel contains an amplifier and a comparator

Size: 50 μm x 250 μm

Readout pixel

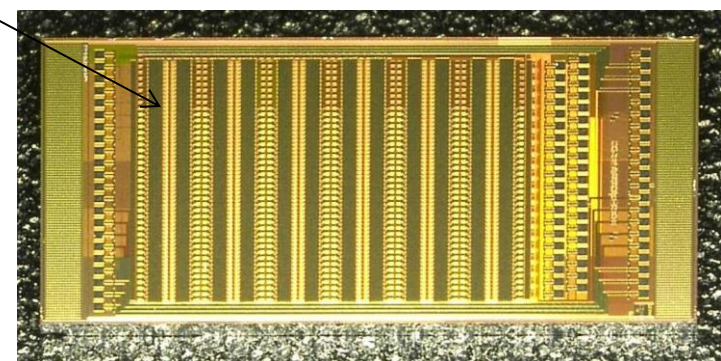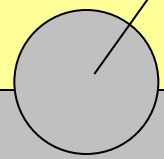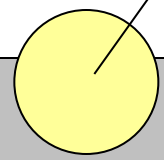TOT = sub pixel address

Different logic 1 levels

Size: 33 μm x 125 μm
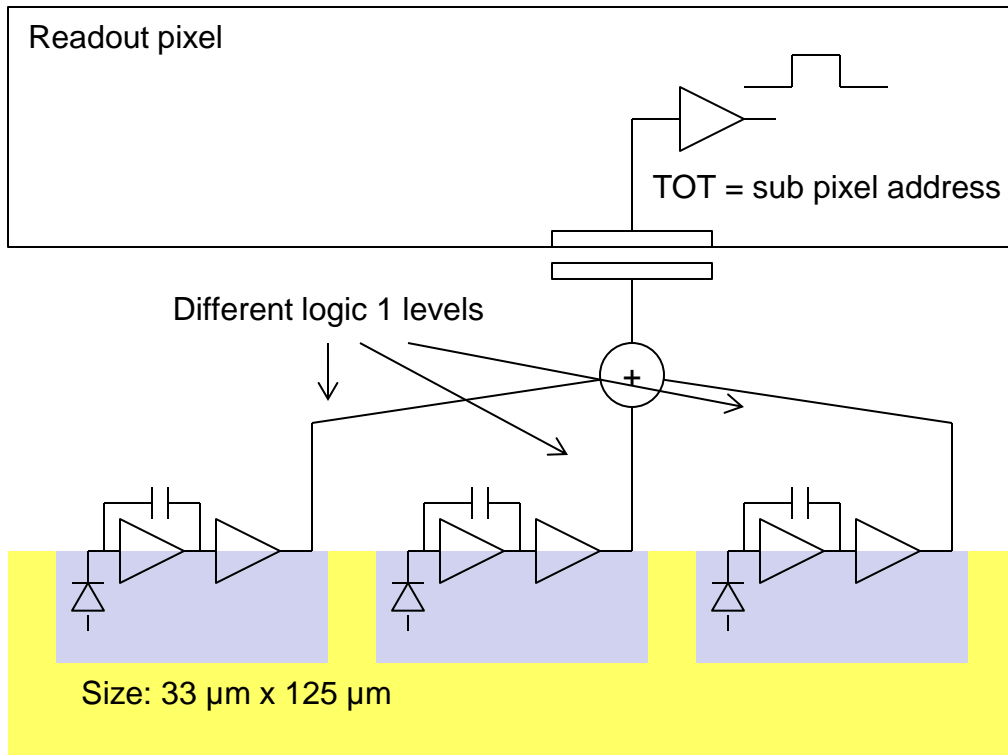
- The digital outputs of three pixels are multiplexed to one pixel readout cell

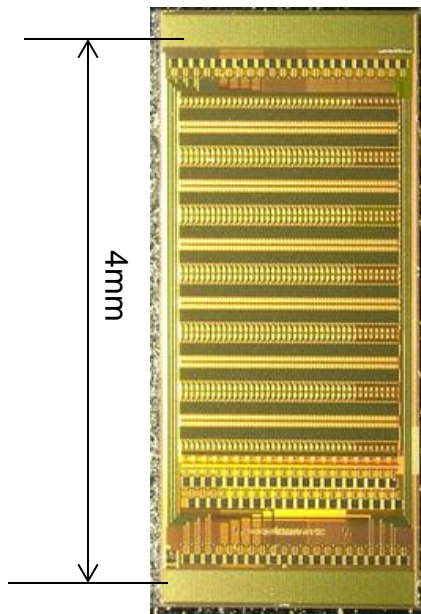Size: 33 µm x 125 µm

CCPD Pixels

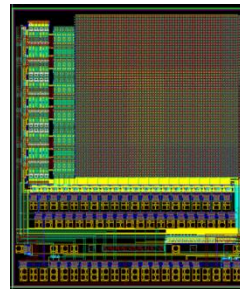| 2	2
3	3
1	1

November 2011: CCPDv1
November 2012: CCPDv2
November 2013: CCPv3/CLICPIX
June 2014: CCPv4

4mm
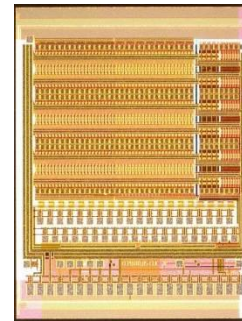
CCPDv1   CCPDv2   CCPDv3   CCPDv4

1) CCPDv1: SNR after neutron irradiation at Jozef Stefan Institute 10^{15} n_{eq}/cm^2 ~20 (5C, -55V bias)
   (Signal ~ 1180e) (measured 2014) (Unirradiated chip @ -50V bias: 1600e)
2) CCPDv2: works after 862 Mrad (x-ray irradiation CERN) (noise at room temperature 150e)
3) CCPDv1: sub pixel encoding works measured for one pixel – still needs optimization

1)

Legend: Histogram of ^{90}Sr signals / Histogram of the base line noise

2)

3)
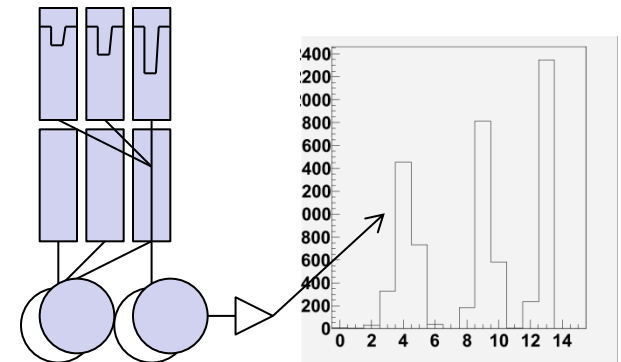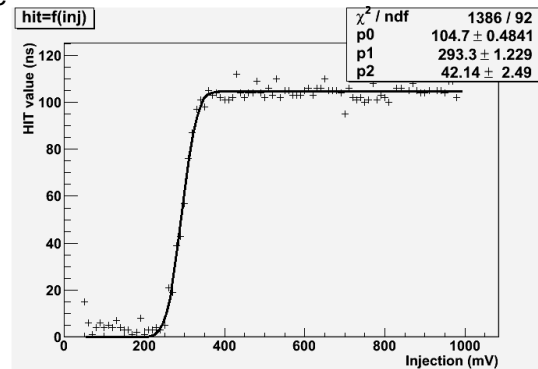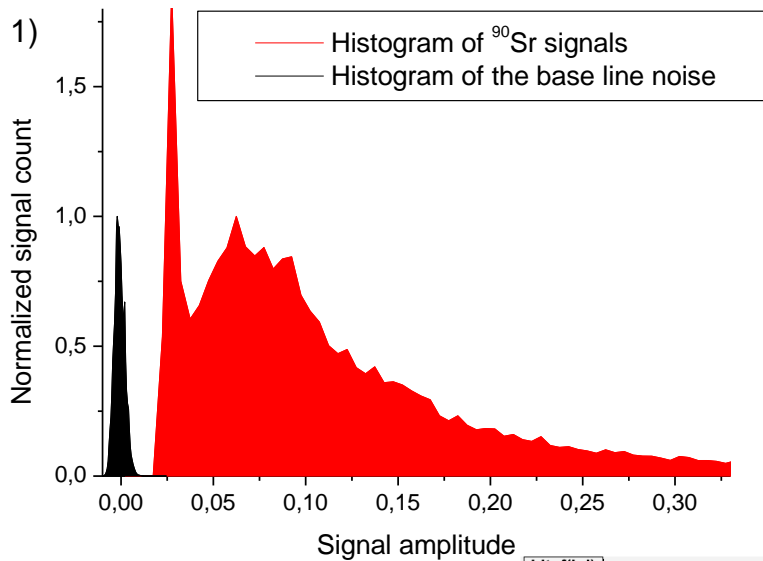
CCPDv2 and v1: test beam measurements in 2013(DESY) and 2014 (PS): efficiency 97%
Sub pixel coding not used
Timing still not as needed

PS Testbeam

DESY Testbeam
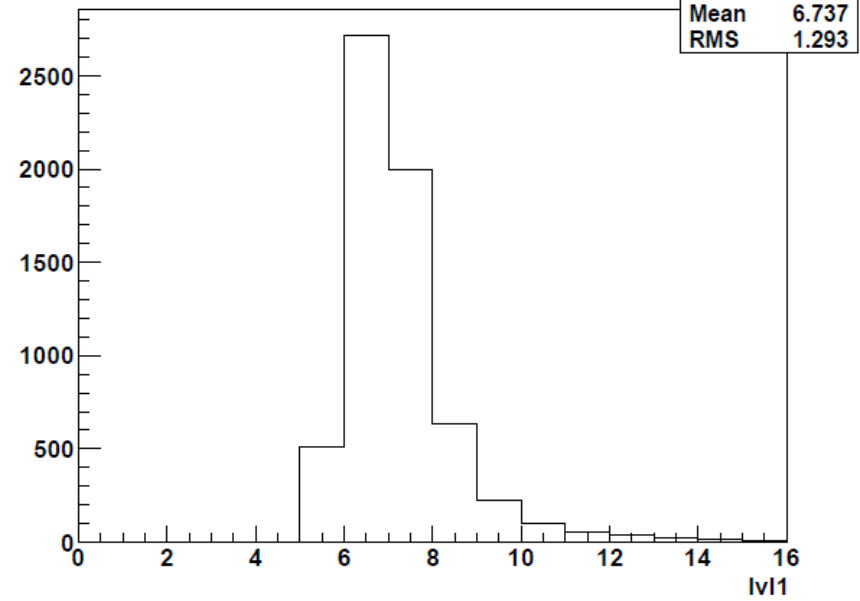
Edge TCT measurements (University of Geneve)
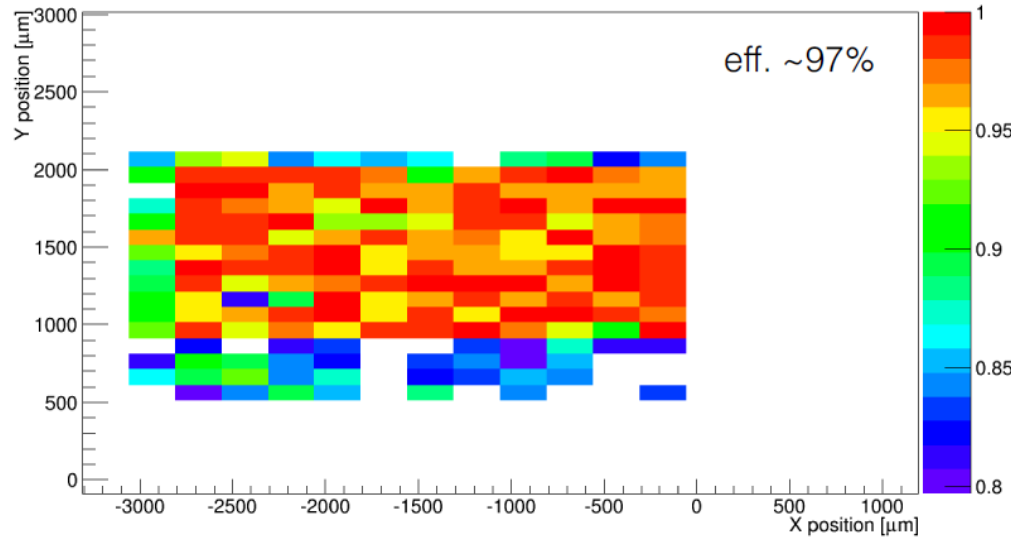

volt-BlineMean:time {z==4.96 && x==6.7}
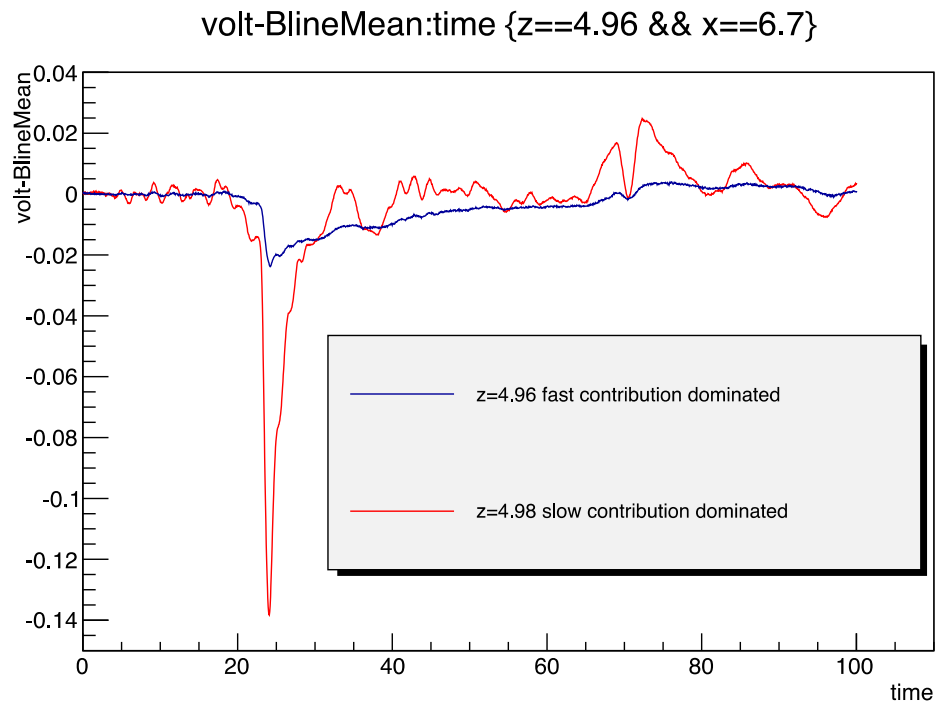
Depleted layer thickness around 15 μm

Bias voltage magnitude increased to the left in these graphs

The quick charge zone increased with bias magnitude

Not irradiated

Irradiated 10^{15} n_{eq}/cm^2

at Jozef Stefan Institute

Signal collected within first 3ns

Ivan Peric: CPIX14, Bonn, 2014

42
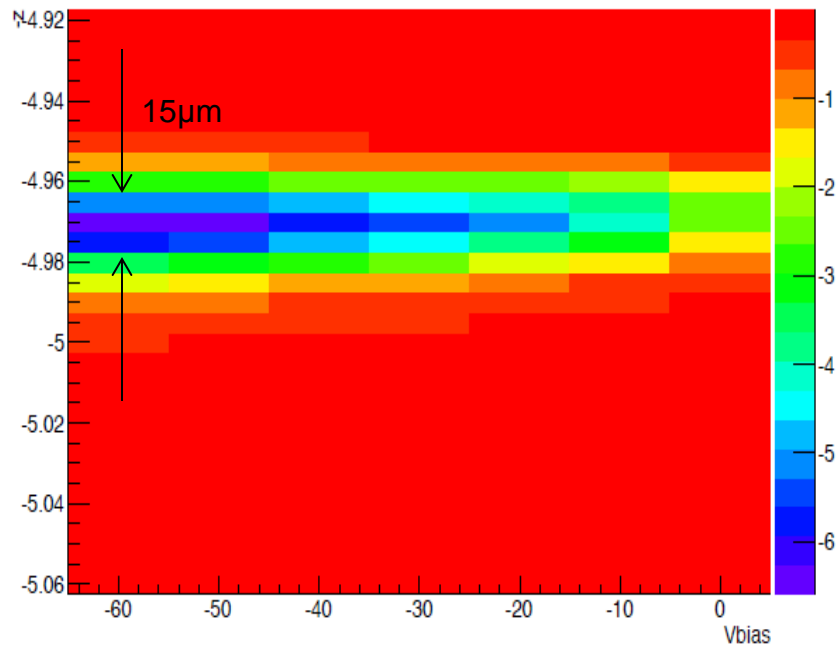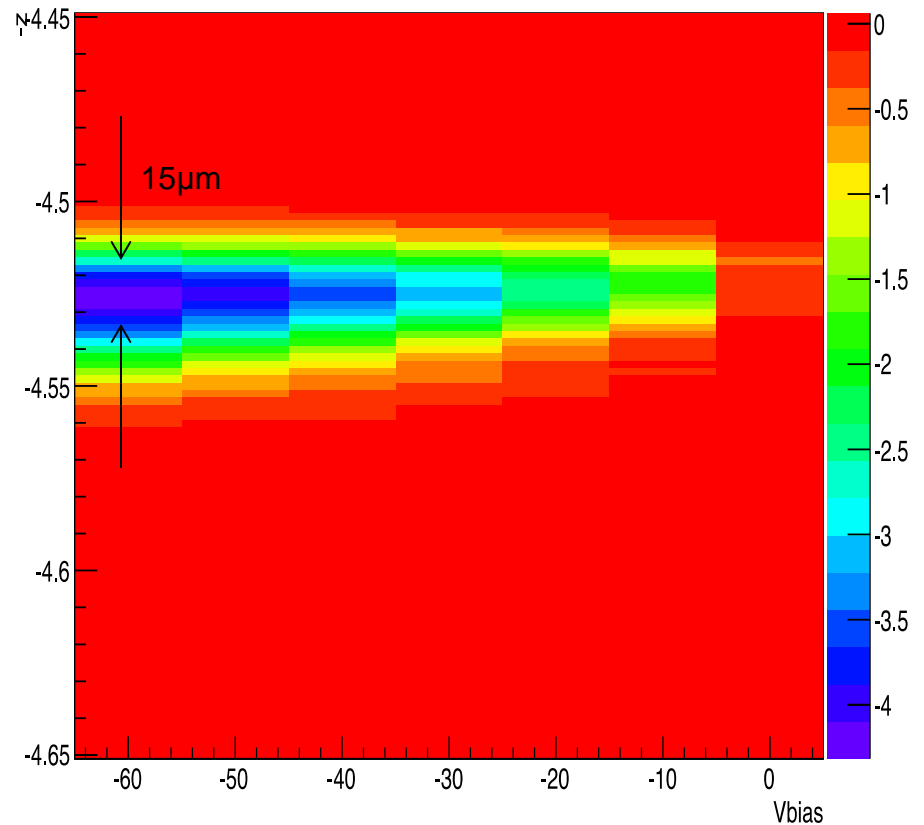
Depleted layer thickness is around 15 µm

Signal collected within first 3ns
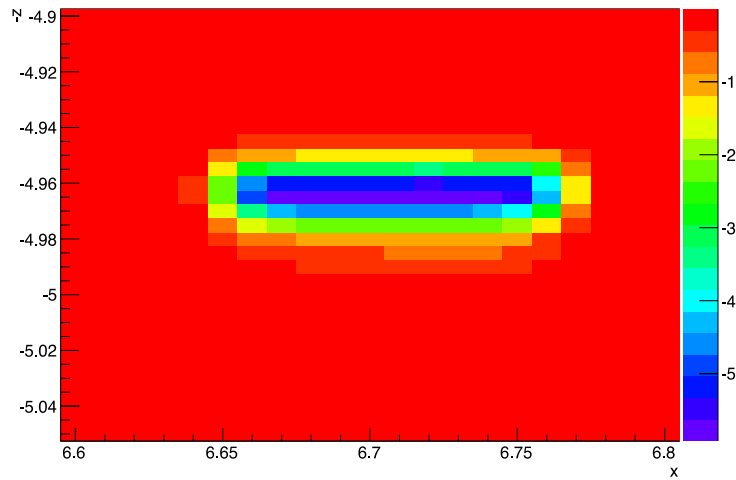
Not irradiated
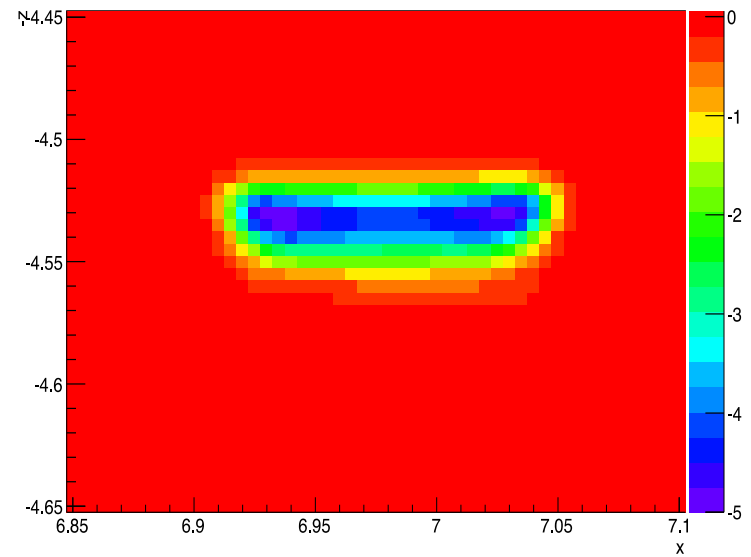
Irradiated 10^{15} n_{eq}/cm^2

at Jozef Stefan Institute

When the HV2FEI4v3 sensor was irradiated its slow signal was reduced by an order of magnitude.

A possible explanation could be trapping of charge carriers

The fast signal, however, did not loose significant height in the conditions considered

Not irradiated
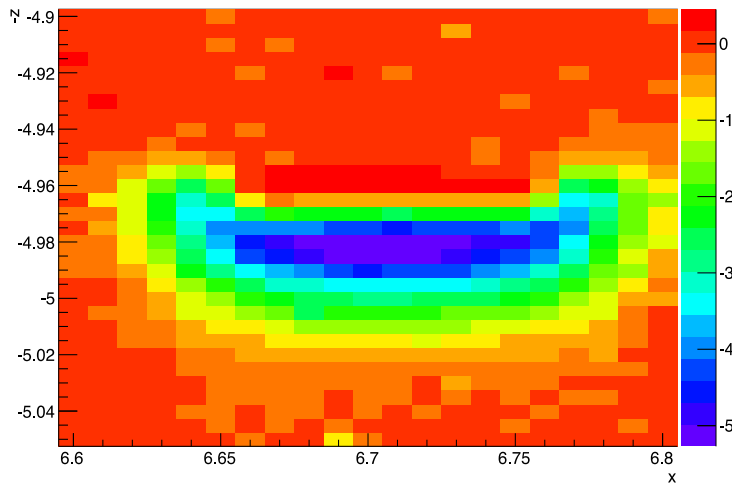
Irradiated 10^{15} n_{eq}/cm^2
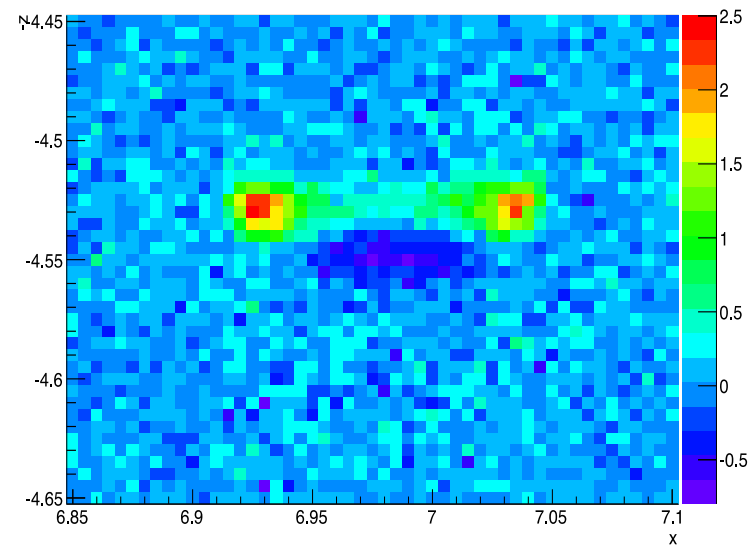
at Jozef Stefan Institute

Signal collected within first 3ns

The fast signal, however, did not loose significant height in the conditions considered

volt-BlineMean:time-16.3 {x==6.71 && z==4.97}
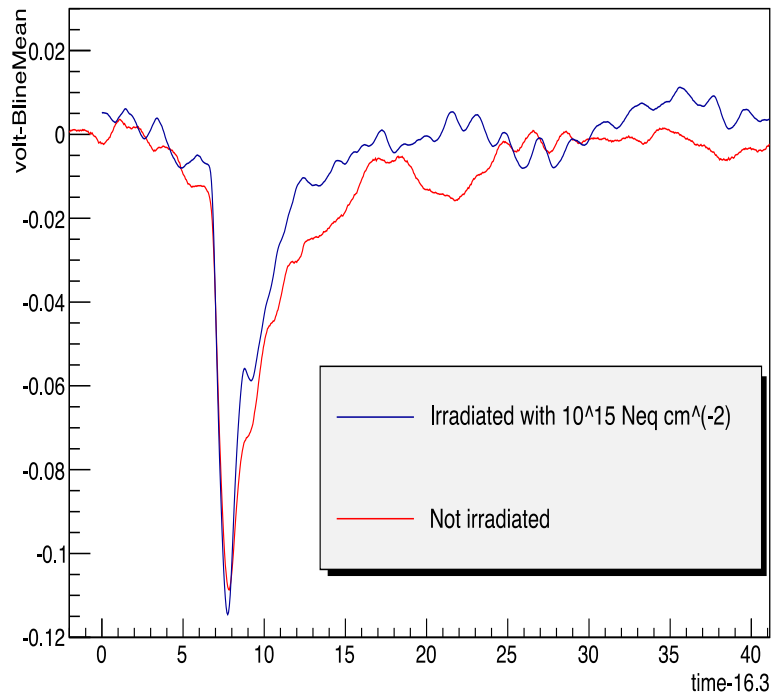
volt-BlineMean:time {x==6.98 && z ==4.56}
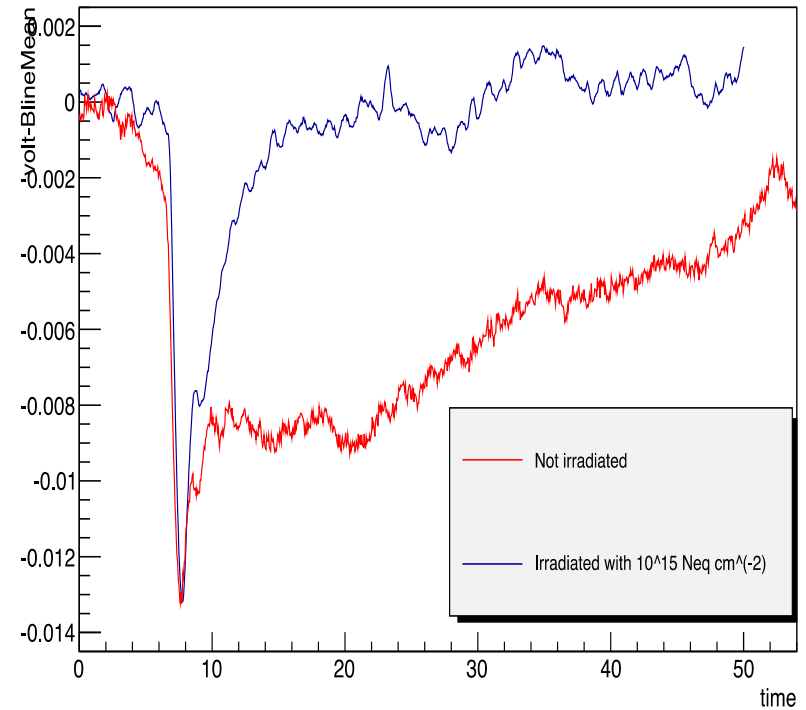
- Average pixel noise ~ 75e (large spread)
- Threshold tuning: dispersion ~ 25e
- Measured MIP signal at 60V: 1600e/1180e
- Required:
- 6 x SD(Noise) + 6 x SD(Threshold) = Smallest signal
- 600e = Smallest signal?
- Question: Smallest signal for MPW = 1100e (probably ~ 1180/2 = 600 e)
- We are almost there
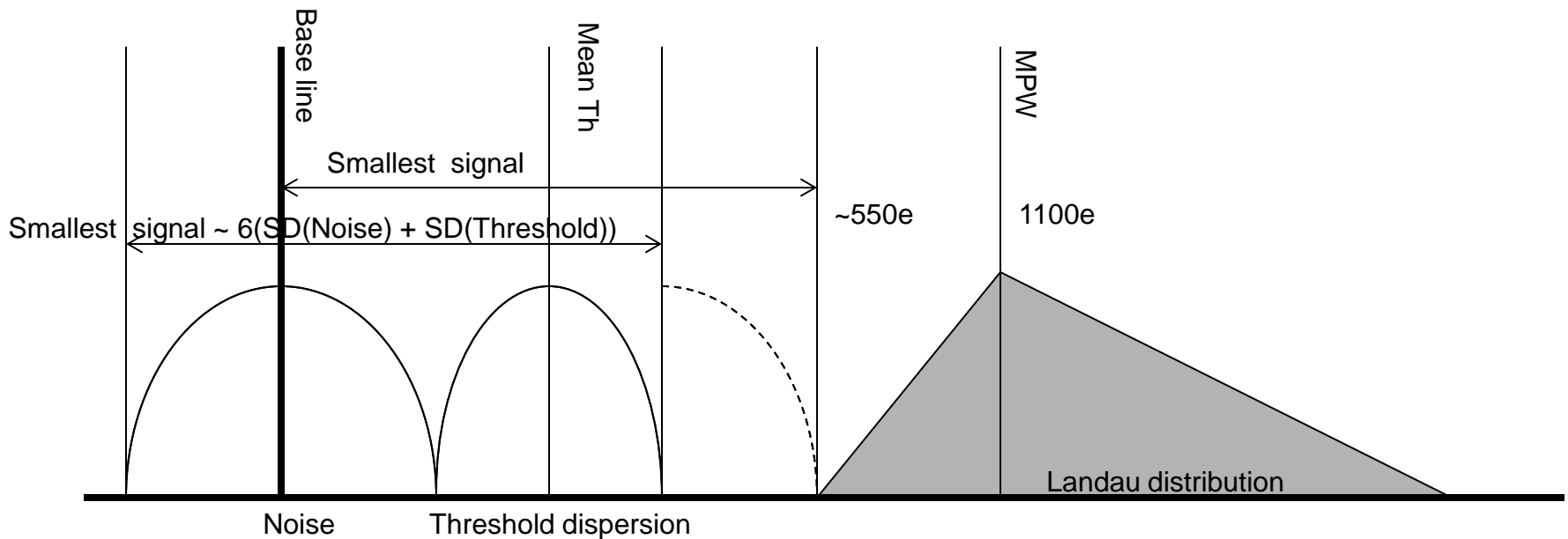
CLIC

- CLIC requirements – little material, high spatial and time resolution
- Option: capacitively coupled pixel detector
- Test detector has been produced (CCPDv3) that can be readout with CLICPIX chip
- Pixel size: 25 µm x 25 µm
- Every HVCMOS pixel has its own readout cell

Size: 25 µm x 25 µm

Readout pixel

Size: 25 µm x 25 µm
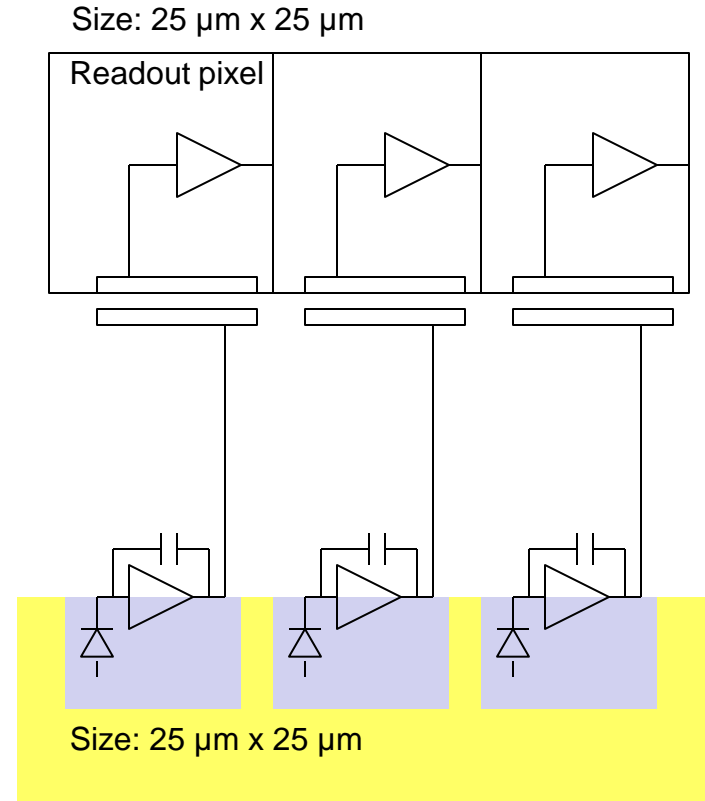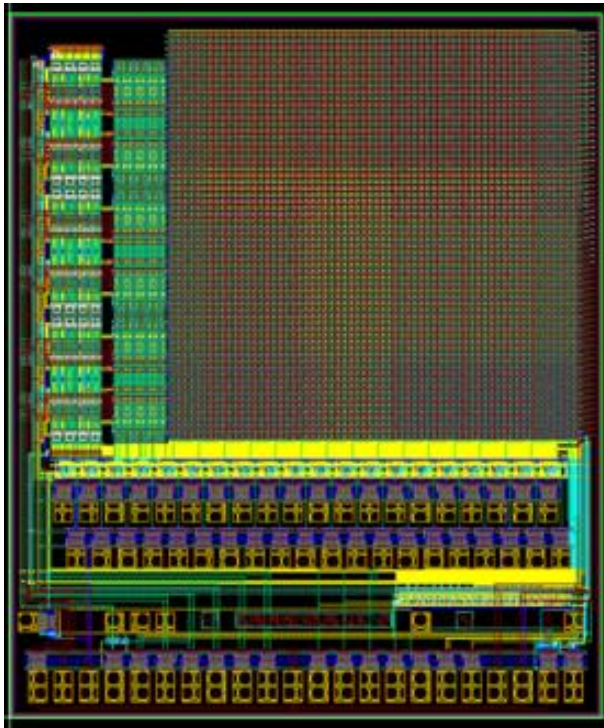
- CLIC pixels – excellent SNR
- Noise for small pixels (25 µm x 25 µm) with analog readout 30e
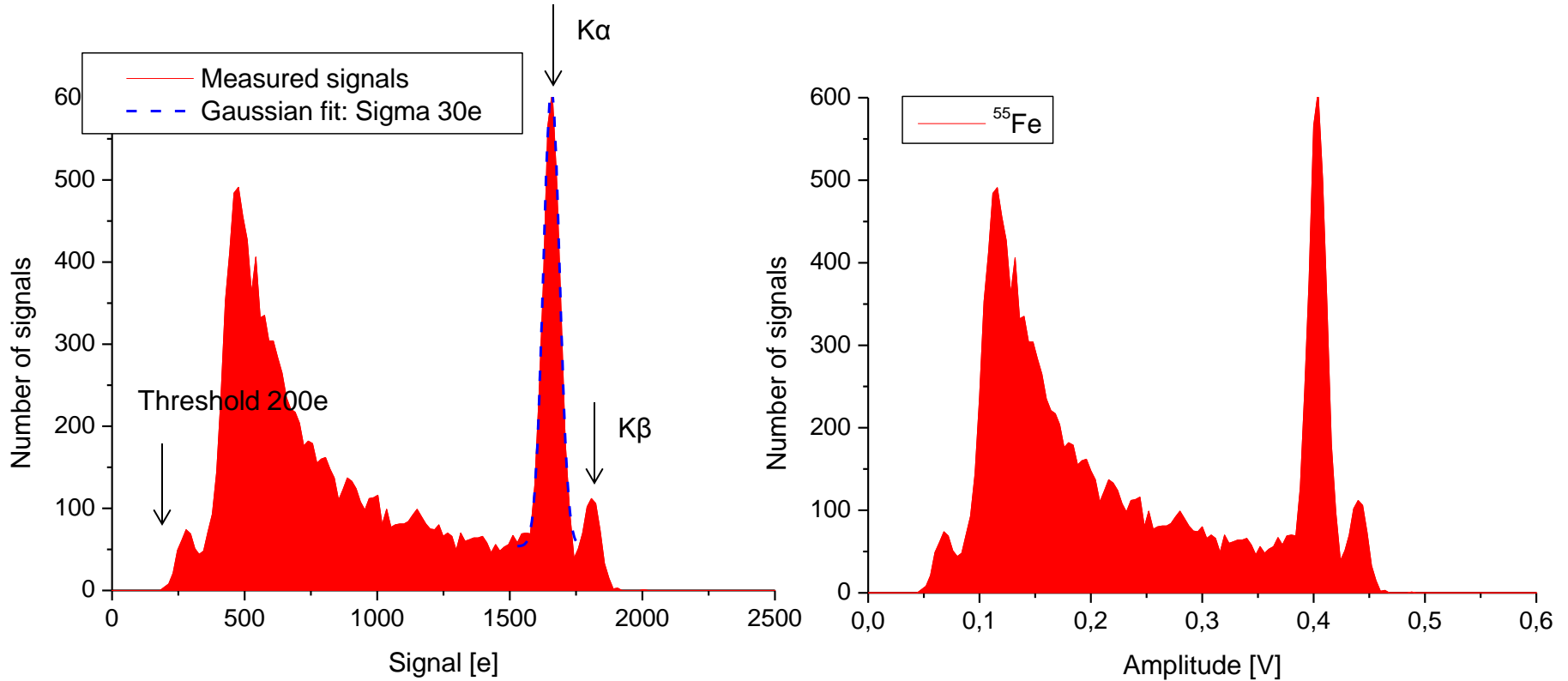
ATLAS Strips

One of possible concepts: Strips are segmented into (long) pixels. Every pixel has its own readout cell, placed on the chip periphery

The periphery generates pixel addresses with a constant delay respecting the hit

Redundant address lines used to cope with simultaneous hits

Strip readout chip (like ABCN) replaced by a purely digital chip (based on existing digital parts)

CSA

Pixel contains a charge sensitive amplifier

Present scheme

ABCN chip

Possible HVCMOS scheme

Digital chip

Pixels

Comparator block

Config. register

Readout block

Ivan Peric: CPIX14, Bonn, 2014

pix

amp

Active pixels

pix

amp

pix

amp

pix

amp

Comp out rising edge

40MHz clock

Synchronizer

Sync hit

Parity in

xor

Parity out

demux

Comp out

↑ ↑ ↑ ↑   clock

Sync hit

Addr

Digital RO

Addr
Addr

Address line 1

Address line 2

Normal comp.

cn ctw

cn ctw

cn ctw

cn ctw

Comparator (time walk compensated)

TWC comp.

Comparator (normal)

Analog multiplexer

SR1   SR2

Digital
RO

Digital
RO

Digital
RO

Digital
RO

6-bit address, hit1,ParOut

6-bit address, hit2,ParOut

serializer

serializer

320MHz clock

40MHz clock

config

config

Mu3e

Mu3e Detector

- Search for particle event μ+ -> e+e-e+
- High muon decay rate 10^9/s
- Low momentum resolution 0.5 MeV/c
- Vertex resolution 100 μm
- Time resolution 100 ns (pixels) (1 ns scintillator fiber)
- Four pixel layers 80x80μm^2 pixel size, 275 MP
- Pixel detector thickness: ~50 μm
- Cooling with helium
- Pixel detector area: 1.9 m^2
- Heidelberg, PSI, Zürich, Genf

Recurl pixel layers   Outer pixel layers

Scintillator tiles

Inner pixel layers

Scintillating fibres

Mu3e Detector

Thinned chips

Kapton PCB &
Supporting structure

1cm

Pixels – active region

~0.5 mm

EoC logic

Ivan Peric: CPIX14, Bonn, 2014
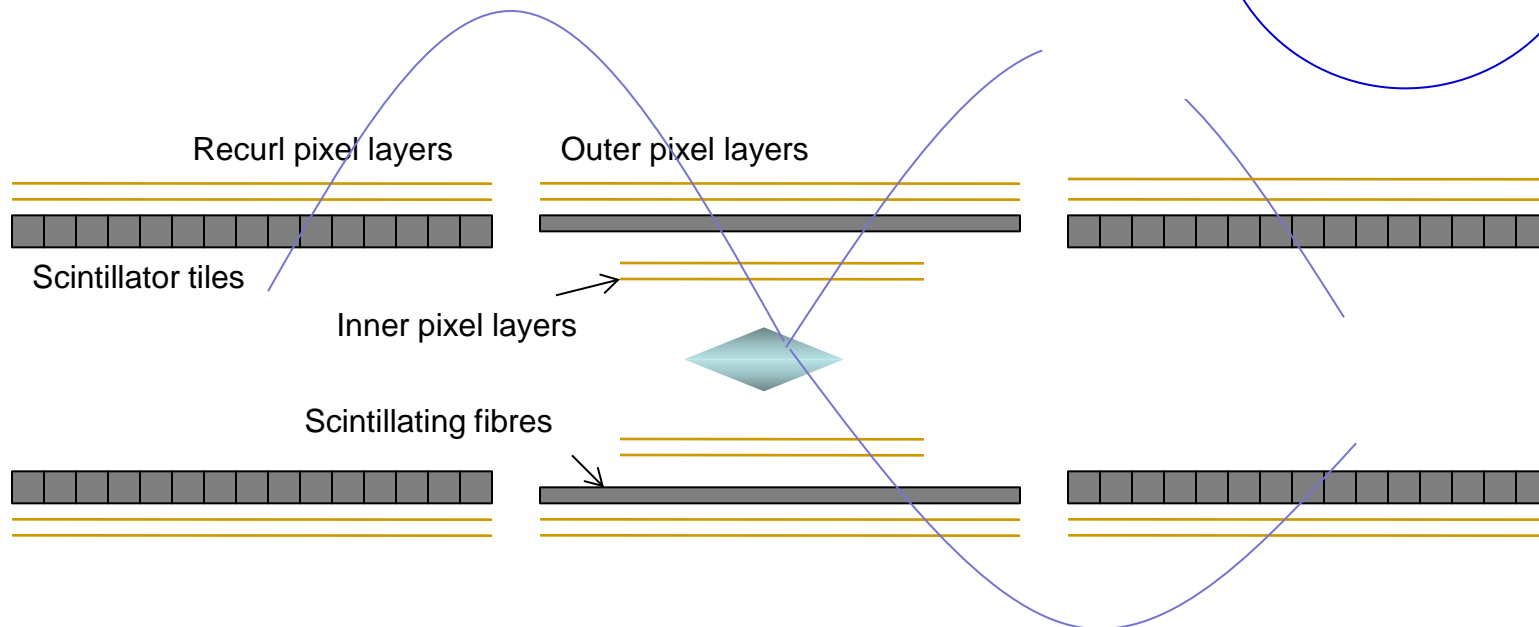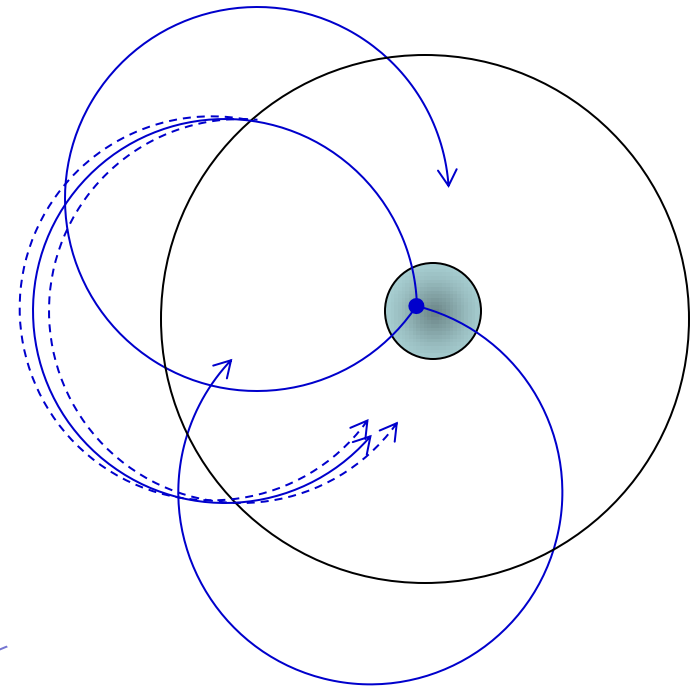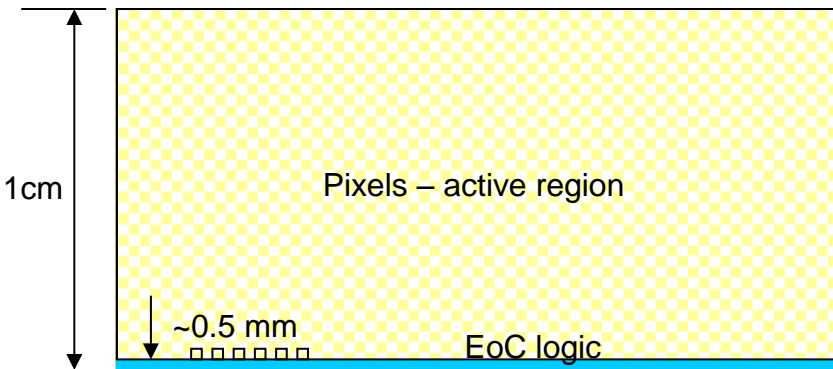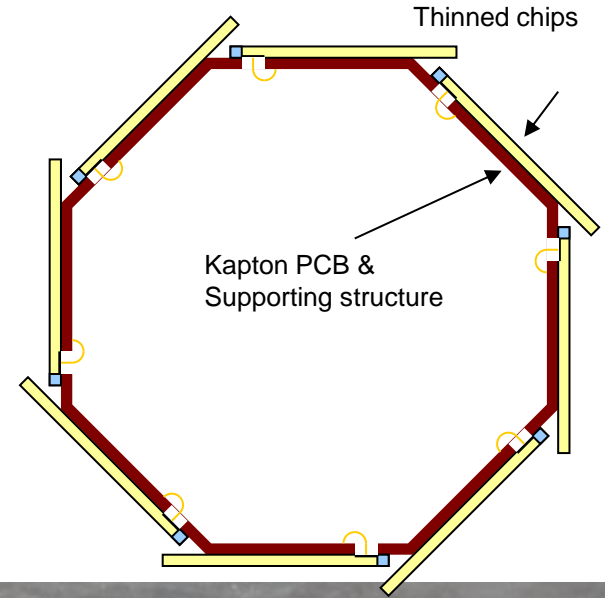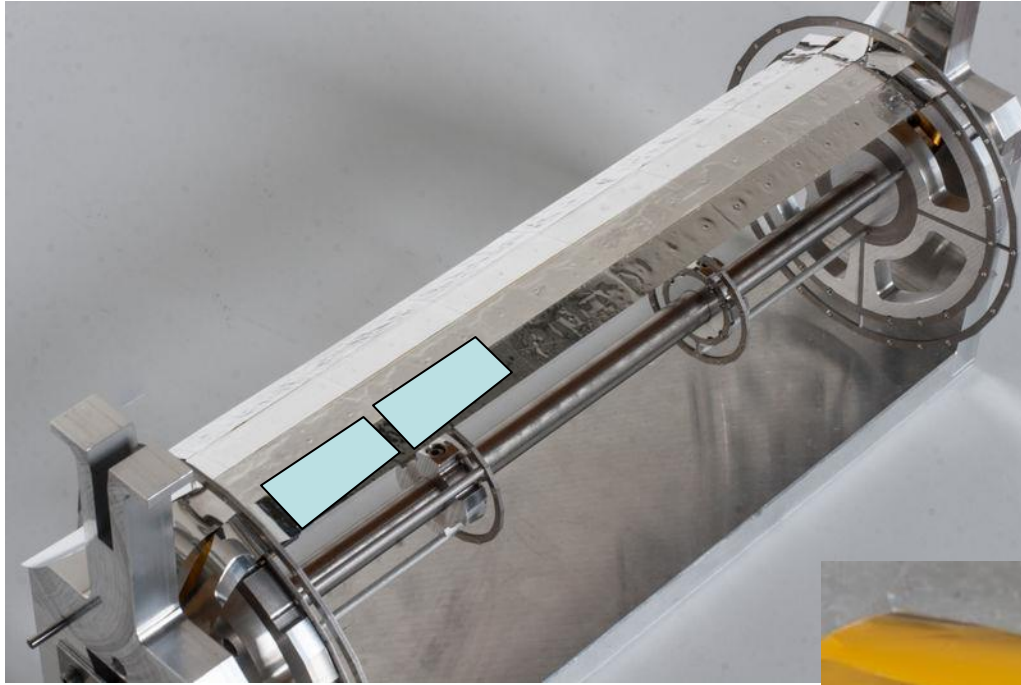
Concept: Every pixel has its own readout cell, placed on the chip periphery

Hit flag

RAM/ROM

Priority scan logic

CSA

Comparator
and Thr tune DAC

Time stamp   Data bus

Read

Pixel contains a
charge sensitive
amplifier

Readout cell function – time stamp is stored when
hit arrives
Hit data are stored until the readout
Priority logic controls the readout order
RO cell size in 0.18 μm AMS technology ~ 7 μm x
40 μm
(with comparator and threshold-tune DAC)

One RO cell
/pixel

Row/Col Addr + TS

3 mm

One pixel

92μm

Readout cell

Ivan Peric: CPIX14, Bonn, 2014

MuPixel test beam

- Test-beam measurement February 2014 DESY
- Result analysis: Moritz Kiehn, Niklaus Berger, PI Heidelberg
- 99% efficiency measured

Ivan Peric: CPIX14, Bonn, 2014

- Test-beam measurement October 2013 DESY
- Time resolution: 18ns (sigma) (not corrected for the pixel to pixel delay dispersion and charge sharing)

Timestamp difference to trigger

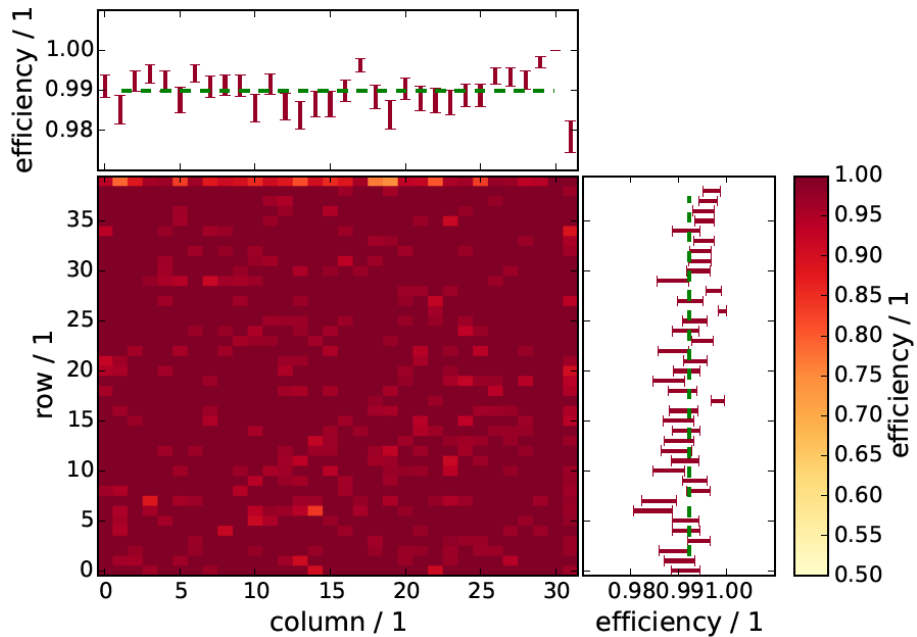| tsdiff	
Entries	56654
Mean	-0.2087
RMS	14.38
c^2 / ndf	1228 / 63
p0	3325 ± 53.0
p1	-2.7 ± 0.0
p2	0.9323 ± 0.0114
p3	174.5 ± 1.7

~ 18 ns time resolution? includes FPGA and TLU

18ns sigma

Probably caused by indirect hits

20 ns bins

Ivan Peric: CPIX14, Bonn, 2014
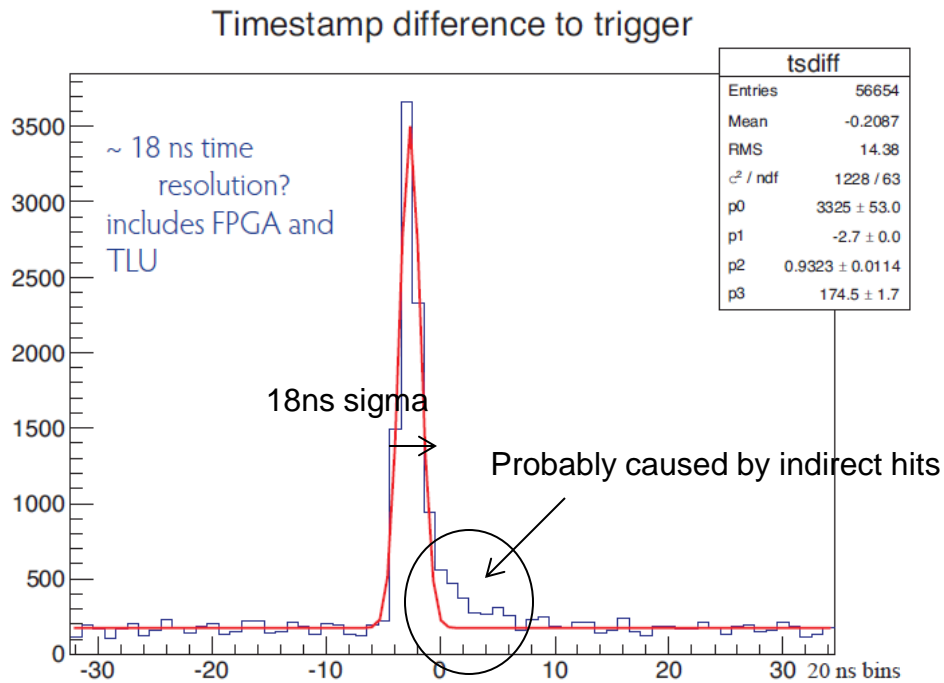
Thin detectors

- Chips have been thinned to < 100 μm and successfully tested

THICK   450 MeV pion signals

THIN

Ivan Peric: CPIX14, Bonn, 2014
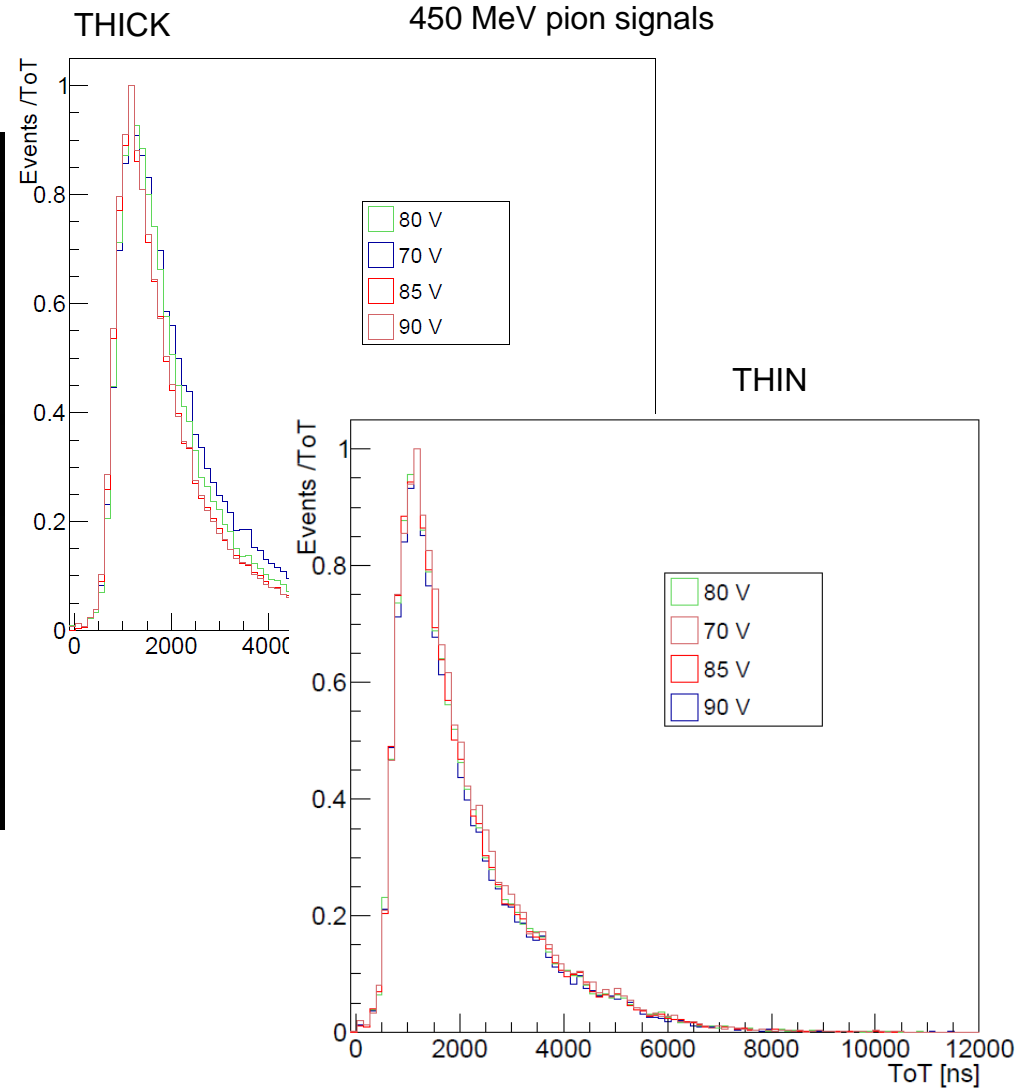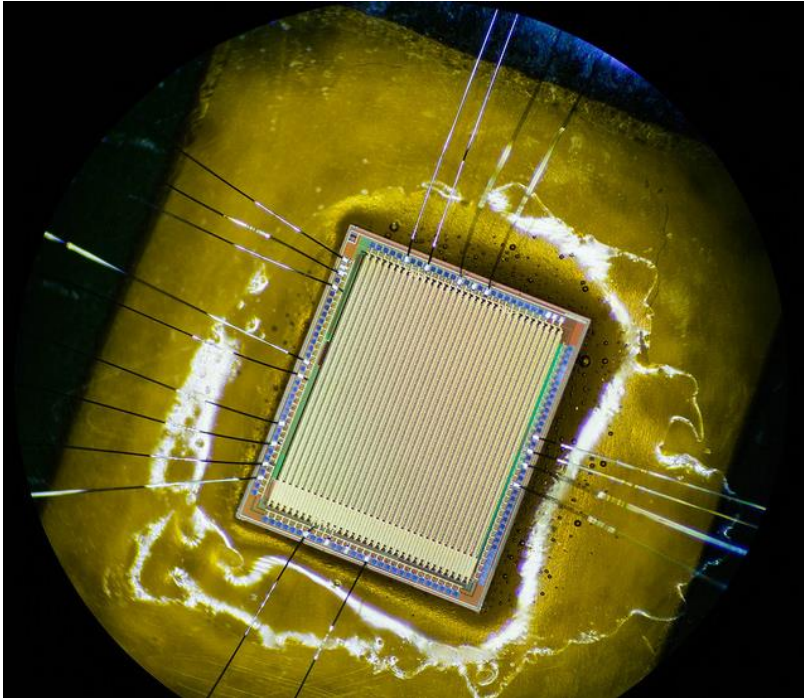
New prototypes

- April 2014 a chip version (MuPix6) with improved threshold-tuning circuitry and two stage amplification produced
- August 2014 new chip version (MuPix7) with high speed serial transmission (up to1.6GBit/s) submitted
- The chips have been ordered thinned to < 50 μm
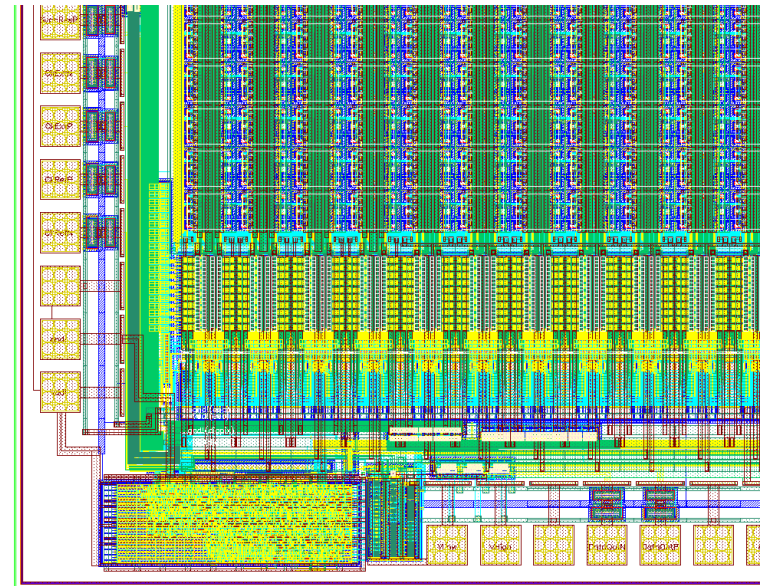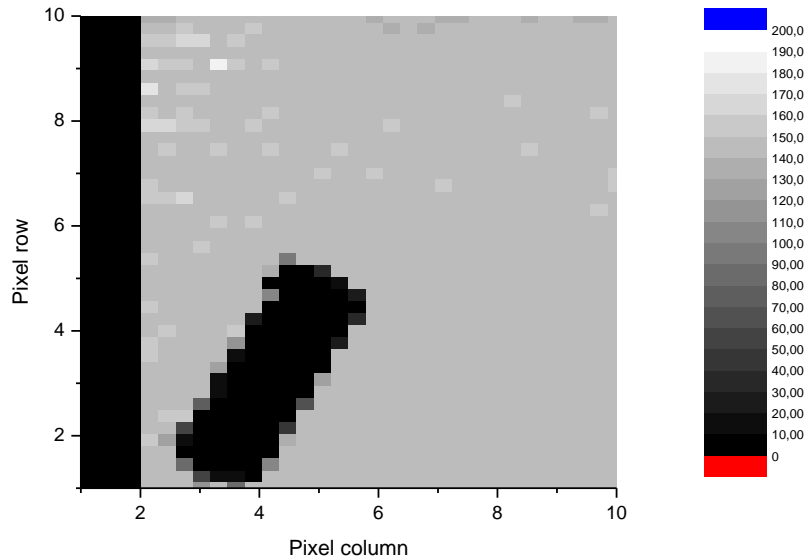
Summary

- HVCMOS sensors are options for ATLAS pixels, ATLAS strip-layers, CLIC and Mu3e experiments
- **Mu3e:**
- Several test chips have been successfully tested
- Trigerless readout, time resolution <100ns
- Efficiency of ~99% have been measured in test beam
- Chips have been thinned to <100μm and they work
- **ATLAS:**
- We are developing prototypes that can be readout using FEI4
- Capacitively coupled pixel sensors in AMS technology – segmented pixels
- We measure good SNR (~20) after 10^{15} n_{eq}/cm^2, detectors work after 800MRad
- Test-beam results are still preliminary, efficiency ~97%
- We are planning to improve the SNR by reducing the noise and/or implementing of sensors on 100 Ωcm substrates
- **CLIC:**
- HVCMOS CCPD with 25μm x 25μm pixels capacitively readout with CLICPIX has been successfully tested
- High SNR measured, first test beam measurement done in August
- **ATLAS strip layers**
- HVCMOS sensor are an option for ATLAS strip layers
- HVCMOS sensor prototype (segmented strips) has been produced in AMS H35 technology
- Hit information transmitted digitally via several address links to the digital readout chip (based on the digital part of ABCN chip) constant delay multiplexing