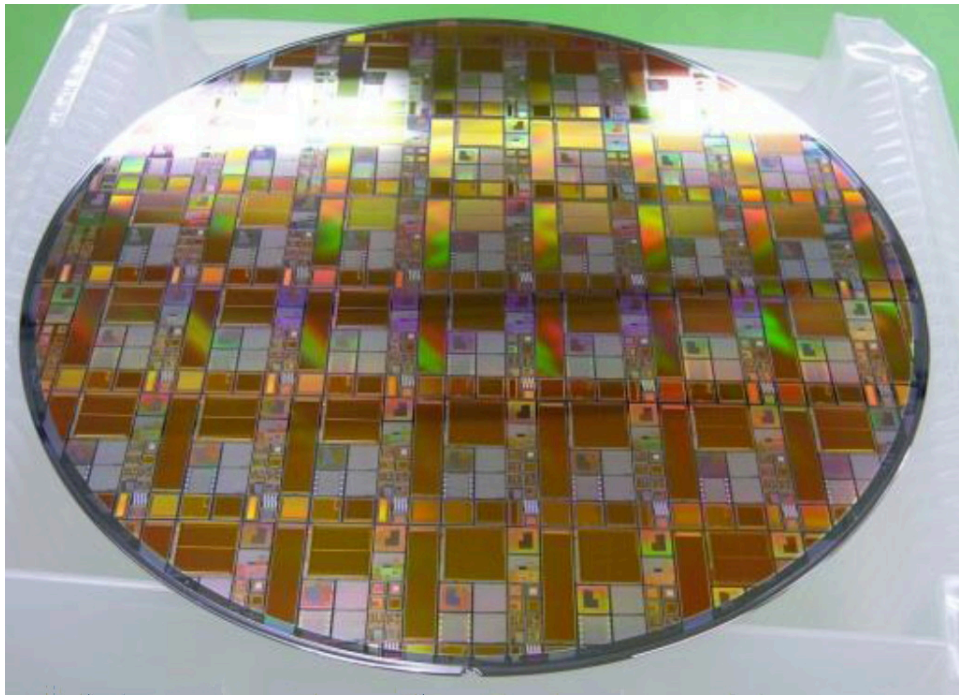
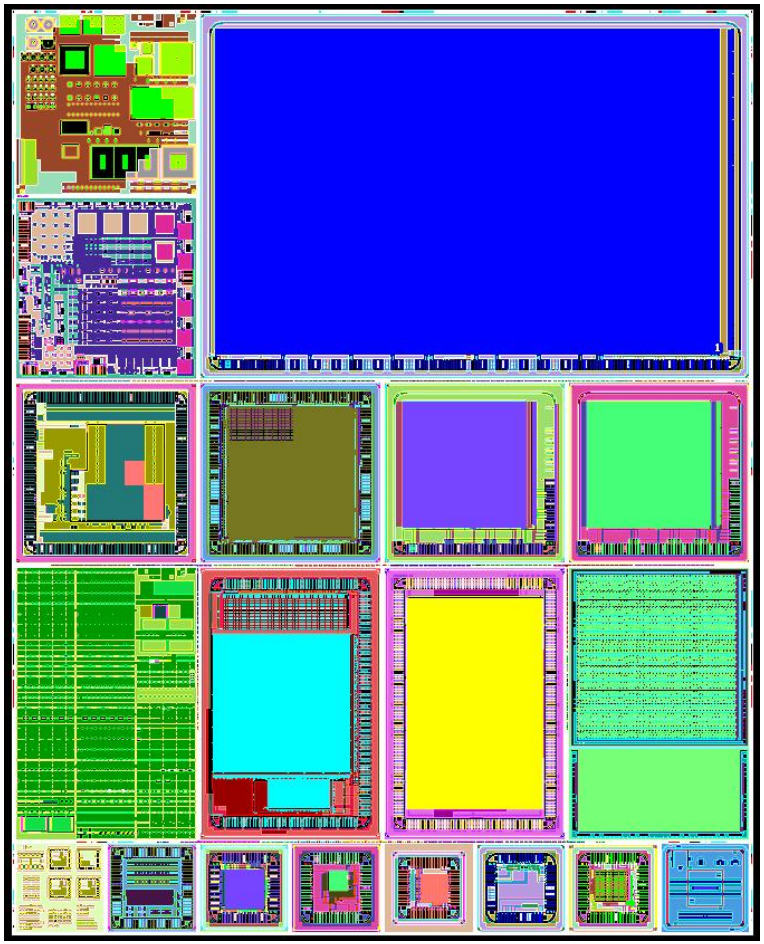
Lapis SOI Technology and Activities



Sep. 17, 2014
CPIX14@U. of Bonn
Yasuo Arai, KEK
On behalf of the SOIPIX Collaboration
yasuo.arai@kek.jp
http://rd.kek.jp/project/soi/

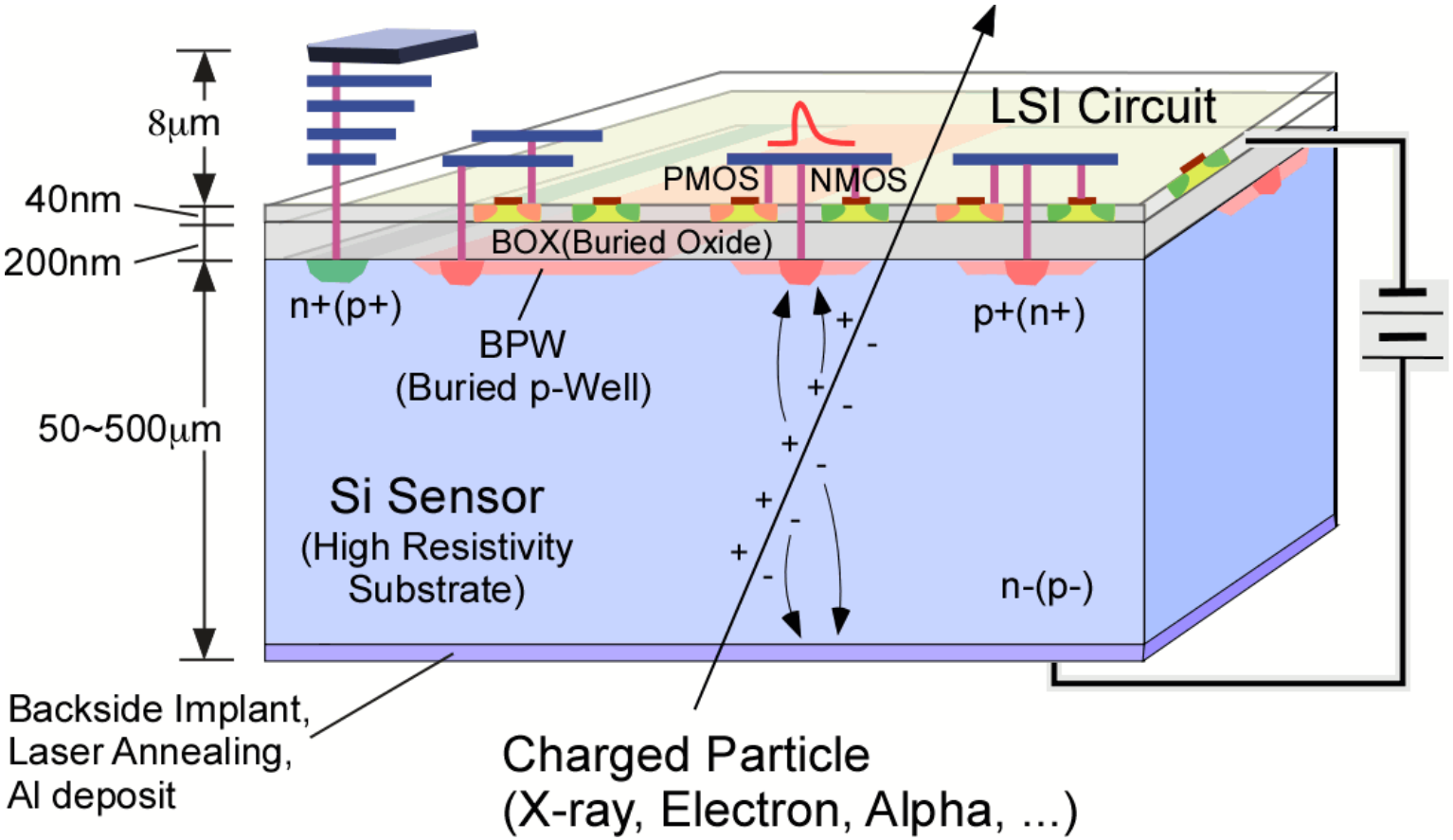
Outline

I. Introduction
II. Collaboration
III. Double SOI
IV. New Developments
V. Summary



I. Introduction

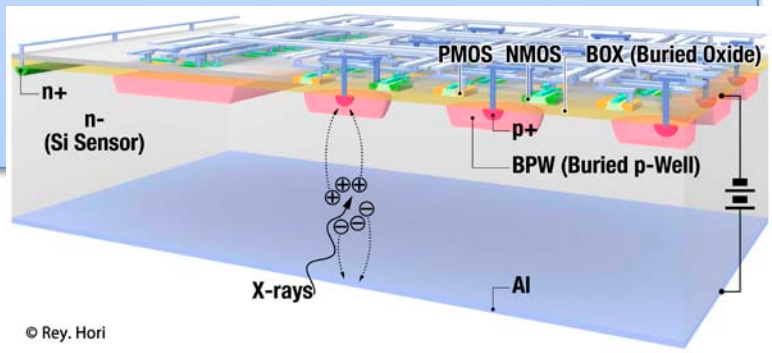
Silicon-On-Insulator Pixel Detector (SOIPIX)



High Resistivity Substrate + CMOS Circuit

Features of the SOI Pixel Detector

- No mechanical bonding. Fabricated in industrial semiconductor process.
- Full CMOS transistors are available.
- Thickness of the sensor is adjustable（50~500um), and possible to operate in full depletion. (Wide Application)
- Low sense node capacitance and possible to fabricate custom sensor structure.
- No latch up and Low single event cross section.
- Can be operated in wide temperature (1K-570K) range.



Lapis Semiconductor 200 nm FD-SOI Pixel Process

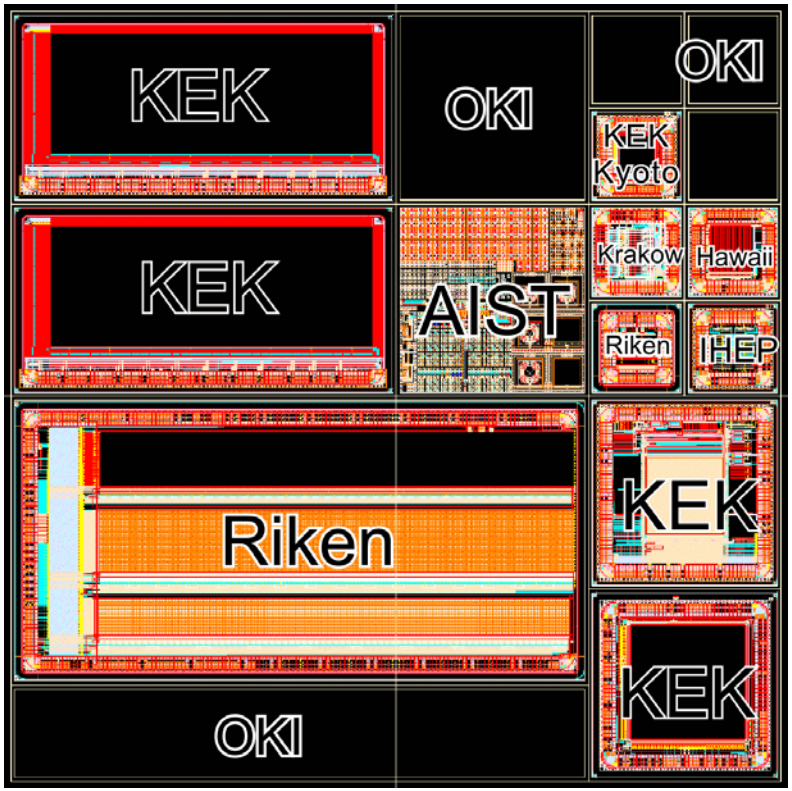
Process	200 nm Low-Leakage Fully-Depleted SOI CMOS 1 Poly, 5 Metal layers. MIM Capacitor (1.5 fF/um^2), DMOS Core (I/O) Voltage = 1.8 (3.3) V
SOI wafer	Diameter: 200 mmϕ, 720 μm thick Top Si : Cz, ~18 Ωcm, p-type, ~40 nm thick Buried Oxide: 200 nm thick Handle wafer: Cz (n) ~700 Ωcm, FZ(n) ~7k Ωcm, FZ(p) ~25 k Ωcm etc.
Backside process	Mechanical Grind, Chemical Etching, Back side Implant, Laser Annealing and Al plating

Regular MPW run (~2 runs/year) operated by KEK

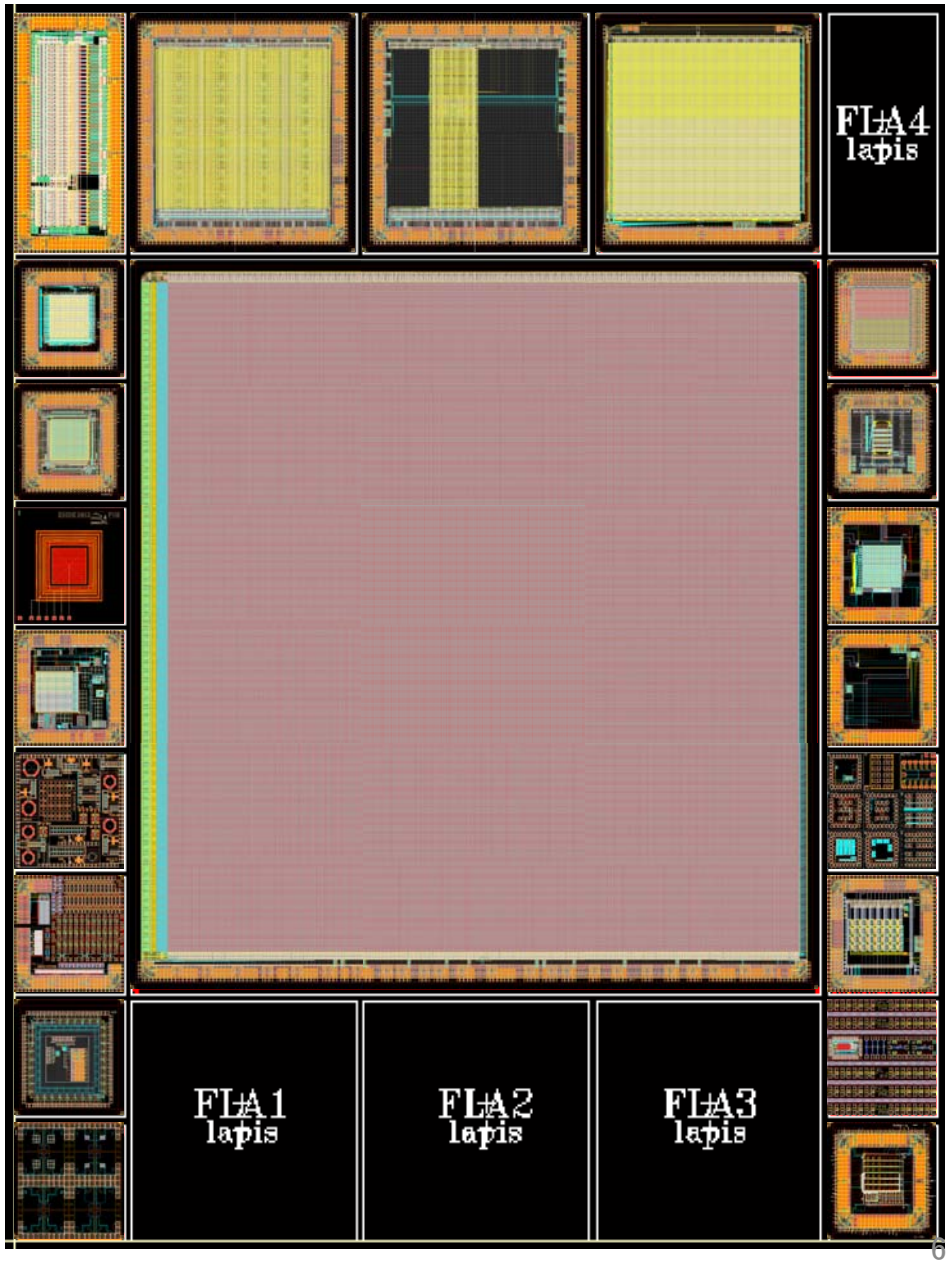
Reticule size

Relatively large reticule is used to ease large detector and include many designs in the MPW.

Old: 20.6 x 20.6 mm

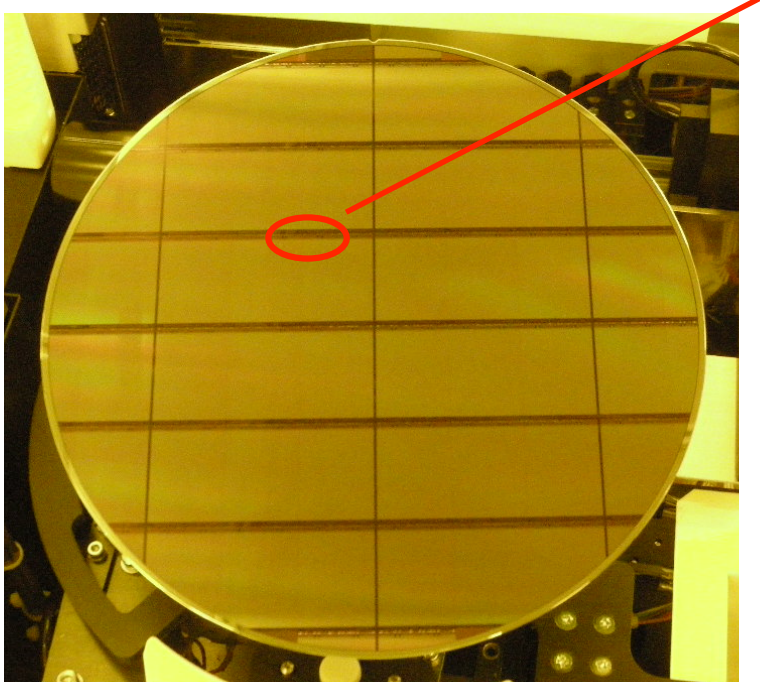


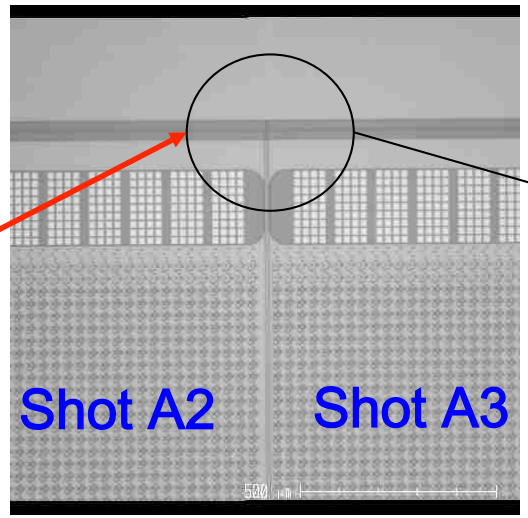
24.6 x 30.8 mm

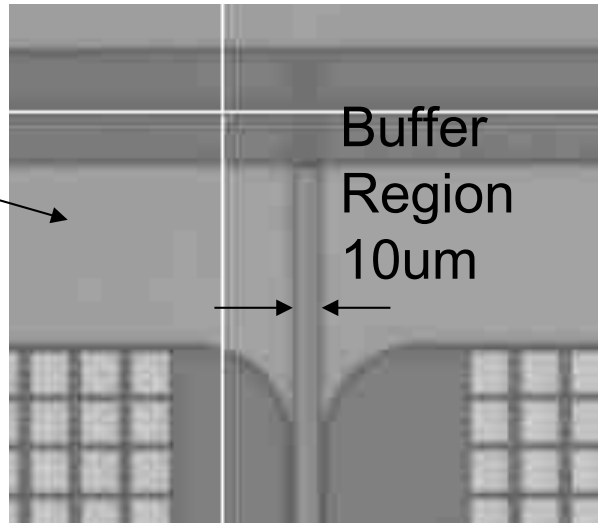


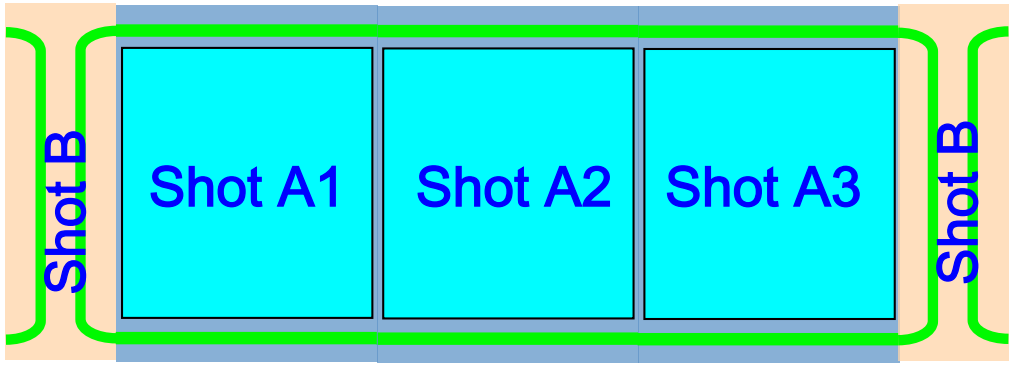
Stitching Exposure for Large Sensor

Produce 26.7 mm x 64 mm Sensing Area (3 Stitching).







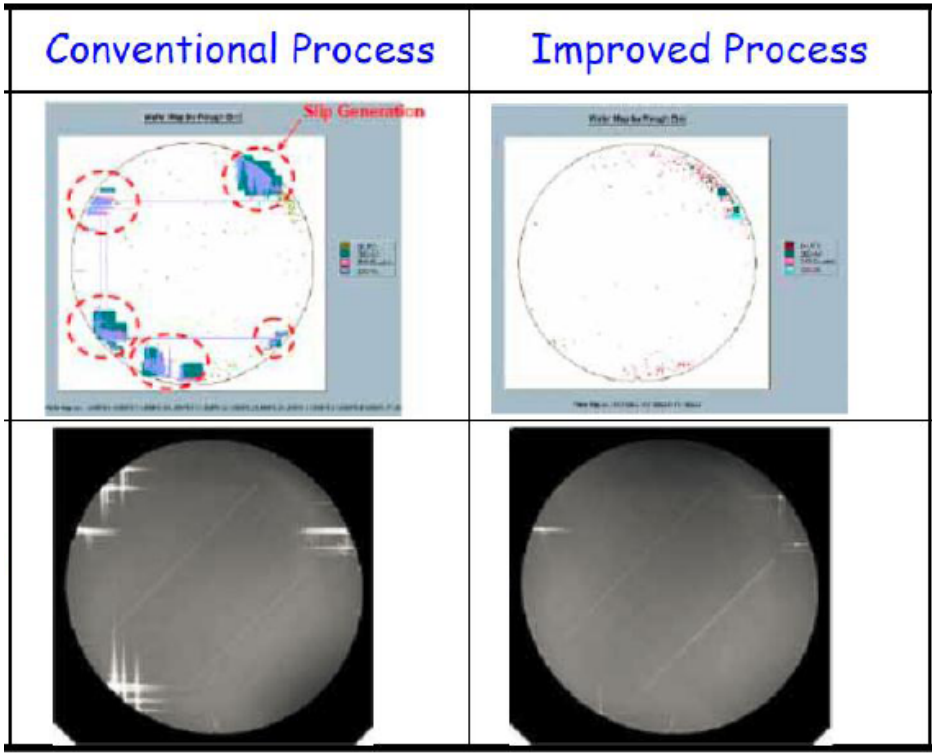


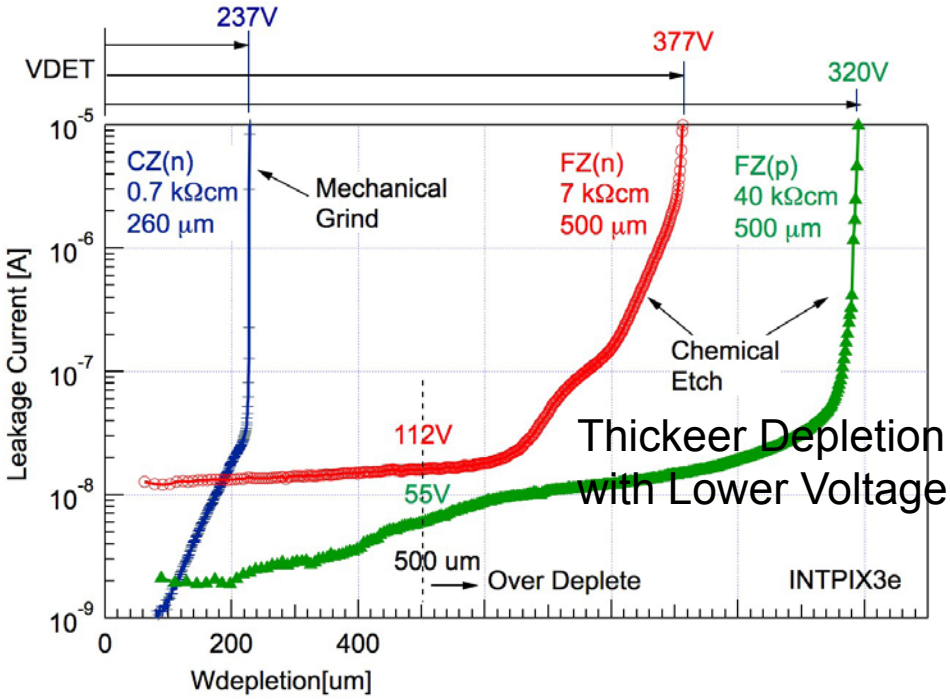
- Width of the Buffer Region can be less than 10um.
- Accuracy of Overwrap is better than 0.025um.
- 1-direction stitching at present.

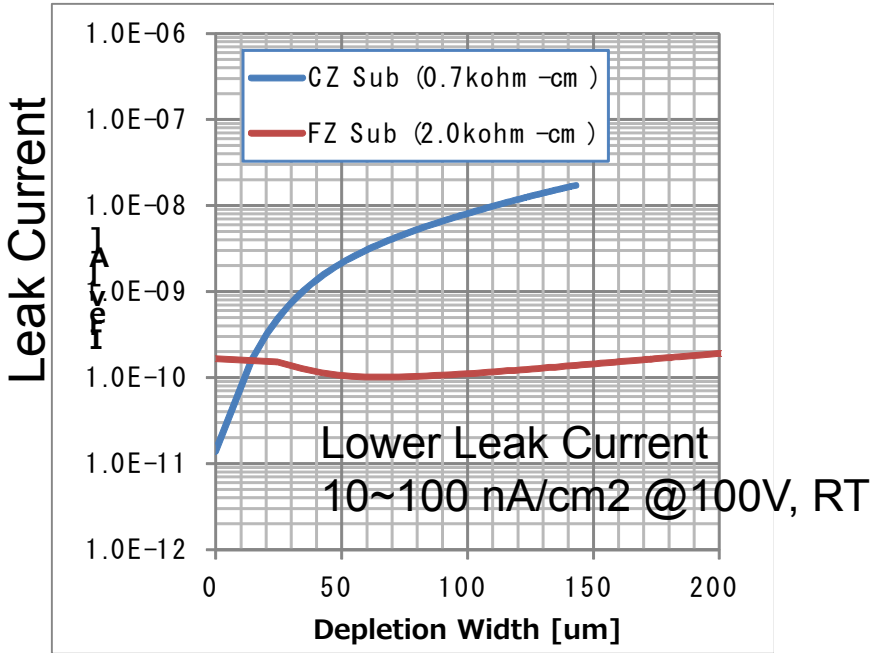
High Resistive FZ(p and n) SOI Wafer

Not only CZ-SOI n-wafer, but also FZ-SOI n/p-wafer (> 2 kOhm•cm) can be used.

Reduction of slip during thermal processes

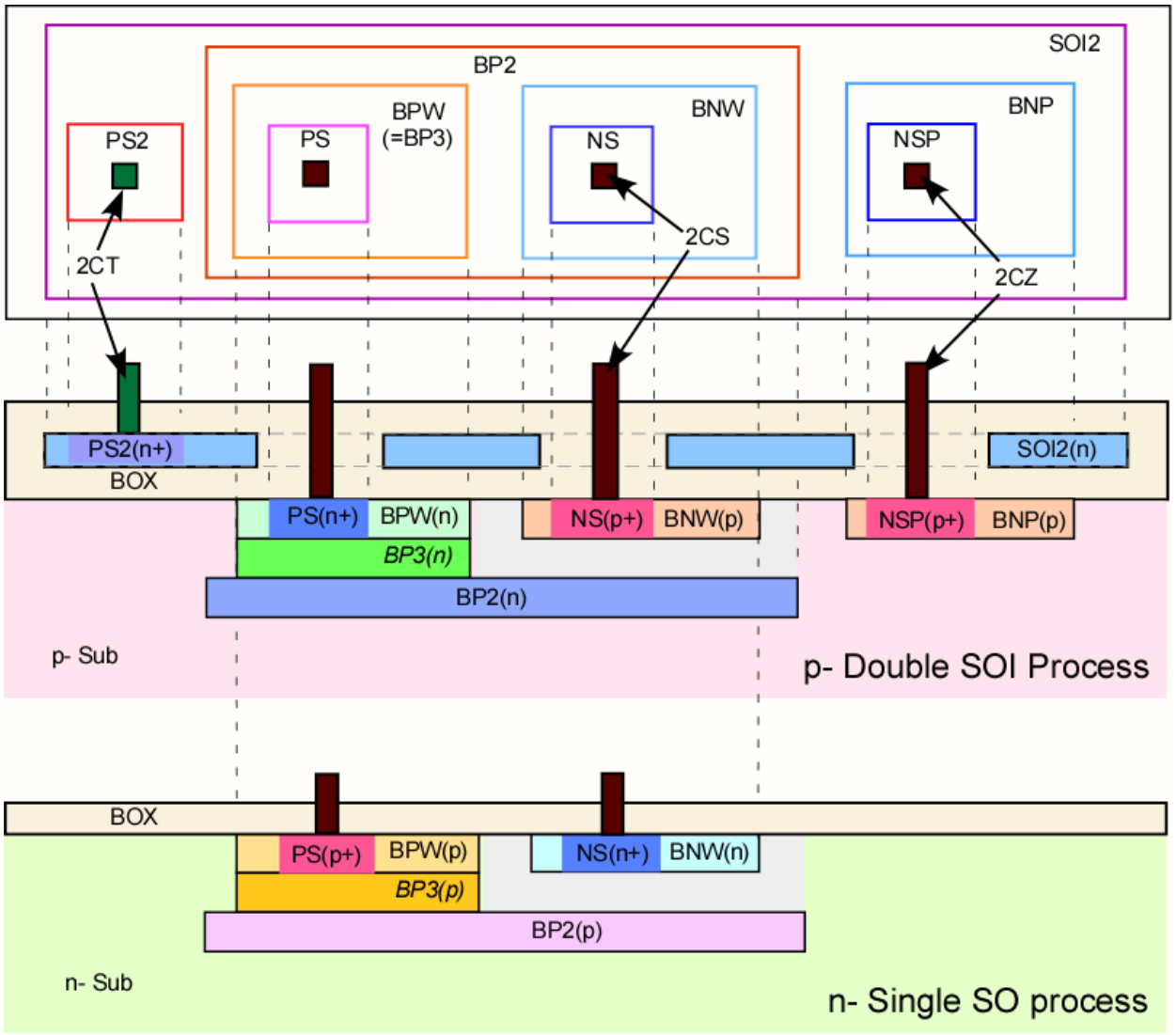






Various Implantation Options in Sensor part

We can fully control implant dose and dpth!

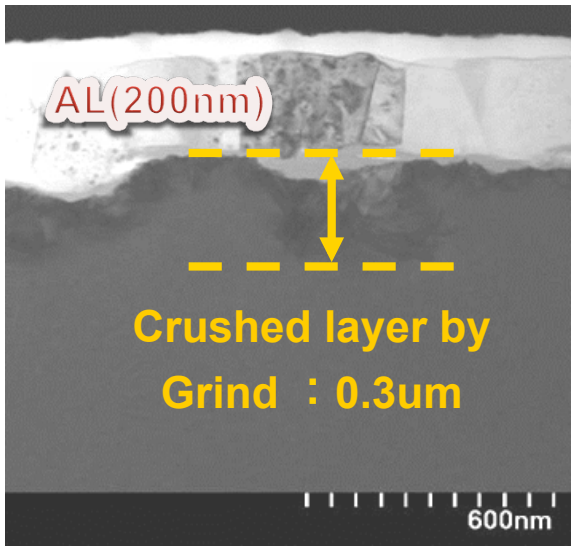


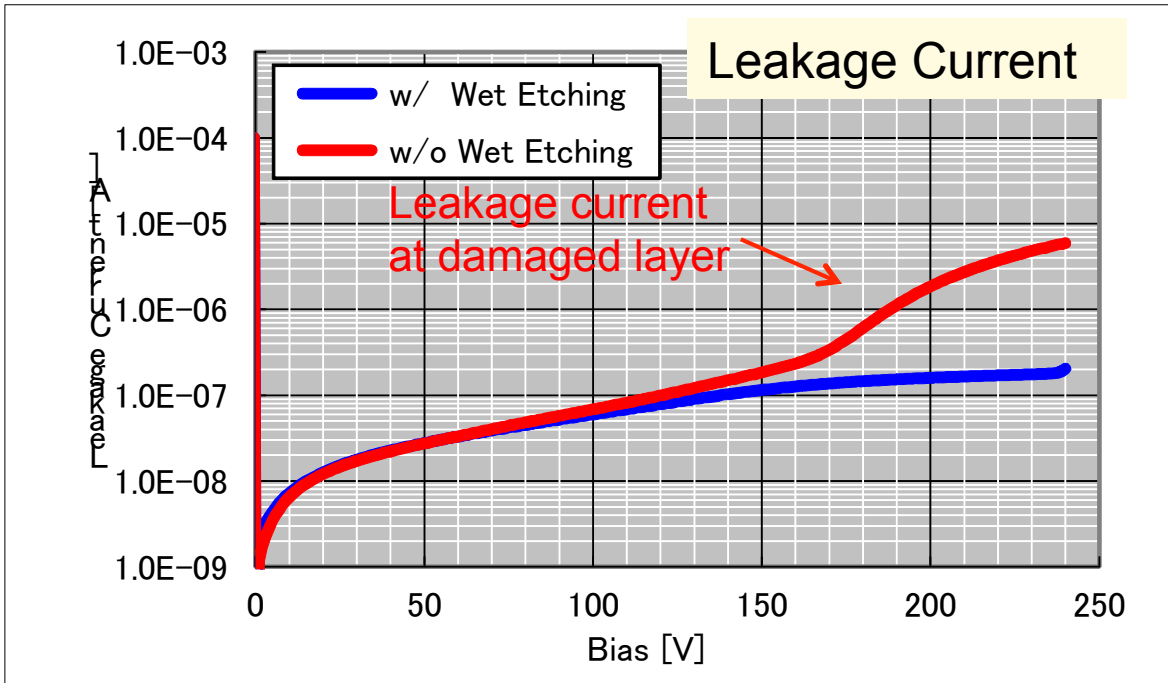
Common Layout can be used for n-, p-substrate and double SOI.

Back Side Process

1. Mechanical Back Grind
2. Wet etching（40um）
3. Ion Implantation
4. Laser Annealing
5. Aluminum deposition（200nm）

Before Wet Etching





After Wet Etching

II. Collaboration

Generic R&D on SOI Detector

KEK

Japan Grant-in-Aid (2013~2018)

- 8 Planned Projects and 7 Applied Projects
- More than 20 Universities and Institutions are involved in many research fields.
  (Riken, Tsukuba U., Kyoto U., Tohoku U., Osaka U., Shizuoka U., JAXA/ISAS, U. of Tokyo, ...)

Collaboration with US
(LBNL, Fermilab, ...)

Collaboration with Europe and Asia
(Krakow, UC Louvain, IHEP, IMECAS ...)

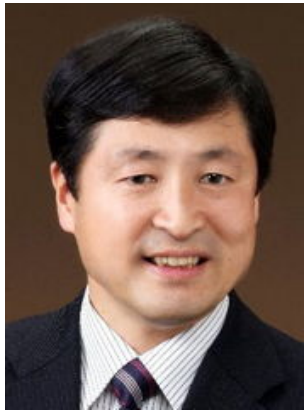
Collaboration with Other Japanese Institutes & Univ.
(NIFS, AIST, JAXA ...)

T-Micro

ROHM GROUP
LAPIS SEMICONDUCTOR

Rigaku

3 New Key Persons are joined



Prof. Nobukazu Teranishi

NEC - Panasonic – U. of Hyogo

Sensor Structure

- Invention of the pinned photodiode for no image lag, low noise and low dark current
- mega –pixel technologies for HDTV cameras and digital still cameras. ...

Prof. Shoji Kawahito

Shizuoka U., CTO of Brookman Technology, Inc.

Low Noise Circuit

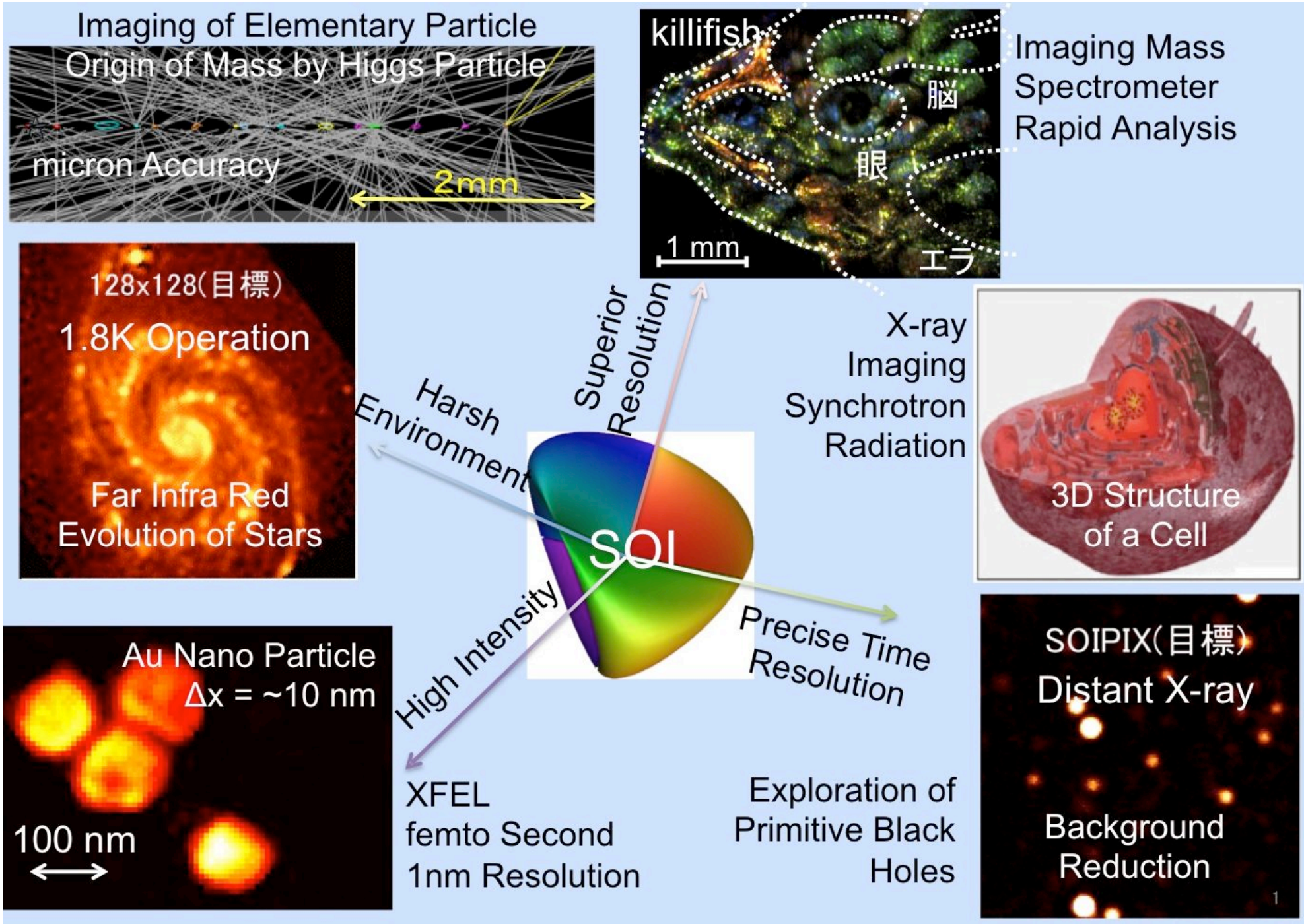
- CMOS Advanced Image Sensors (High Sensitivity, Low Noise, Wide DR, High Speed)
- Mixed signal integrated circuits design (A/D, D/A Converter, Sensor interface circuits) ...
- More than 10 papers were selected in ISSCC in the last 10 years.

Prof. Ikuo Kurachi

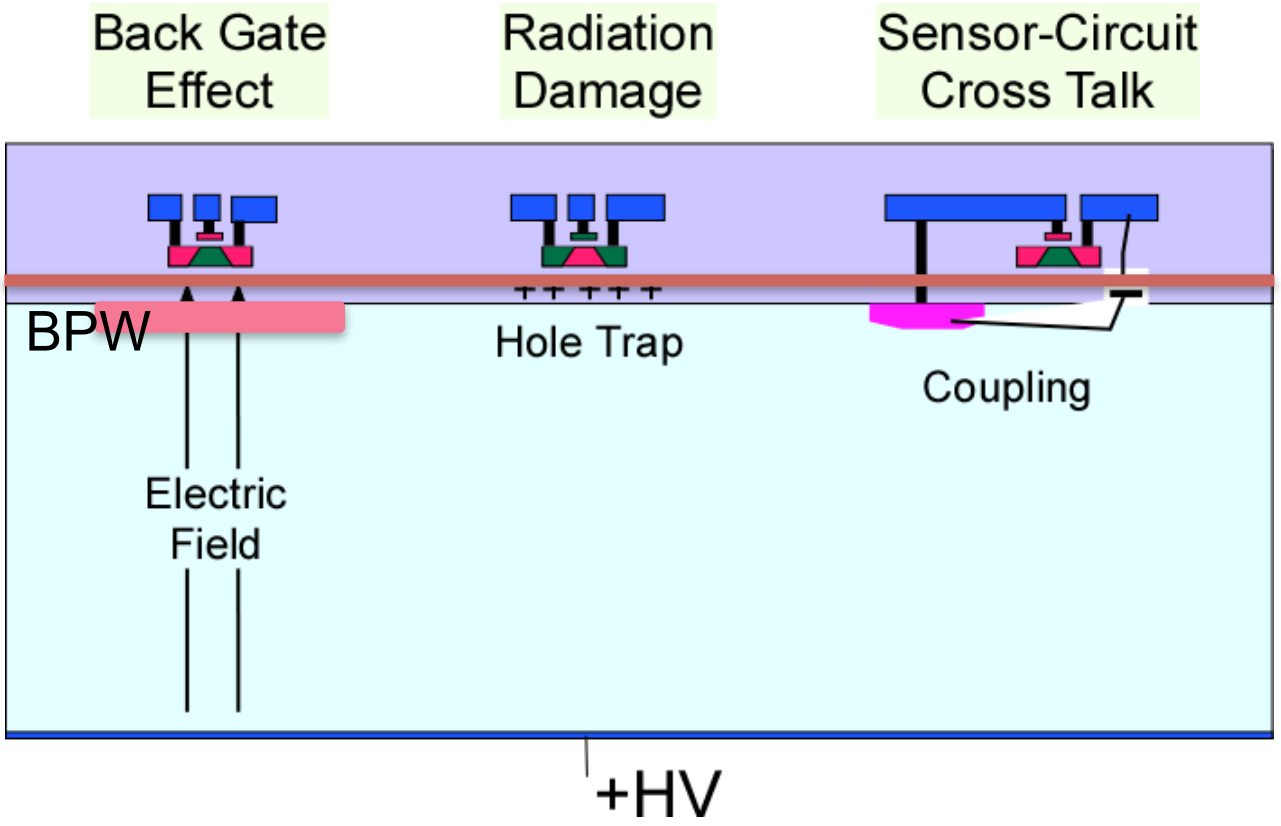
Lapis (OKI) semiconductor – Powerchip Tech. – KEK

SOI Process

- General Manager of Device Technology Development Div. in OKI
- 30 Years of CMOS Process Development (1.8um – 30nm)
- Involved in SOI Pixel Development while in OKI.

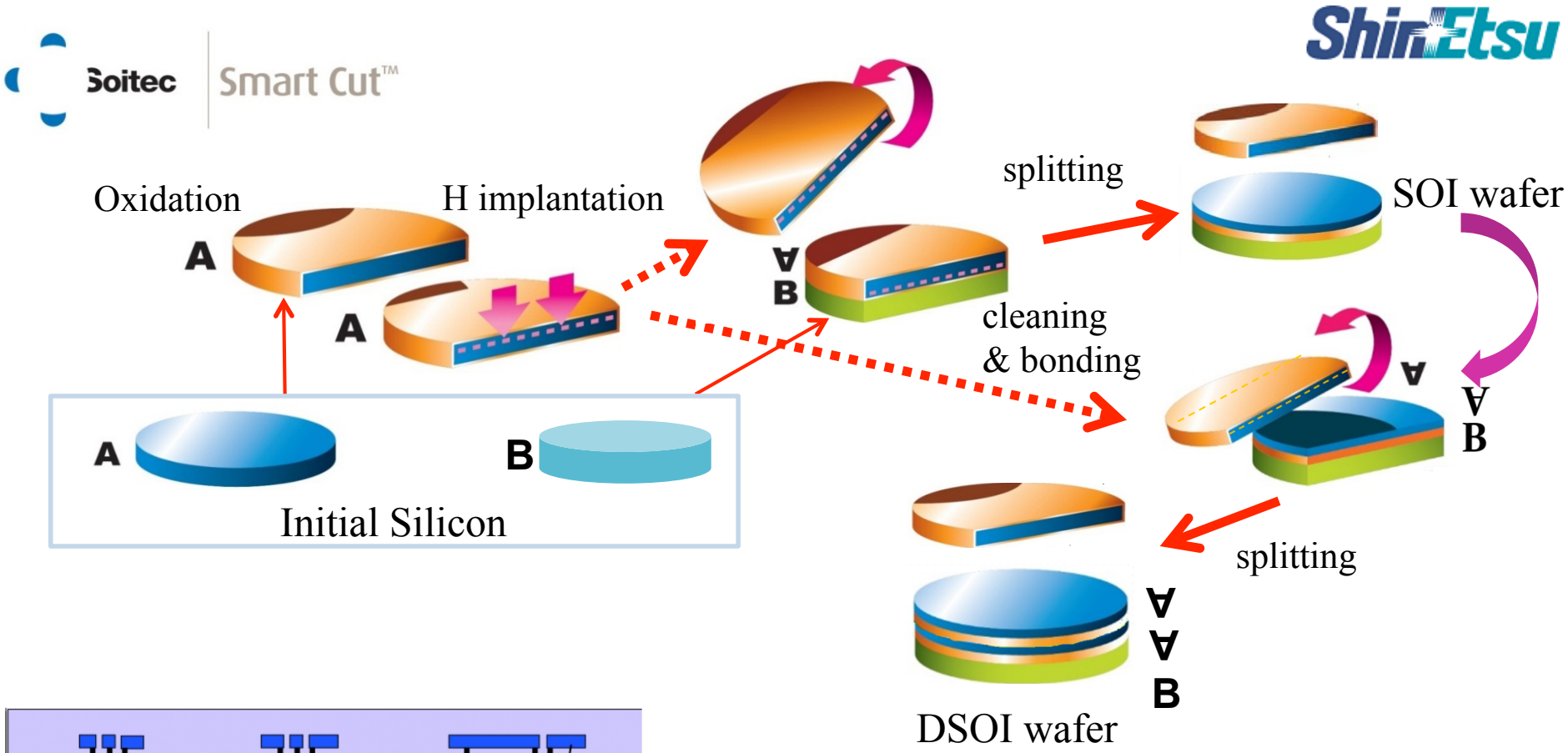

Imaging of Elementary Particle
Origin of Mass by Higgs Particle
micron Accuracy
2mm
killifish
脳
眼
エラ
1 mm
Imaging Mass
Spectrometer
Rapid Analysis
128x128(目標)
1.8K Operation
Far Infra Red
Evolution of Stars
Harsh
Environment
Superior
Resolution
X-ray
Imaging
Synchrotron
Radiation
3D Structure
of a Cell
SOI
High Intensity
Precise Time
Resolution
Au Nano Particle
Δx = ~10 nm
100 nm
XFEL
femto Second
1nm Resolution
Exploration of
Primitive Black
Holes
SOIPIX(目標)
Distant X-ray
Background
Reduction

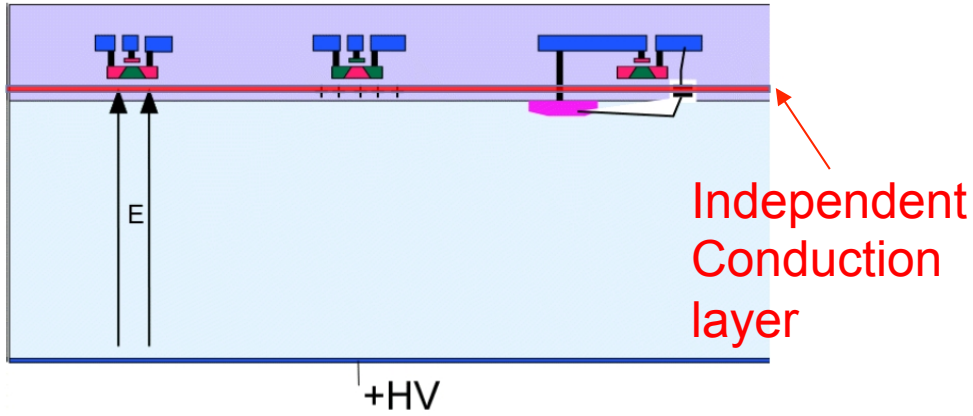
III. Double SOI

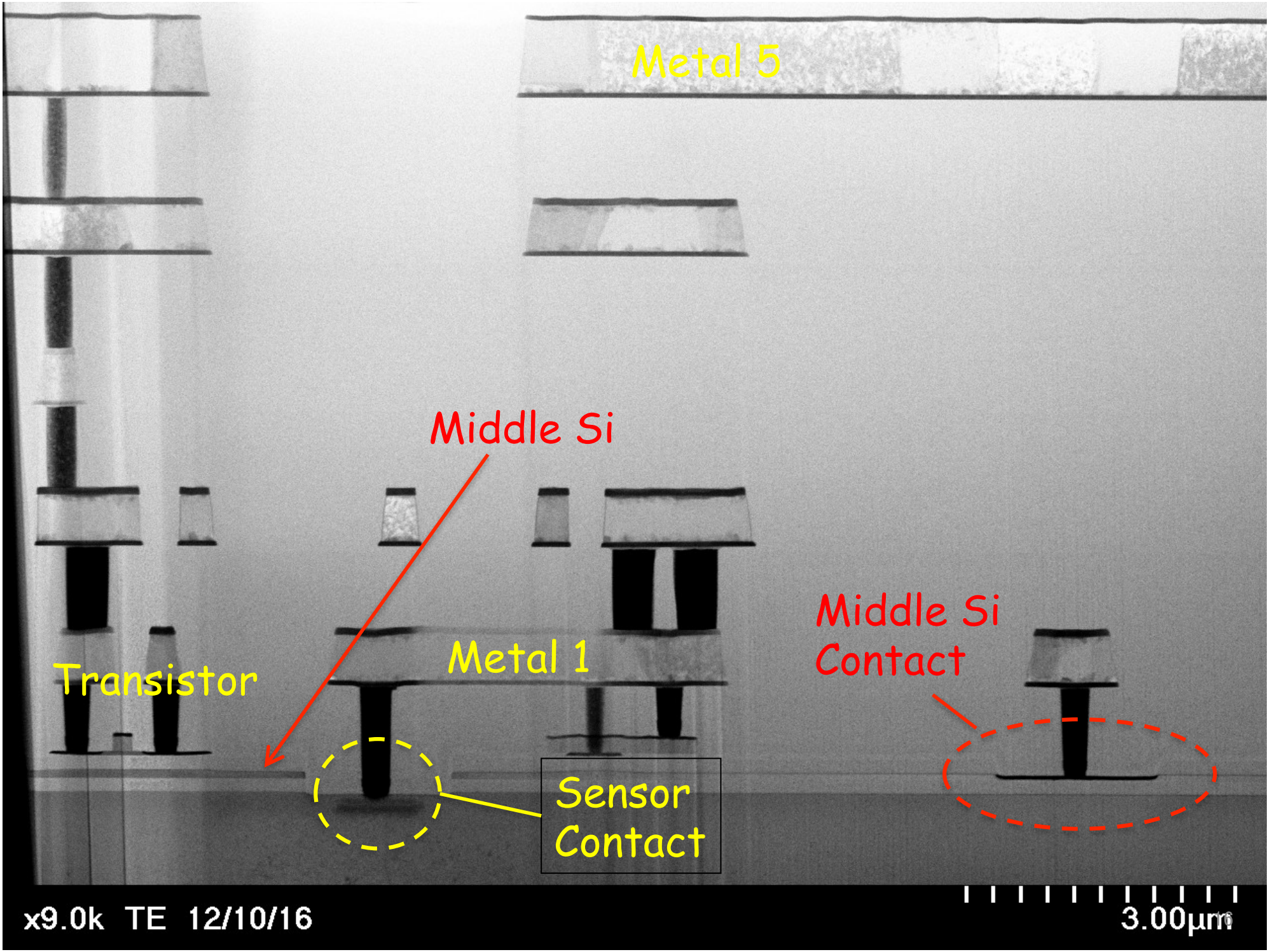


- shield the back gate effect
- compensate effect of box charge
- shield the sensor to circuit crosstalk

Double SOI Wafer

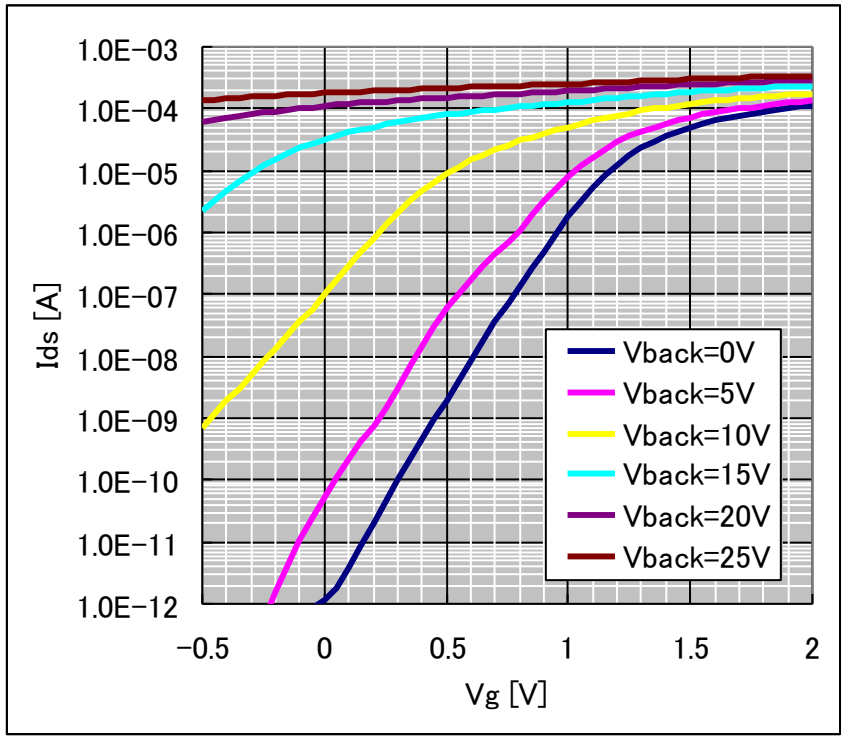




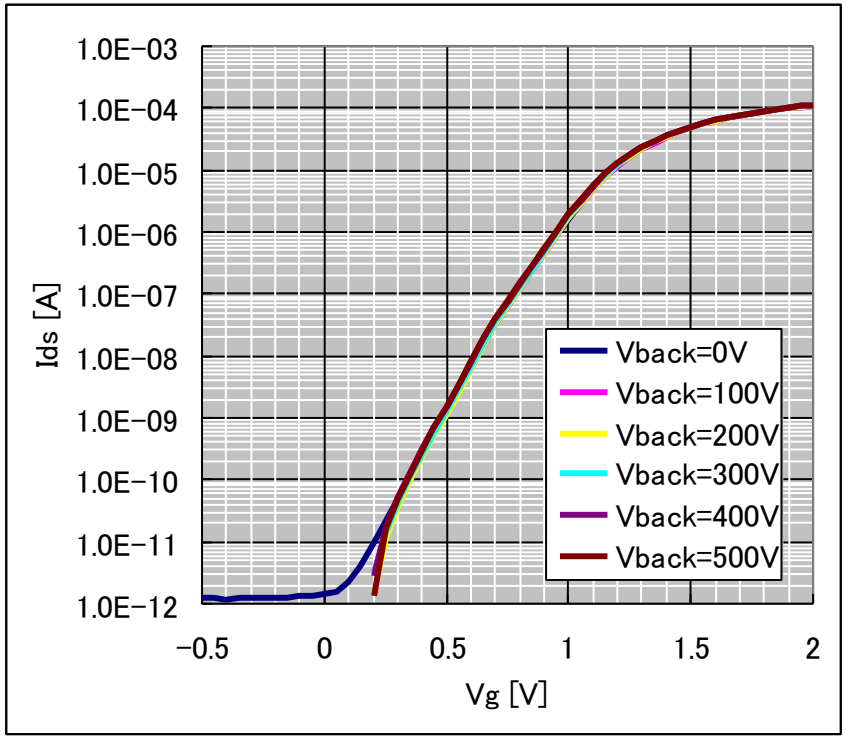

Metal 5
Middle Si
Transistor
Metal 1
Middle Si
Contact
Sensor
Contact
x9.0k TE 12/10/16
3.00µm

Suppression of Back-Gate Effect with Middle-Si layer

a) Middls-Si Floating



b) Middle-Si = GND



Back-Gate effect is fully suppressed with the Middle Si Layer having fixed voltage.

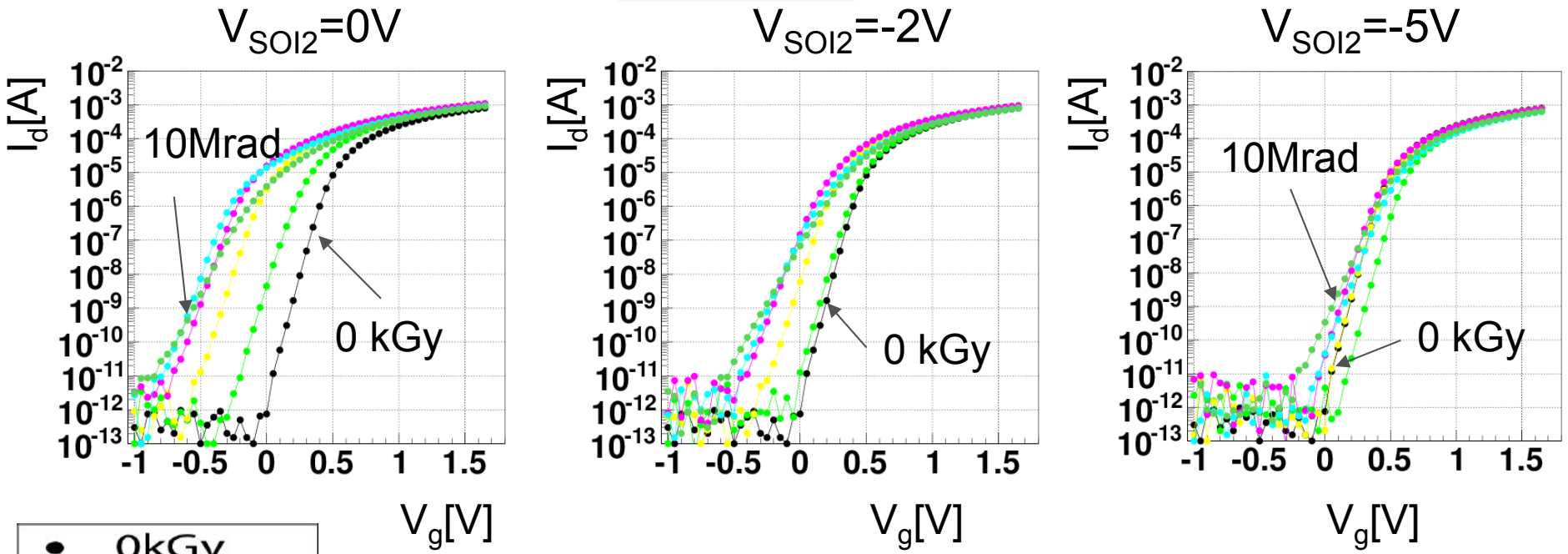
Nch Core Normal-Vt
L / W = 0.2 / 5.0um
Vd=0.1V

Free to select BPW size without annoying the Back-Gate effect.

Gamma-ray Irradiation Test
(Id-Vg Characteristics v.s. SOI2 Potential)

I/O normal Vth
Source-Tie Tr.
L/W =0.35um/5um

NMOS

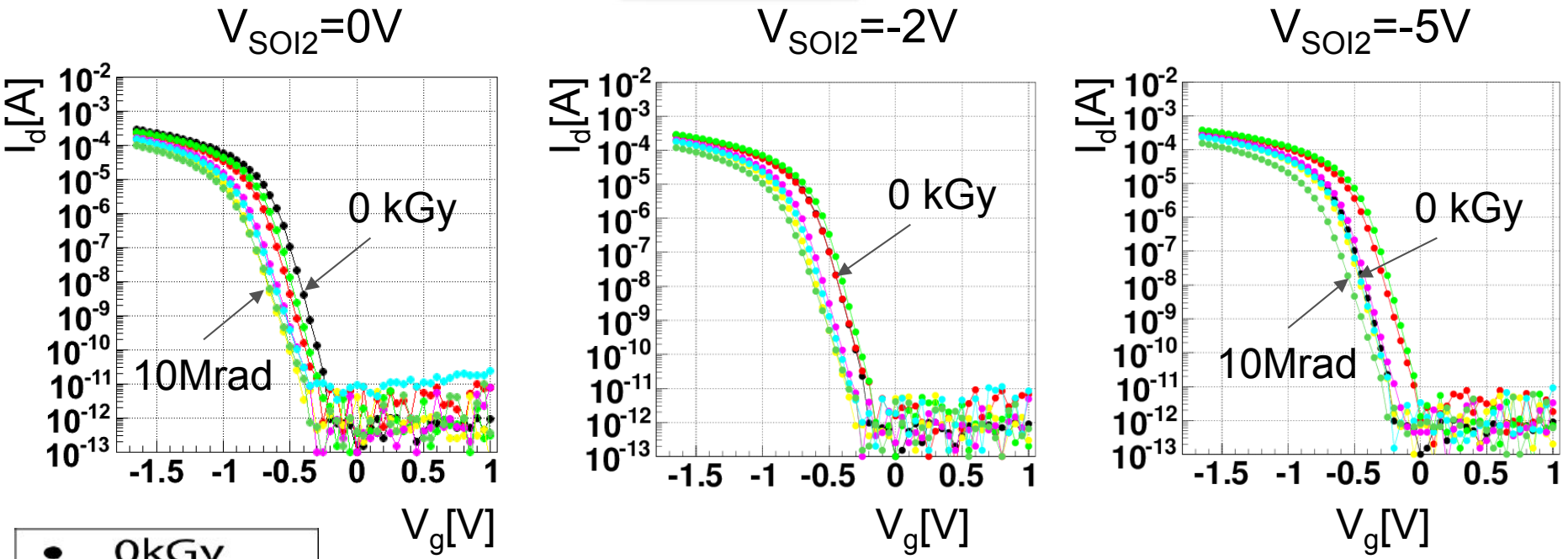


By setting Vsoi2 ~ -5V, Id-Vg curve returned nearly to pre-irradiation value.

Variation of Id-Vg Characteristics and Effect of SOI2 Potential

I/O Normal Vt
Source-Tie
L/W =0.35um/5um

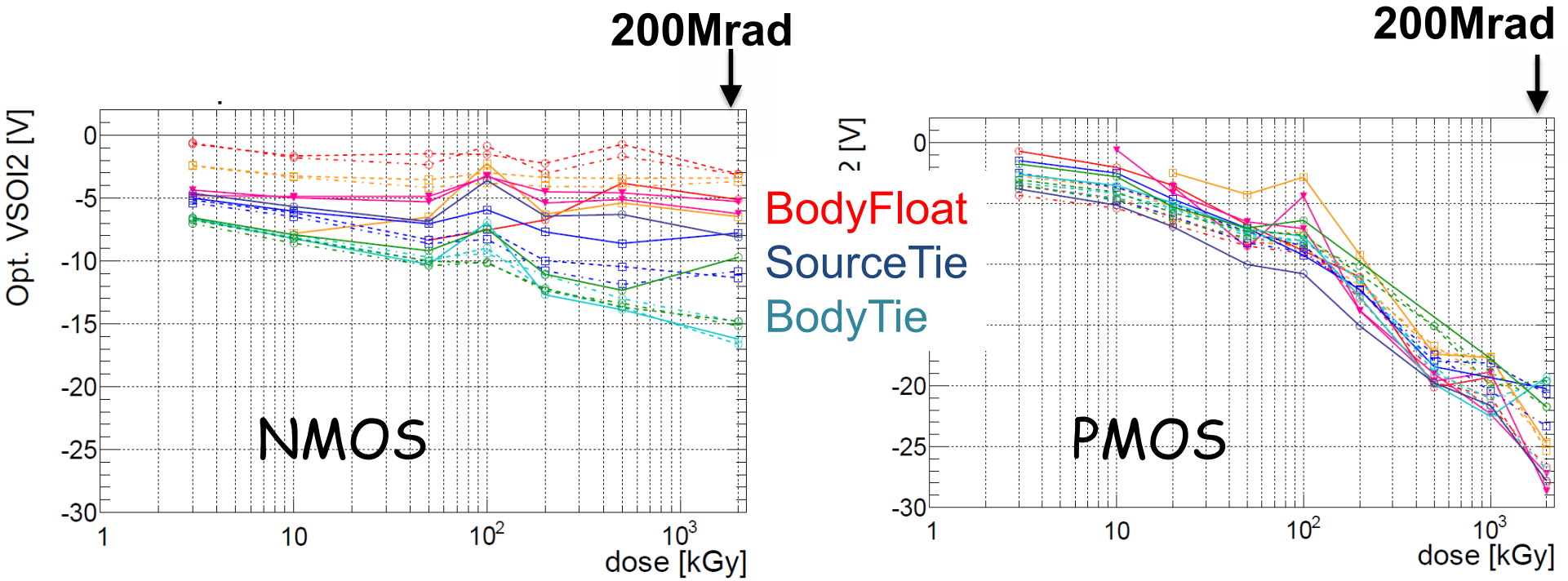
PMOS



The V_{SOI2} effect to PMOS is not so large compared to NMOS case.
Id-Vg curve also returned to pre-irradiation value @VSOI2~-5V.

Optimum V_{SOI2} for V_{th} compensation

V_{SOI2} to compensate for Vth to back to pre-irradiation

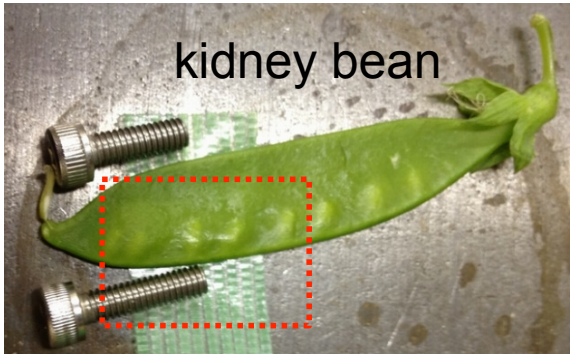


Noticeable differences are observed among various transistor types.

➔Different V_{SOI2} settings might be preferred to compensate fully the TID for NMOS, PMOS and each body connections.

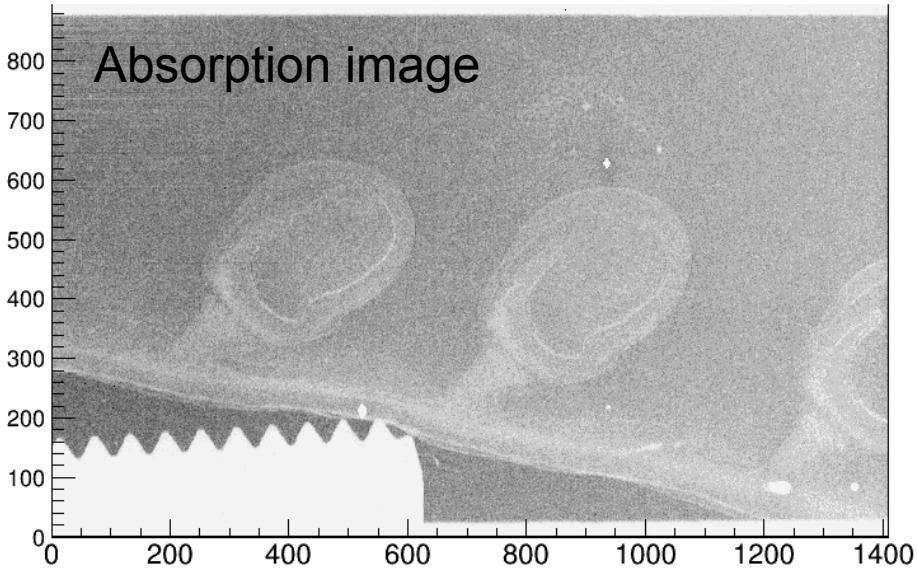
S. Honda, TPP2014

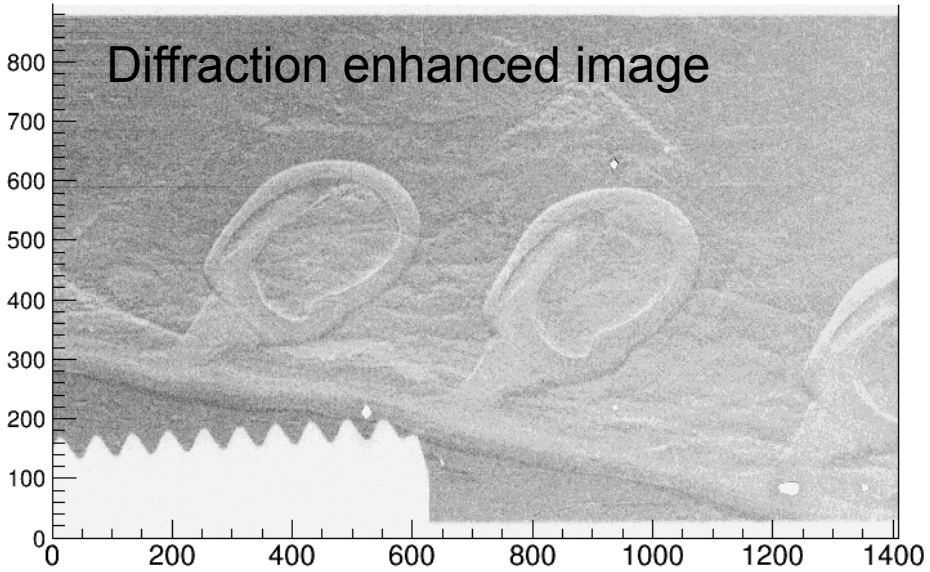
IV. New Developments



- 3D Vertical Integration
- Ultra Low Temperature
- *Damage Refresh*
- *New Sensor Structure*
- *New Device*

Some of the results are very preliminary!

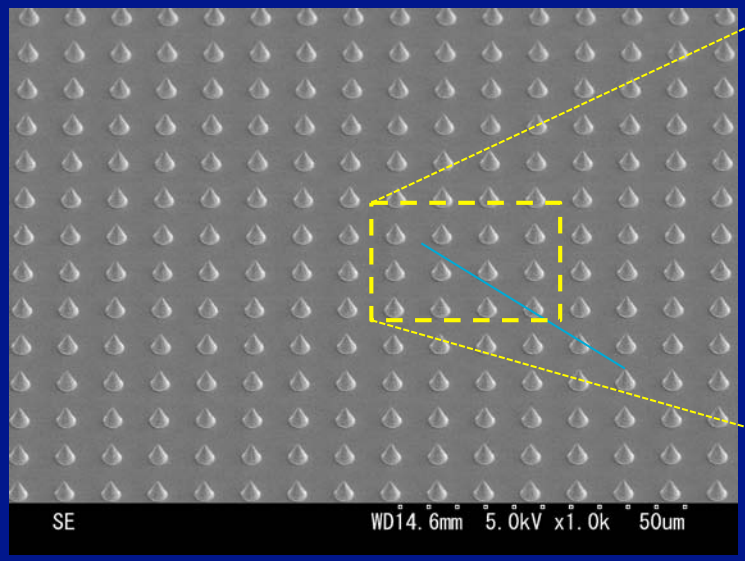


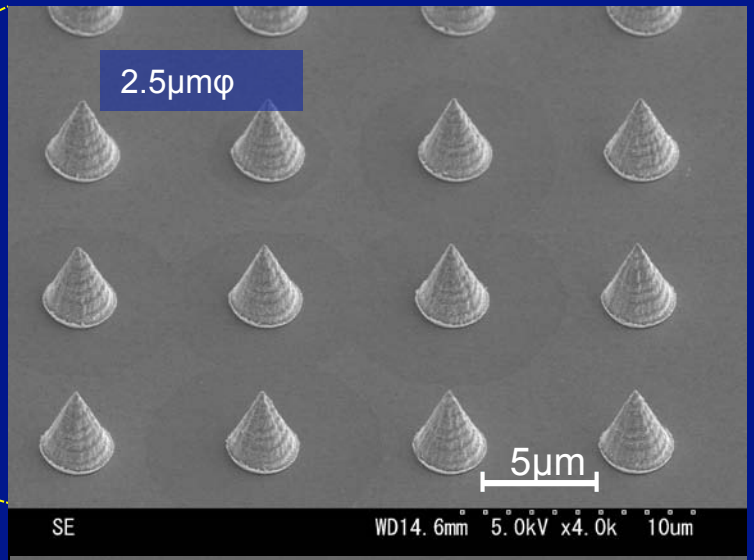


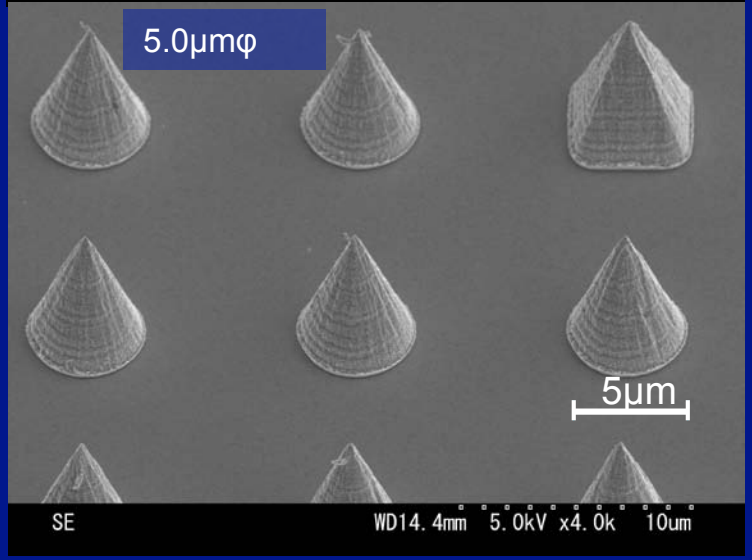
FZn-INTPIX5 $(12um)^2$ pixel

T-Micro

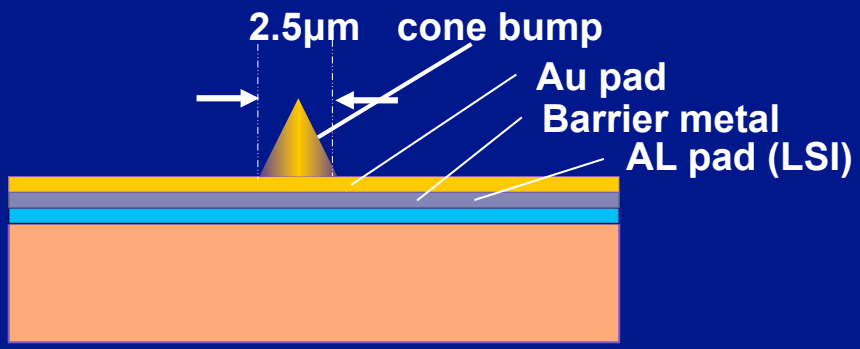
2.5/5.0μmφ Au Cone Bump



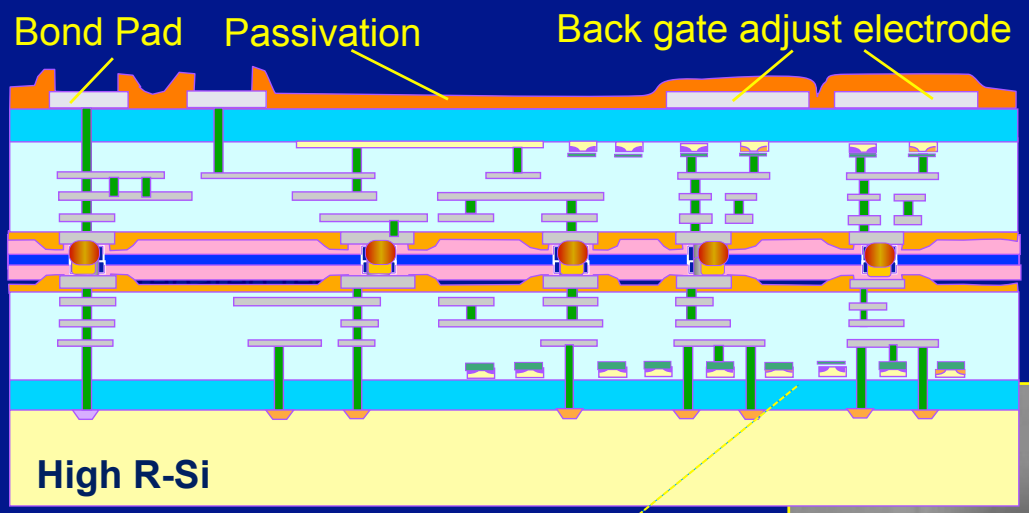


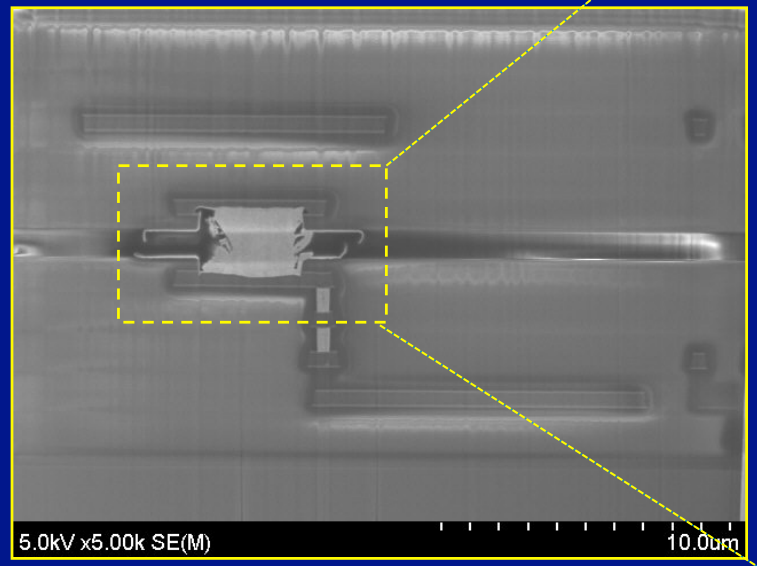


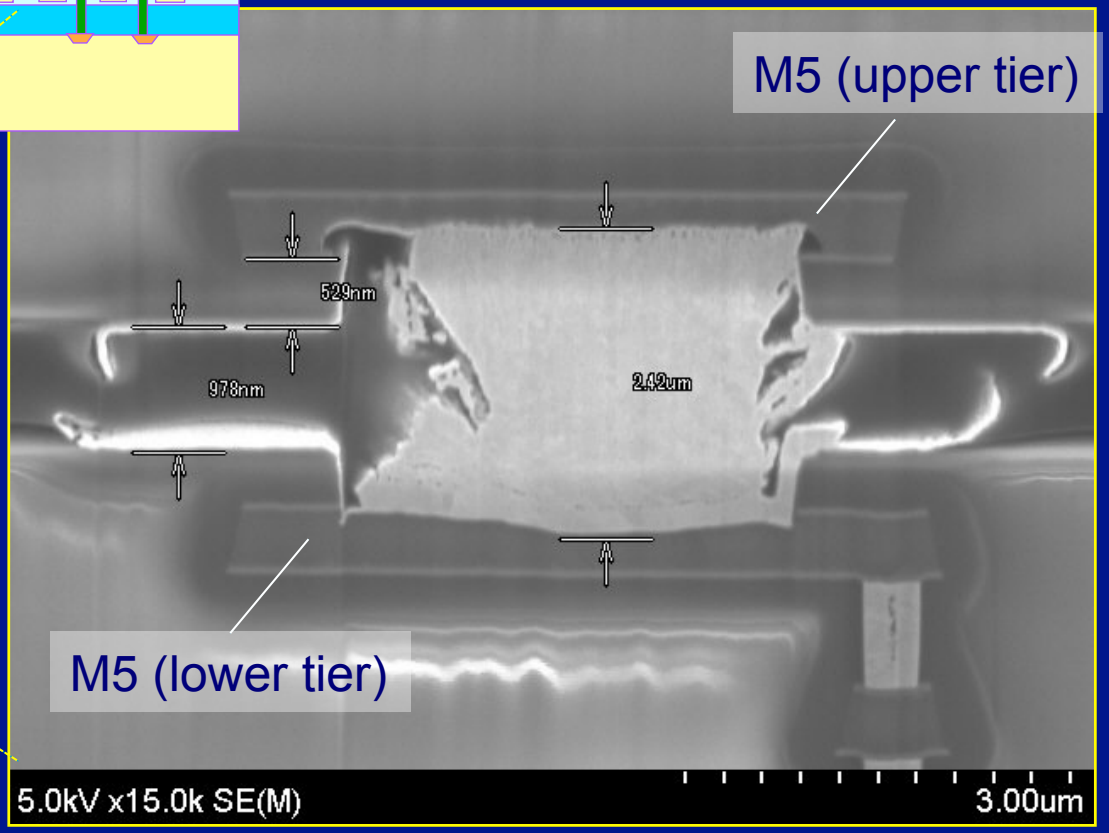
TEG cross section



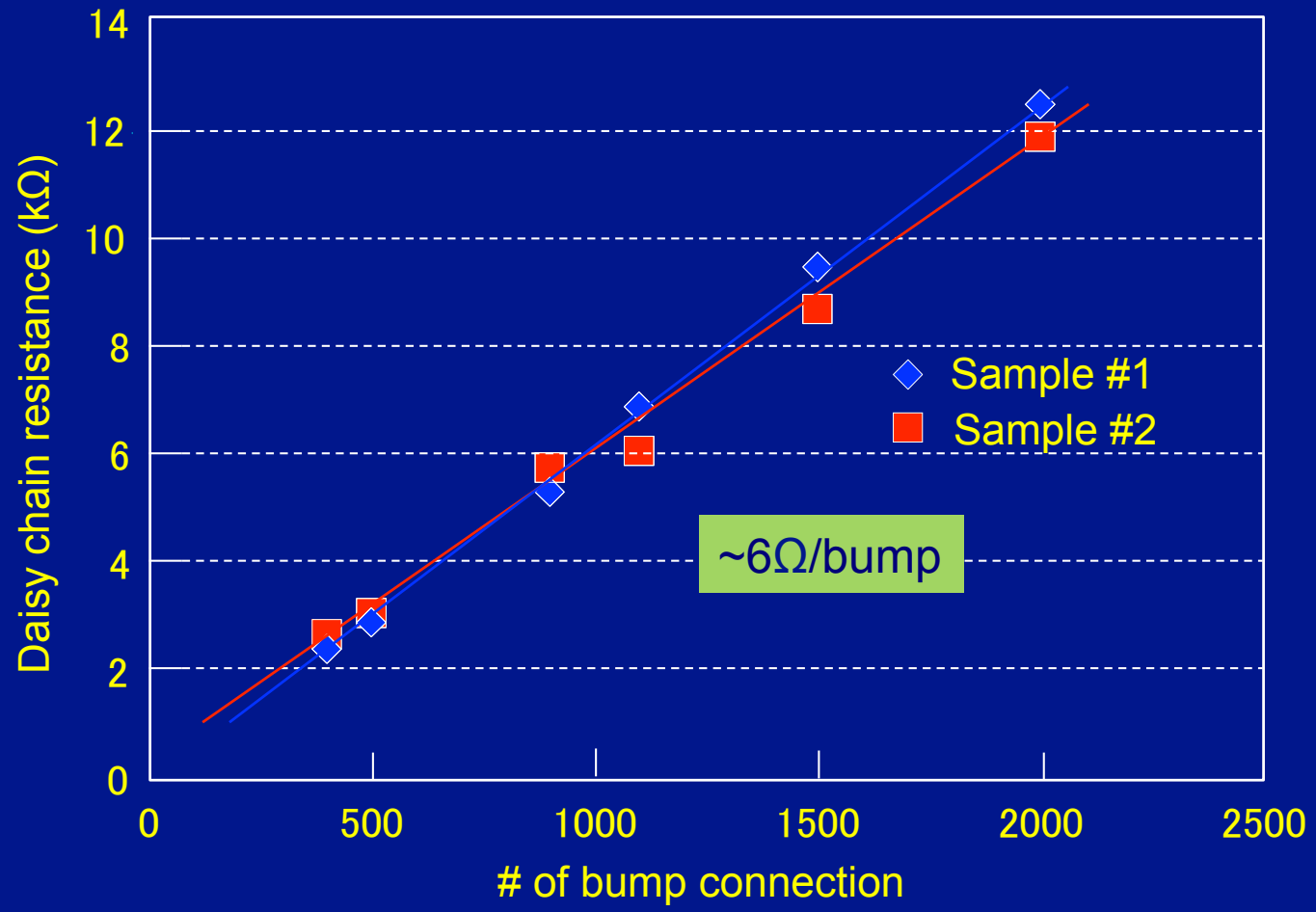
Cross section of Au cone bump junction







Daisy Chain Resistance



Ref. ～5Ω by 4 terminal resistance

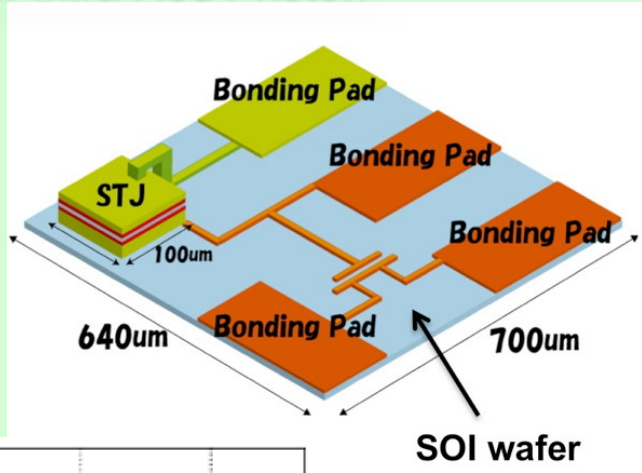
Ultra Low Temperature Electronics:

STJ (Superconducting Tunnel Junction) on SOI

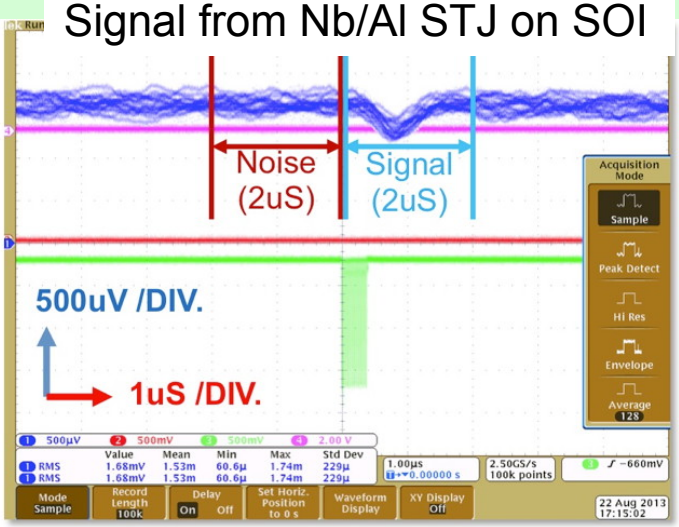
Tsukuba Univ. : Detection of Far Infra Red Photon

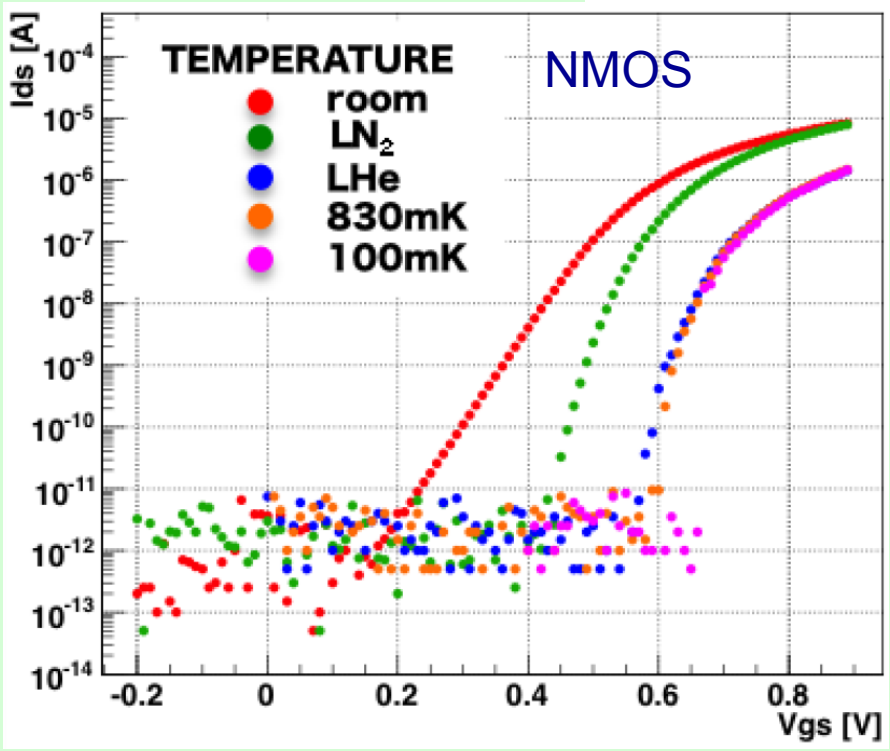
SOI Tr work at T < 1K.

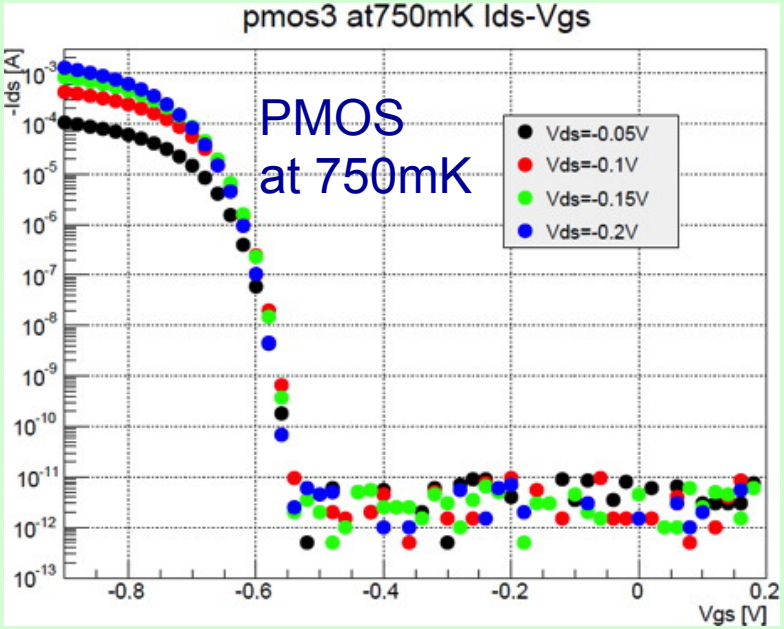
STJ sensors are fabricated on SOI for multiple channel readout.



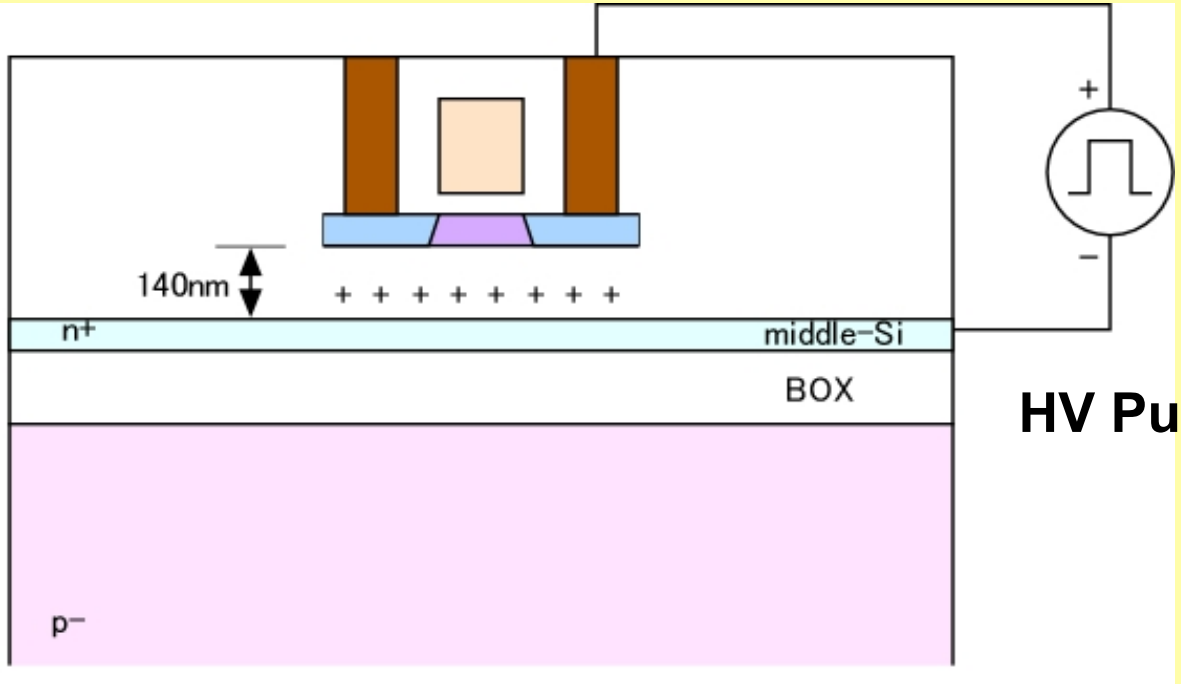
Signal from Nb/Al STJ on SOI



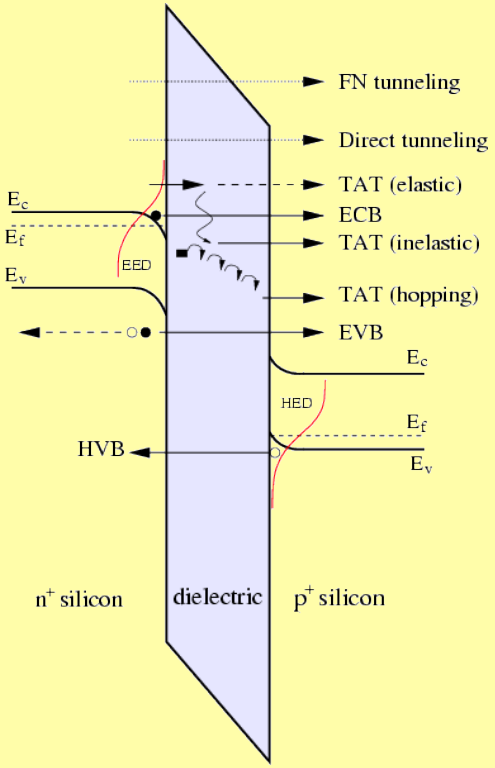




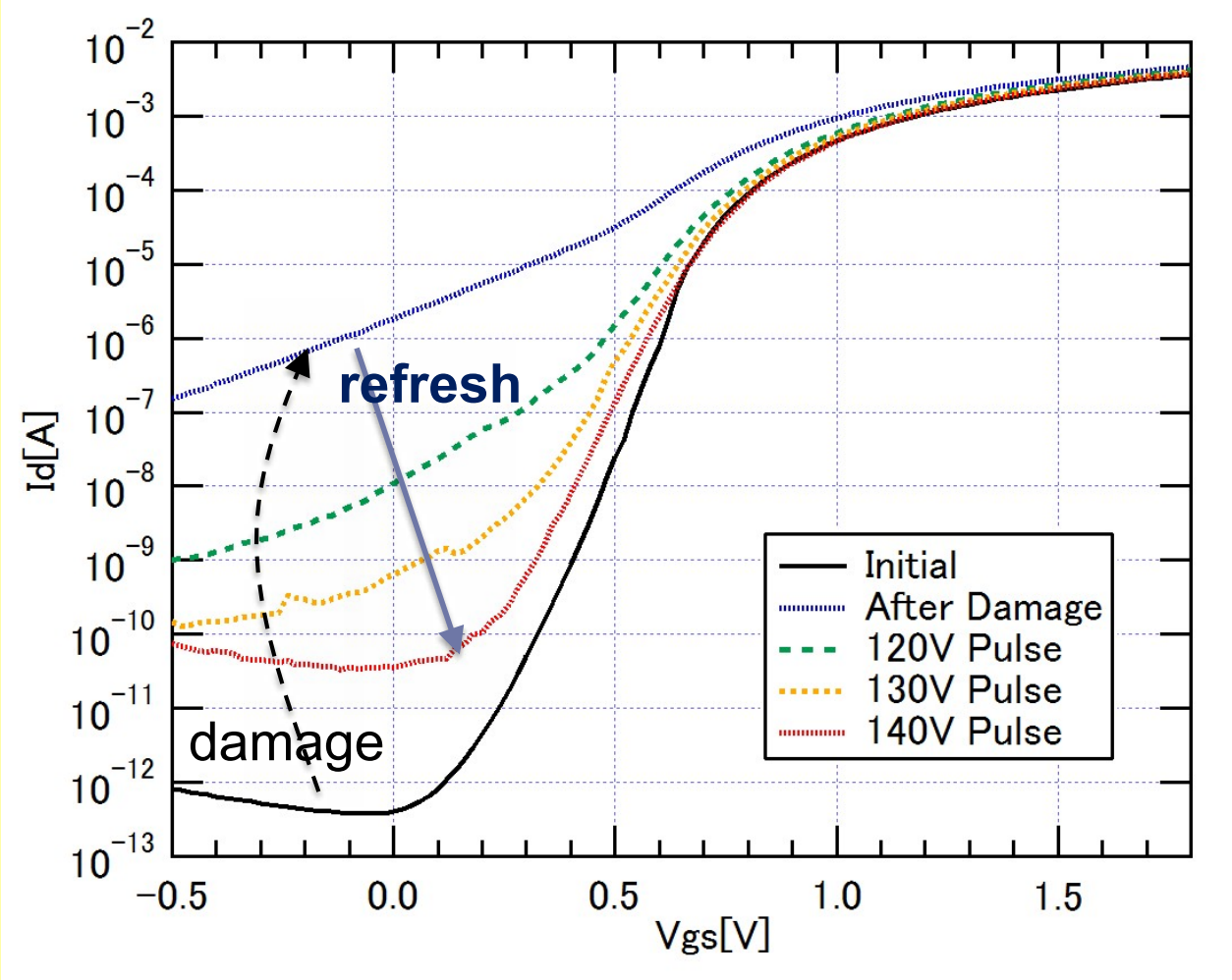
Refresh by using middle SOI2 layer



HV Pulse



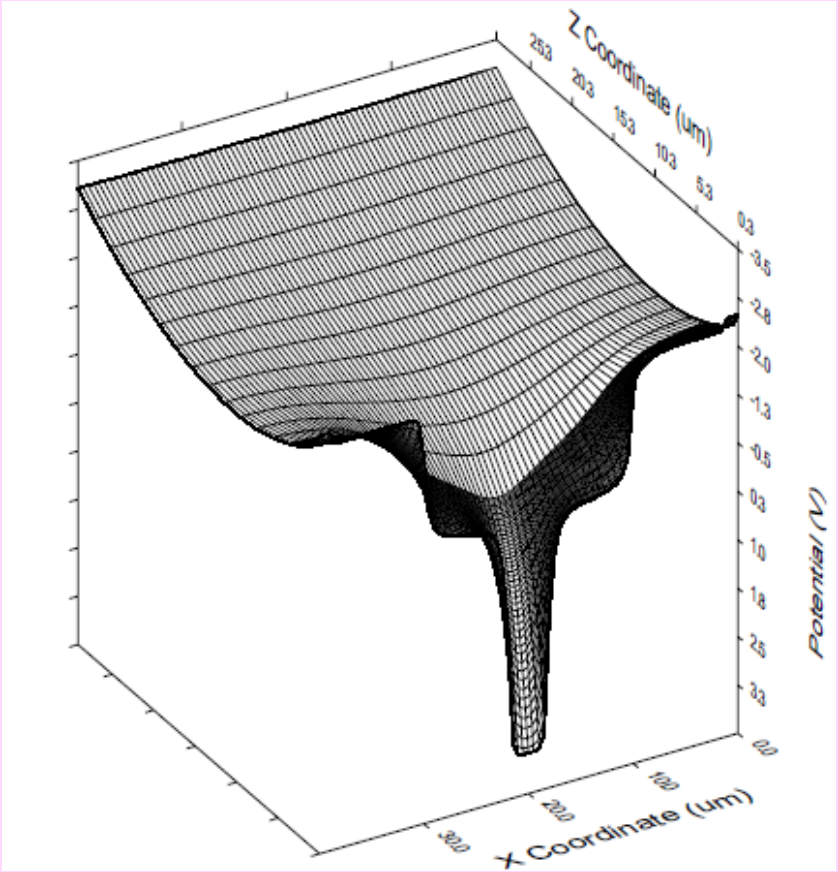
Preliminary!



We could observe refresh phenomena in SOI chip.
(in this test BPW layer in a single SOI is used instead of the middle SOI layer)

New Sensor Structures

Ex.) Charge Collection by field shape



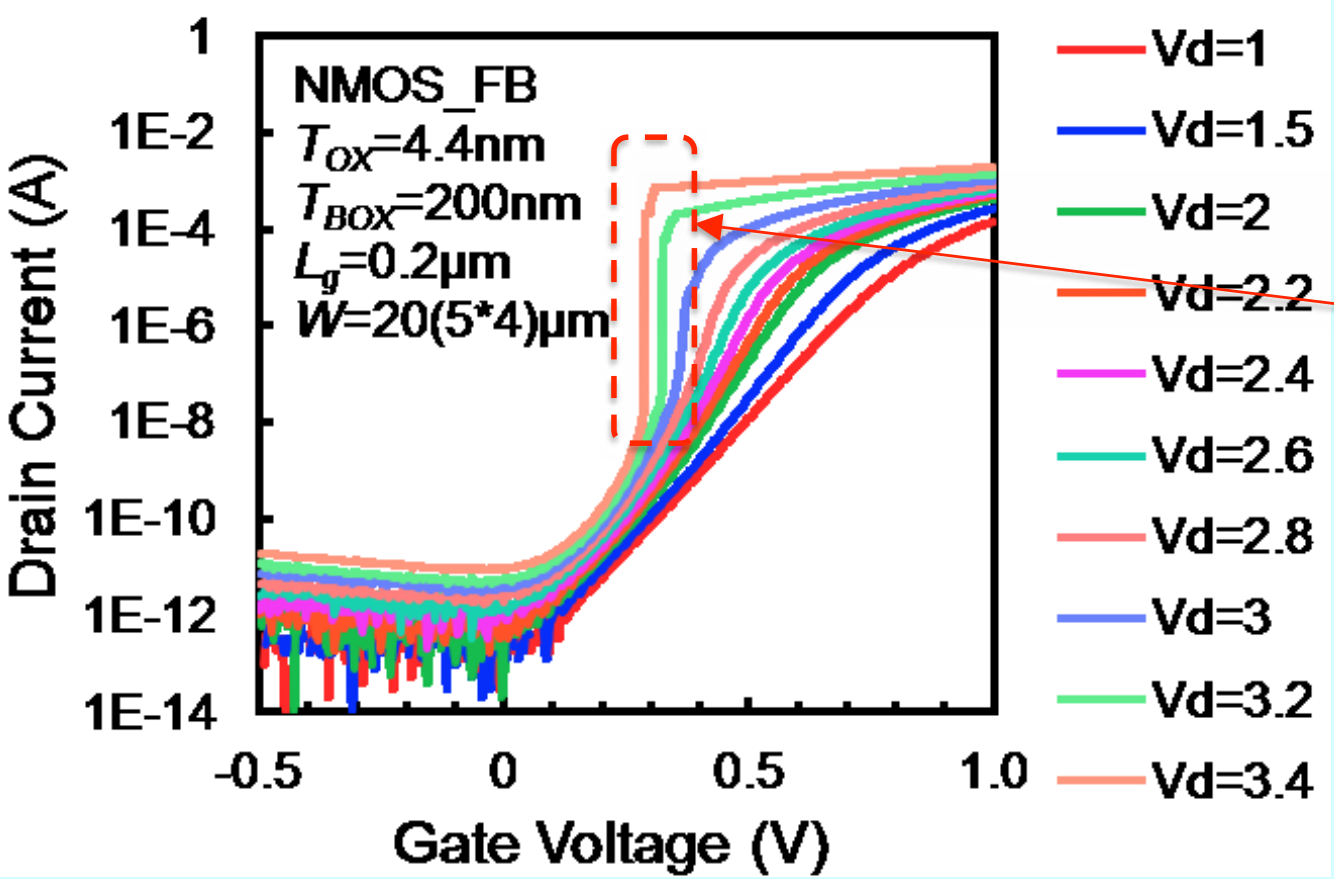
Preliminary!

- Deplete from Back Side
- Very Low Input Capacitance
- Lower Leakage current
- Better charge collection

Shizuoka Univ.

New Devices

Super-Steep Cut-Off Subthreshold-Slope Transistor



Preliminary!

S<1mV/dec

Kanazawa Univ.

T. Mori and J.Ida, IEEE S3S Conf. 2013, 6a.5 1-2pp

Summary

- SOIPIX R&D has entered new phase by including many new collaborators.
- We are keeping regular SOI MPW runs twice per year.
- Lots of new process technologies have been introduced or are under development:
  Stitching, many Implantation layers, High-resistive FZ-SOI wafer, Double SOI wafer, 3D Vertical integration …
  and various new sensor/device ideas.
- Many R&D Projects are going on not only in high-energy experiments but also in many other fields.

Thank You!

SPRiT

(SOI Portable Radiation image Terminal)

INTPIX4
832 x 512 pix
$(17um)^2$