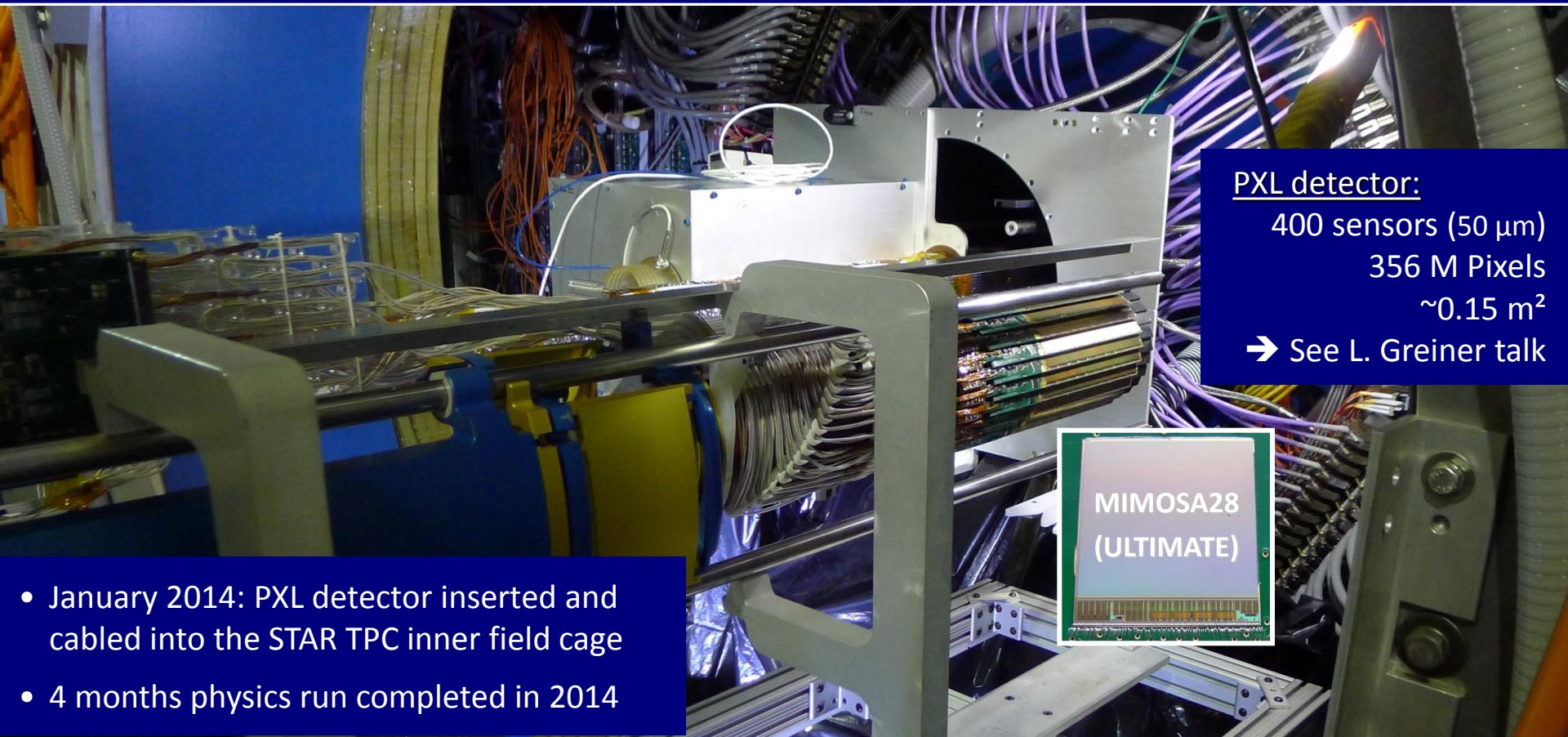
Design of CMOS Pixels Sensors for the STAR Experiment

Christine Hu-Guo (on behalf of the PICSEL team of IPHC-Strasbourg)



PXL detector:
400 sensors (50 µm)
356 M Pixels
~0.15 m²
➔ See L. Greiner talk

- January 2014: PXL detector inserted and cabled into the STAR TPC inner field cage
- 4 months physics run completed in 2014

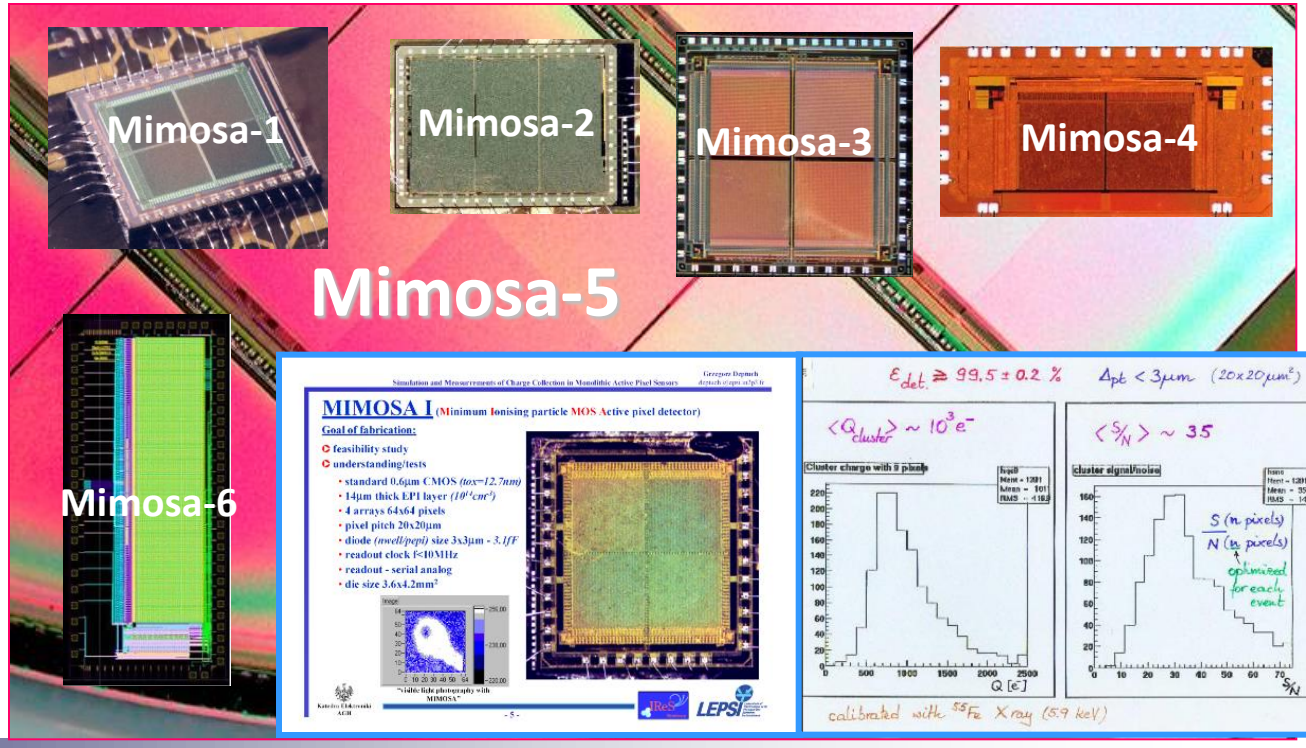
CPS (CMOS Pixel Sensors) Long Term R&D (1)

- *R&D activity of CPS initiated in 1999 for future subatomic physics experiments which express a growing need for very high performance flavor tagging*
  - *Physics constraints: high resolution, low material budget, swift readout and radtol were not achievable simultaneously by existing detectors at that time*
  - *At the beginning of the R&D, numerous simple demonstrators were designed*
    - ⋆ *To study critical parameters: CCE, S/N, ε_{det}, … in radiation environment*
      To find the optimum CMOS process for this new CPS technology
    - ➔ *Validate proof of detection concept*

- Assistant Prof. UDS (2001)
- CMOS Sensor Design group leader at RAL (UK)

- Leader of the PICSEL scientific group

- Ph.D student UDS (2002)
- ASIC development group leader at Fermilab (USA)



Long Term R&D (2)

- *R&D activity of CPS initiated in 1999 for future subatomic physics experiments*
- *First contact for STAR PXL took place in Year 2000 during the workshop Vertex-2000*

Long Term R&D (3)

- *R&D activity of CPS (CMOS Pixel Sensors) initiated in 1999 for future subatomic physics experiments*
- *First contact (H. Wieman & M. Winter) for STAR PXL in Year 2000 during Vertex-2000 workshop*
- *Three years later, the partnership between LBNL and IPHC became a reality thanks to the further discussion between H. Wieman & G. Deptuch, W. Dulinski, M. Winter*
- *First prototype in Year 2004 ➔ Final Sensor fabrication in Years 2011, 2013*

➔ *STAR PXL sensor R&D allows tracing back the evolution of CPS*

- *At the beginning of the development, there were no roadmap, no defined architecture, …*
- *Physics constraints:*
  - *Detection efficiency > 99.5%, space resolution < 10 µm*
  - *Material budget: the goal ~0.3% X_o/layer ➔ air cooling ➔ low power consumption*
  - *Radiation load: 150 kRad/yr & few 10^{12} N_{eq} /cm² /yr*
  - *Hit density ~ $2.4x10^5$ hits/cm²/s*
- ***Available budget marginally adapted to commercial CMOS processes (no specific R&D)***
  - *Mitigates the intrinsic detection performance*
- *Sensor R&D may be classified into 3 periods: Early-, Mid- and Mature stages*
  - *Corresponding to 3 generations of CMOS pixel sensors*
  - *Sensor specifications progress with CPS development & CMOS technology evolution*

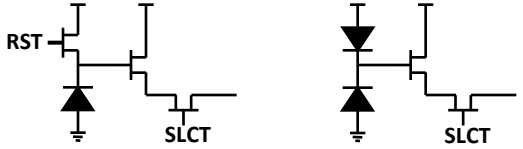
Early-Stage of CPS Development: … - 2006 (1)

- *Choosing an "optimum" CMOS process for detector running in radiation environment*
- *Optimising sensing elements*

} ***Accurate models not available for simulation tool !***

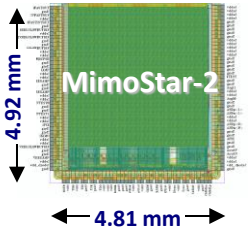
Typical RO chain

- *Study of CCE, S/N, Noise ~ f (Type, layout & dim. of diode, No. of diodes / pixel, Pixel pitches;…)*
- *Study of radiation tolerance by using special layout: removing thick oxide surrounding N-well diode by replacing with thin-oxide*
  - ★ *3T or 2T pixels*
  - ★ *Rolling shutter analogue readout*



- *First prototypes for PXL: 2T pixels, multiplexed analogue output RO*
  - *MimoStar-1 (Mimosa-10, TSMC 0.25, 2004) & MimoStar-2 (Mimosa-14, AMS 0.35 opto, 2005)*
    - ★ *2007: A MimoSTAR-2 sensors based telescope was constructed by LBL and performed measurements inside STAR detector environment*

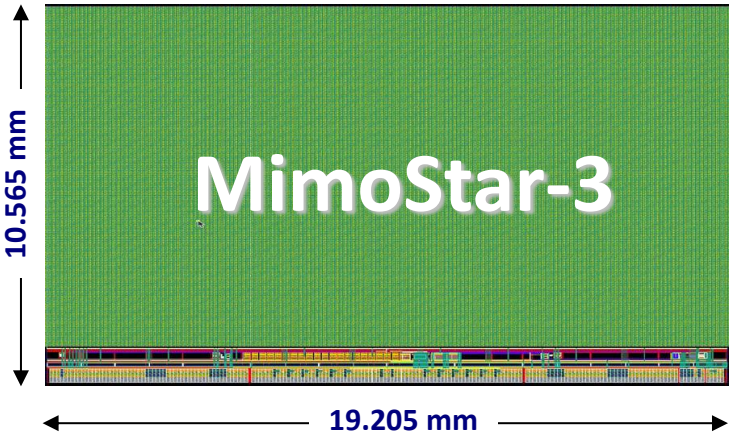
➔ *Validate CPS detector concept for STAR PXL*



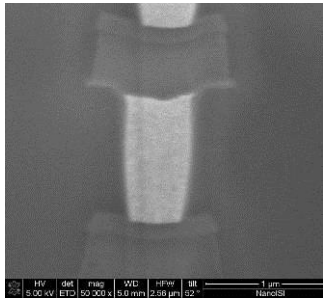
Early-Stage of CPS Development: … - 2006 (2)

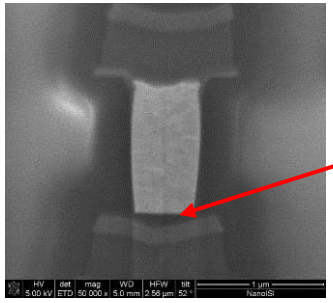
- *Half-reticule sensor: MimoStar-3 (Mimosa-20, AMS 0.35 opto, 2006) to validate yield performances*
  - *Pixel array: 640 x 320, 30 µm pixel pitches (~2x1 cm²)*
  - *~2 ms integration time ➔ 4 ms for full reticule sensor*
  - *2 serial output links at 50 MHz*

➔ ***Finding suitable CMOS process: AMS 0.35 µm opto***

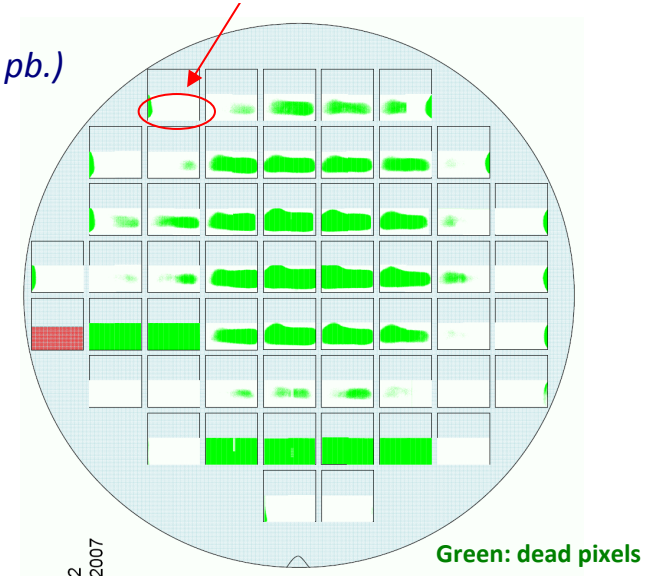


- *Scaling from small prototype to half-reticule size sensor was not straightforward*
  - *Initial yield was 10-20 %*
  - *Fault analysis by LBL: Problem with incomplete via contacts in the middle of wafer (some features of our design may be the origin of the pb.)*


Periphery of wafer


Centre of wafer

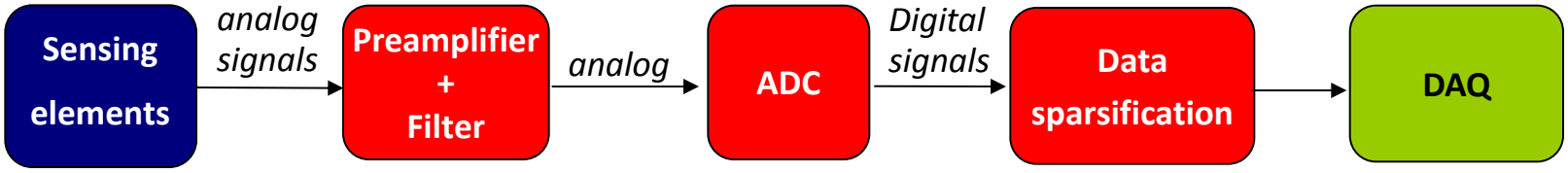
Gap between via and metal layer



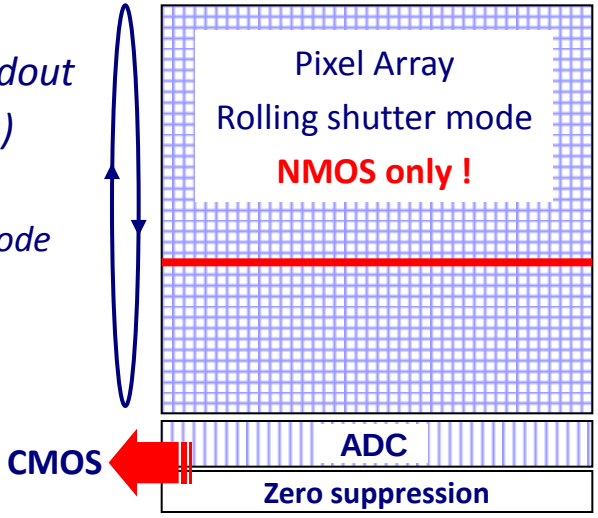
➔ *Solved by adjustments in the fabrication process*

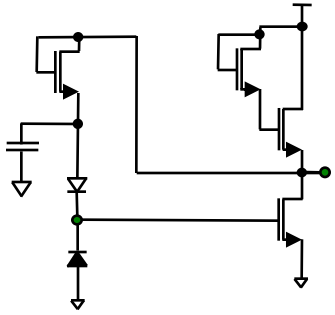
- *Weaknesses of the 1st generation analogue output sensor:*
  - *Long integration time (4 ms, was complying with initial requirement): events pile-up*
  - *Cross talk between analogue channels in a flex cable*

Mid-stage of CPS Development: 2003 - 2008 (1)



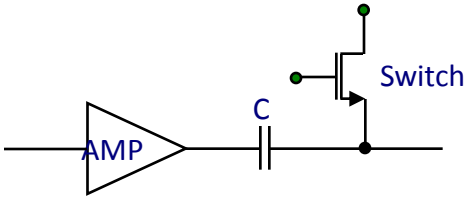
- *Development of RO architecture: rolling shutter column parallel readout with integrated zero suppression logic (in a twin-well CMOS process)*
  - *NMOS only in pixel array. Because any additional N-well used to host PMOS would compete for charge collection with the sensing N-well diode*
- *Development of on-sensor signal processing blocks*
  - *Increasing S/N at pixel-level (coll. with Irfu/Saclay)*
    - ⋆ *In-pixel amplification*





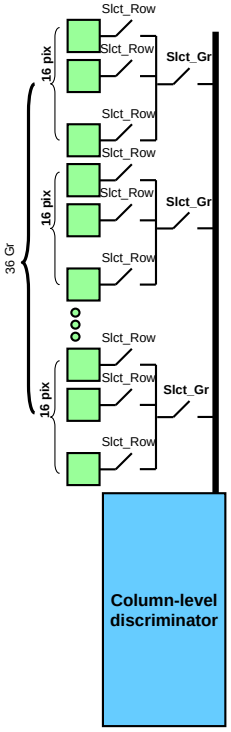
Feedback ➔ decrease gain dispersion due to process variations and after irradiation

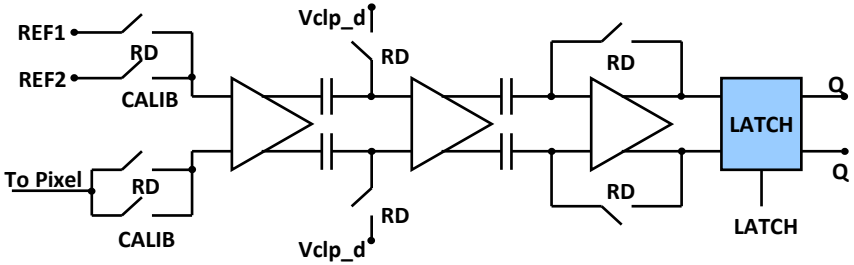
- ⋆ *In-pixel CDS: clamping technique*
  - ✓ *Realised by 1 capacitor + 1 NMOS switch*
  - ✓ *Need 2 phases to perform cDS*



Mid-stage of CPS Development: 2003 - 2008 (2)

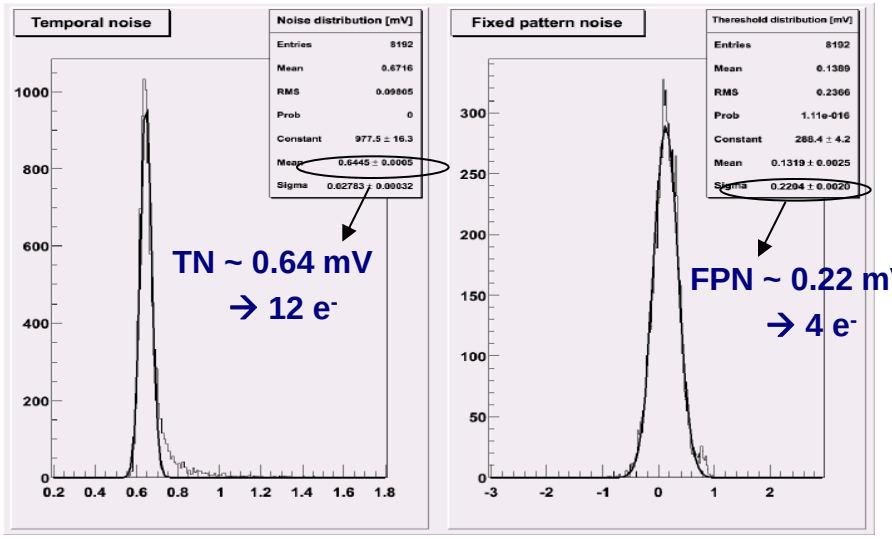
- *A to D Conversion at end of column*
  - ★ *For STAR PXL detector, considering the resolution requirement (10 µm), 1 bit ADC was sufficient*
  - ➔ *1 discriminator ending each column (Y. Degerly. Irfu/Saclay)*
  - ★ *Small input signal ➔ Offset compensated amplifier stage followed by a latch*

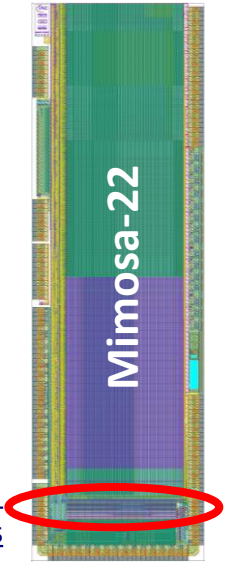




Prototypes: *Mimosa-8 (TSMC, 2003), Mimosa-16 (AMS, 2006), Mimosa-22 (AMS, 2007-8)*

- ✓ *Pixel array ended with discriminators*



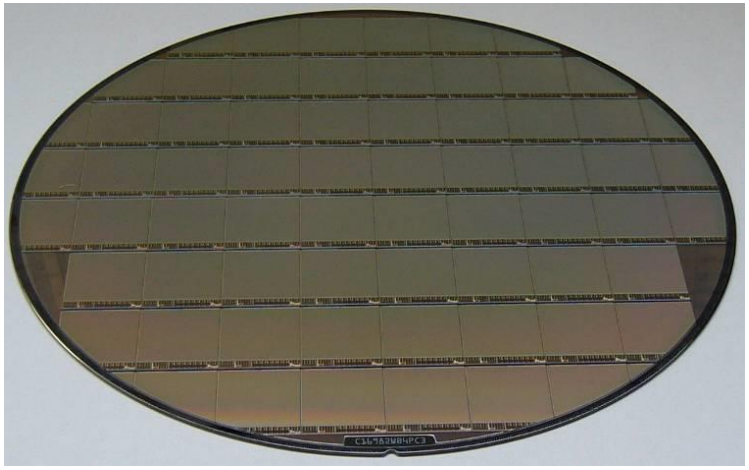


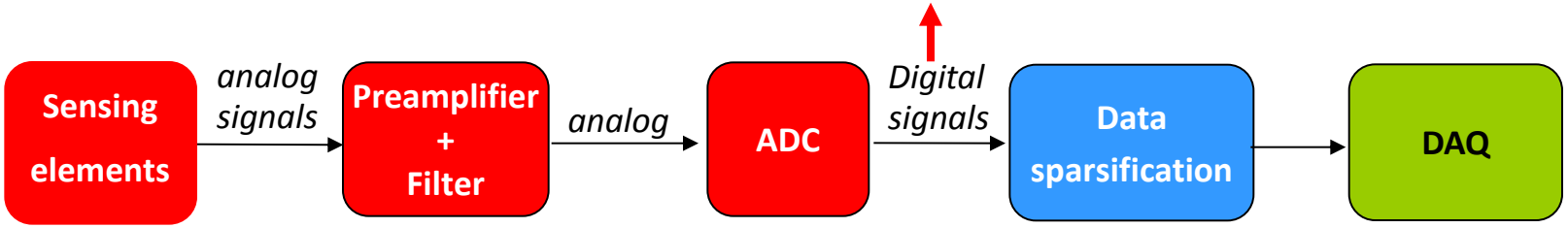
128 end-of-column discriminators

➔ *1st feasibility study of the rolling shutter column-parallel readout architecture*

Mid-stage of CPS Development: 2003 - 2008 (3)

- *Validation of the rolling shutter column parallel readout architecture*
  - ➔ *Scaling from Mimosa-22 to PHASE-1 (Mimosa-23 2008) ➔ 2nd generation of STAR PXL sensor*
    - ★ *Reticle size (1.952 x 2.112 cm²)*
    - ★ *Pixel pitch 30 µm*
    - ★ *640 x 640 pixels ➔ ~ 410 k pixels*
    - ★ *Column parallel readout*
    - ★ *End-of-column discriminators*
    - ★ *Binary readout of all pixels*
    - ★ *Data multiplexed onto 4 $LVDS_{TX}$ @ 160 MHz*
    - ★ ***Integration time 640 µs***

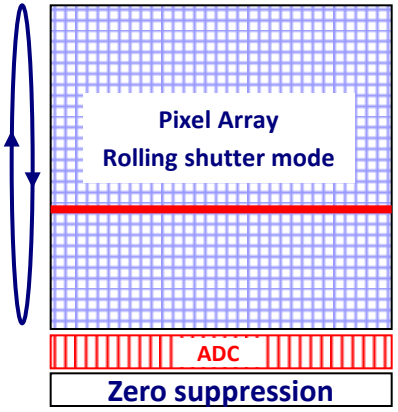


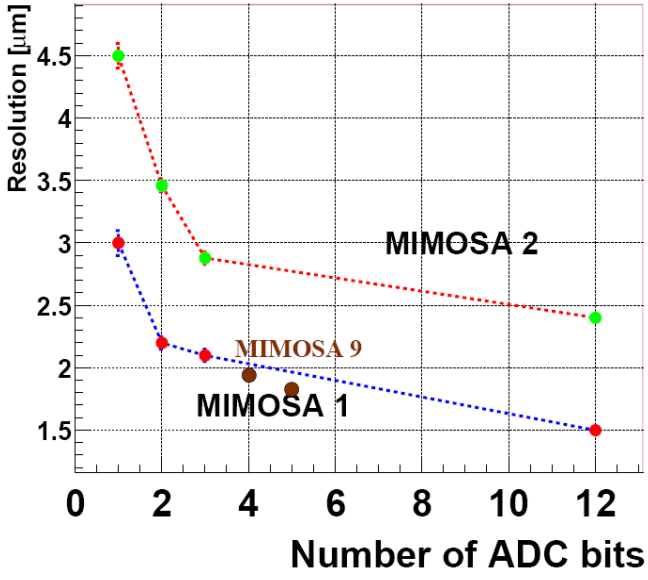


- *Gain confidence to achieve next design sensor with massive parallel discriminators*
  - ↳ *Lesson learned with 640 discriminators with not sufficient uniformity*
    - ★ *Discriminators timing optimisation*
    - ★ *Group division with adjustable reference voltages per group to compensate process dispersions over 2 cm long*

Mid-stage of CPS Development: 2003 - 2008 (4)

- *A to D Conversion at end of column*
  - ★ ***For ILC**, 3-5 bit ADCs (Wilkinson, SAR, pipeline, flash or mixed …) at end-of-column were developed simultaneously with end-of-column discriminators*
    - ✓ *Potentially replacing end-of-column discriminators ➔ to increase spatial resolution while maintaining or reducing power consumption*



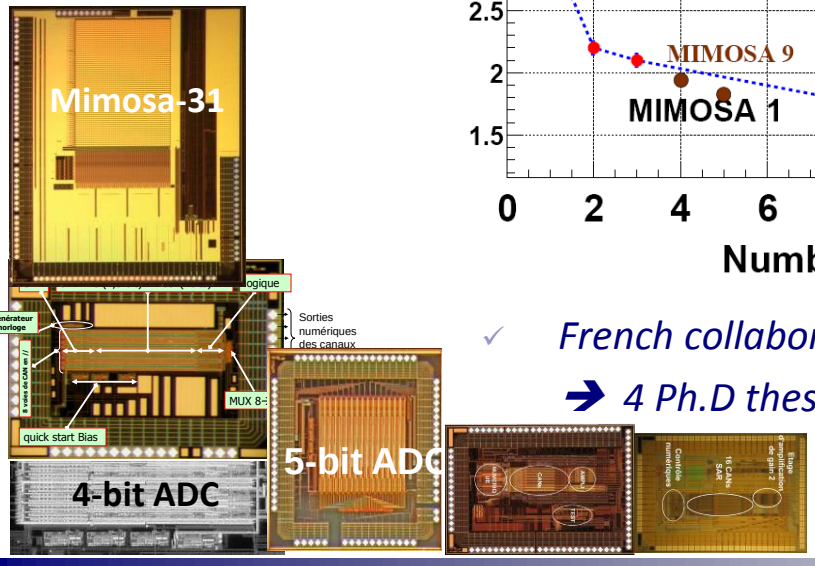


for 20 µm pitch:

- *5 bits: σ_{sp} ~1.7–1.6 µm*
- *4 bits: σ_{sp} < 2 µm*

critical parameters:

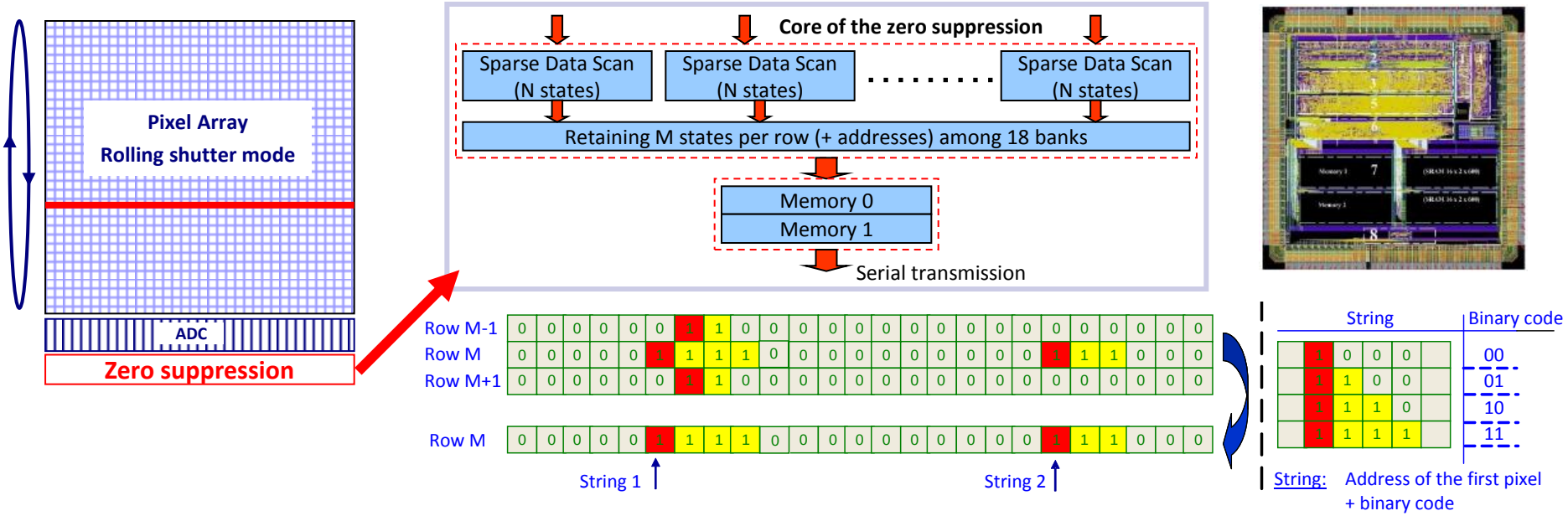
- *LSB ~ 1mV*
- *Power consumption < 500 µW*
- *Conversion time ~100 ns*
- *Form factor: width = pixel pitch ~20 µm*



- ✓ *French collaboration: LPCC, LPSC, IRFU, IPHC*
  - ➔ *4 Ph.D theses in these subjects*

Mid-stage of CPS Development: 2003 - 2008 (5)

- *Zero suppression micro-circuit & output memories: SUZE-01 (AMS 0.35 µm, 2007) was based on row by row sparse data scan readout in pipeline mode in 3 steps:*



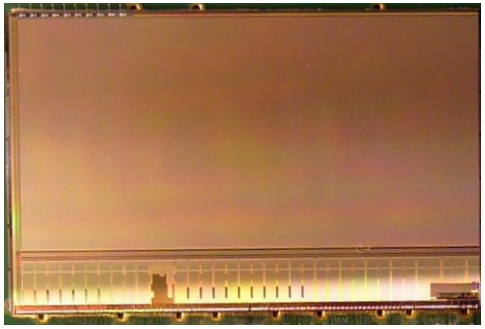
  - *To find strings of hit pixels (up to N strings) in a row, in parallel in all banks and encode in 2 bits word following by address of the 1st pixel*
  - *To read out the outcomes of the 1st step in all banks and keep up to M strings + add row and bank addresses*
  - *Outcomes are stored to a memory buffer: 2 IP's buffers for continuous RO*
    - *Serial out by 1 or 2 LVDS at up to 160 MHz*

➔ *Sizable & adaptive Logic vs. sensor size. SUZE logic was suited to hit density >~ 10^6 hits/cm²/s*

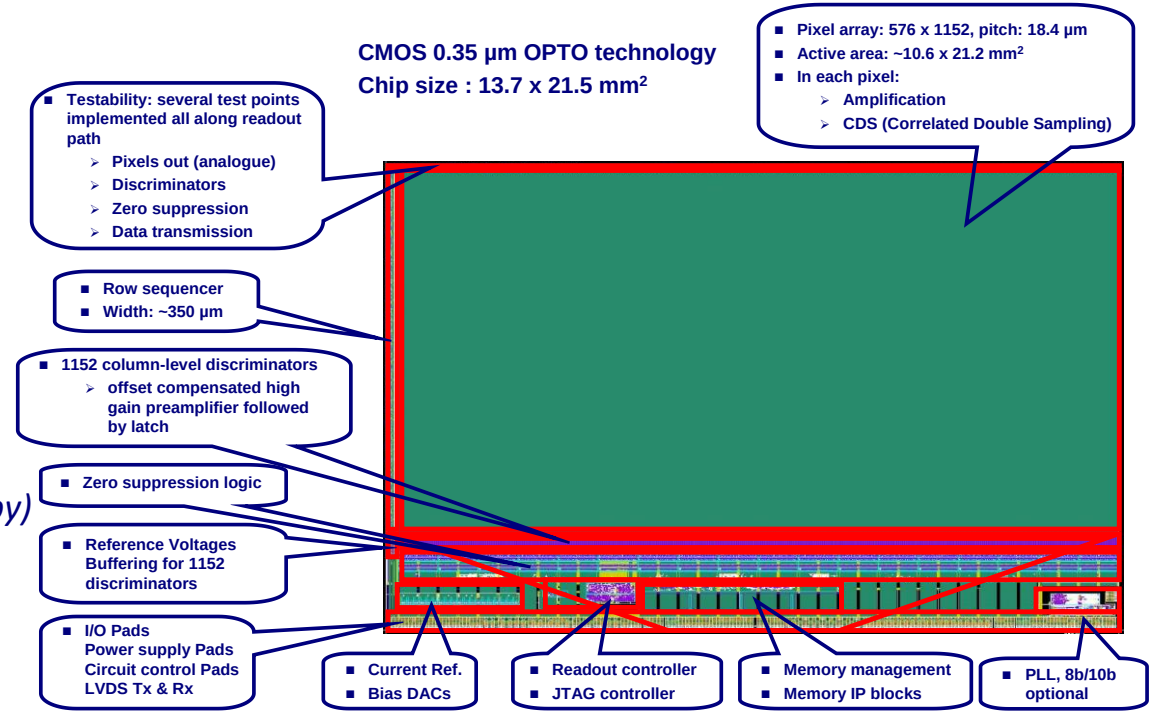
- ***Development of building blocks for system level design ➔ SoC***
  - *Bias DAC, ADC, Latch-up free Memories, Serialiser, Rx-Tx , Slow Controller, Band Gaps, Regulators, Power On Reset, PLL …*

Mature-Stage of CPS Development: 2008 - … (1)

- *Combine sensing, building blocks & signal processing parts in a large scale sensor:*
  - *Mimosa-26 (2008): sensor equipping EUDET (FP6) beam telescope*
    - ★ *Milestone in CPS development*



MIMOSA26: 1st MAPS with Integrated Ø

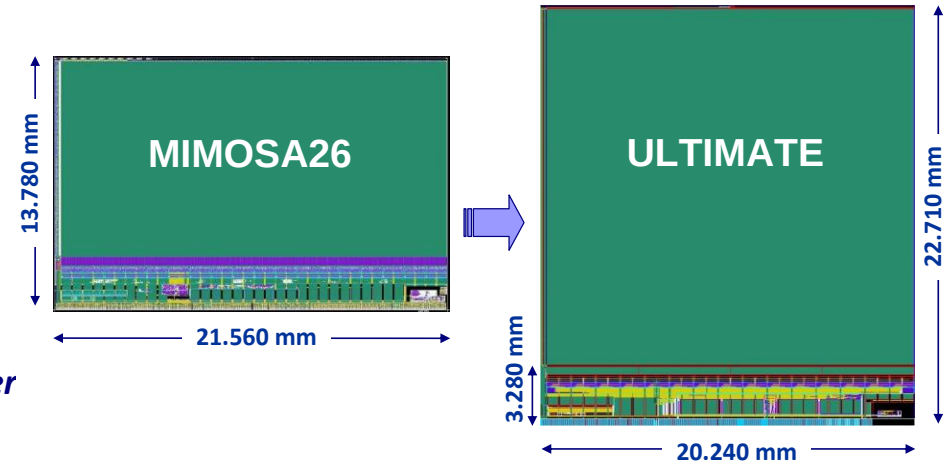


Spin-offs:

- *CBM-MVD demonstrator*
- *Hadrontherapy : FIRST*
- *Proton imaging and dosimetry (ocontherapy)*
- *NA63 expt (positron prod. in crystal)*
- *PLUME double-sided ladder*
- *AIDA (EU-FP7) alignment device*

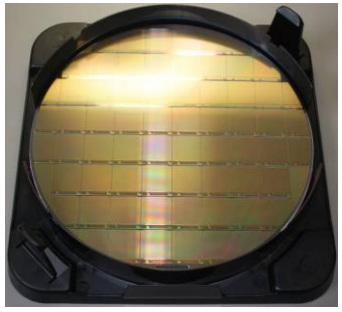
Mature-Stage of CPS Development: 2008 - … (2)

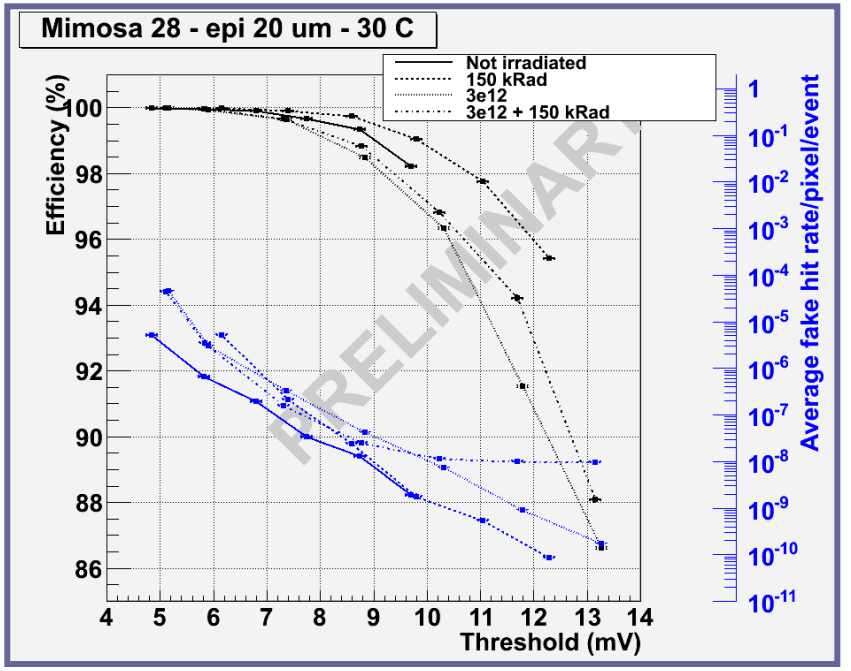
- *Final sensor for STAR PXL: ULTIMATE (M-28, 2011) → not only an extension of Mimosa-26*
  - *Reduce power dissipation*
  - *Improve CCE, radiation tolerance*
  - *Optimise pixels & discriminators uniformity*
  - *Implement on-chip voltage regulators*
  - *Adapt SUZE to STAR condition*



- *ULTIMATE main characteristics:*
  - *0.35 µm process **with high-resistivity epitaxial layer***
  - *Active area: 19.9 × 19.2 mm² , 960 x 928 pixels*
  - *Pixel pitch: 20.7 µm → $\sigma_{s.p.}$ >~ 3.5 µm expected*
  - *Column // architecture with in-pixel ampli. & CDS*
  - *End-of-column discri. and binary charge encoding, followed by SUZE logic → suited to >10^6 hits/cm²/s*
  - *$t_{r.o.}$ <~ 200 µs with 2 LVDS outputs at 160 MHz*
  - *Temperature: 30-35 °C, ~160 mW/cm²*
  - *Radiation tolerant ~150 kRad/yr & 3x10^{12} n_{eq}/cm²/yr*

- *Design review (end of 2010)*
  - → *1st fabrication in Q1 2011, 2nd batch in Q1 2013*

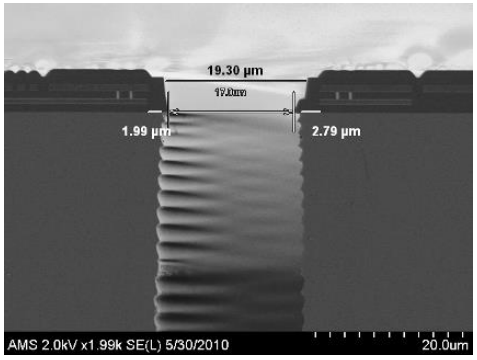




CPS Detection Performance vs. Technology Parameters

- *High-resistivity epitaxial layer*
  - *2 important parameters for CCE, radiation tolerance: resistivity & thickness of epitaxial layer*
  - *We had no choice on these technology parameters for a long period*
    - ⋆ *Standard EPI layer (~10 Ω.cm) & 14 µm thick*
    - ⋆ *These limitations fostered going for high voltage CMOS process*
      - ✓ *CCE mitigated by absence of EPI/substrate interface*
  - *Customised EPI layers ➔ provide a breakthrough for CPS detectors*
    - ⋆ *We accessed to high resistivity EPI layer since 2011*
      - ✓ *STAR PXL: > 400 Ω.cm (15 µm thick)*

- *DRIE (Deep Reactive Ion Etching)*
  - *Edgeless sensors ➔ improve butting during detector ladder assembly*
    - ⋆ *100 HiRes EPI wafers produced with DRIE pre-dicing for STAR PXL*



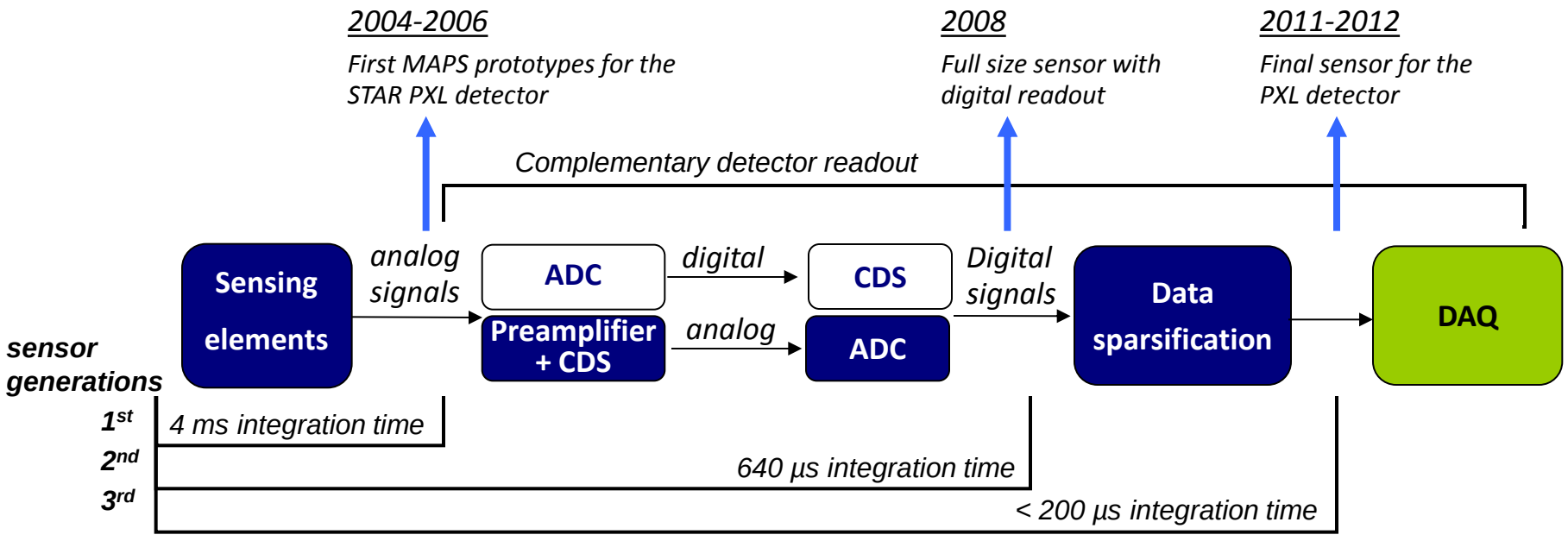
DRIE cross section, 17 µm

MIMOSA-28 edgeless corner

DRIE trenches

STAR PXL sensors

- *Three generations of sensors have been specifically designed for the PXL detector*
  - *STAR PXL sensors R&D illustrates evolution of CPS development*



Courtesy of M. Szelezniak, HICforFAIR Workshop 2014

- *Architecture (rolling shutter column parallel readout with integrated zero suppression logic) developed for STAR PXL is well suited to a twin-well CMOS process*
  - *New architectures are being developed with TJ 0.18 µm CIS process (quadruple well process)*
    - ⋆ *See Marc Winter talk on sensors design for ALICE-ITS upgrade*

Conclusion (1)

- *STAR PXL is the first CPS based detector in a large physics experiment*
  - *Completed 4 months data taking*
- *Structuring project both for design & team organisation*
  - *Design: from sensing elements, …, building blocks to system level integration (SoC)*
  - *Team: coherent task dispatching between design, test, system integration*
    - *2000: 3 FTE ➔ 2014: ~25-30 FTE*
    - *~ 20 Ph.D students involved in the development*

- *Very successful LBNL-IPHC collaboration in all R&D stages*
  - *Detector design, Sensor Development, Construction, Installation, Commissioning*
  - *Know-how exchanges, Rapid reactivity ➔ stimulate further collaborative momentum*

- LBNL: focused on the PXL global architecture, benefited from IPHC expertise in cutting edge CMOS Pixel Sensors technology

- IPHC: focused on sensor design, acquired knowledge of full system design guided by LBNL

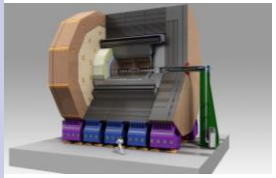
Conclusion (2)

- *STAR PXL sensors benefited from synergy among experiments also requiring CPS development at IPHC*
  - *Common submissions, human resources, budget*

- ***Initial objective: ILC, with staged performances***
  - *CPS applied to other experiments with intermediate requirements*

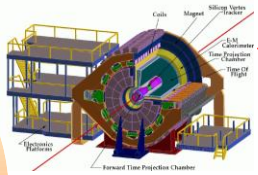
EUDET 2006/2010
Beam Telescope

ILC >2020
International Linear Collider

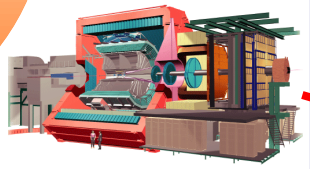


EUDET (R&D for ILC, EU project)
STAR (Heavy Ion physics)
CBM (Heavy Ion physics)
ILC (Particle physics)
HadronPhysics2 (generic R&D, EU project)
AIDA (generic R&D, EU project)
FIRST (Hadron therapy)
ALICE/LHC (Heavy Ion physics)
EIC (Hadron physics)
CLIC (Particle physics)
BESIII (Particle physics)
…

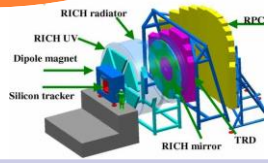
STAR 2013
Solenoidal Tracker at RHIC



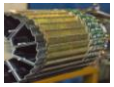
ALICE 2018
A Large Ion Collider Experiment

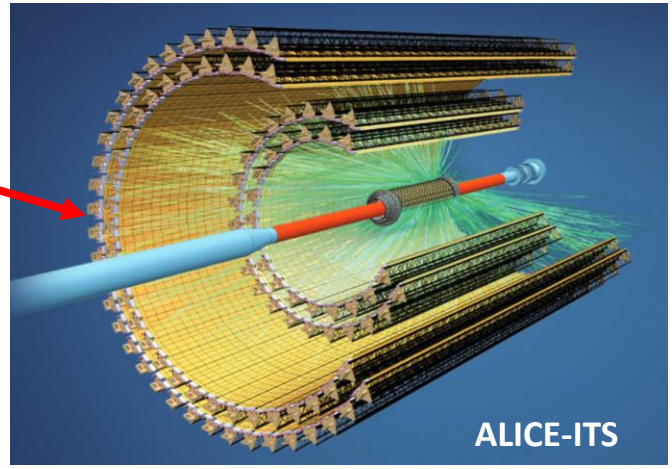


CBM >2018
Compressed Baryonic Matter



STAR-PXL



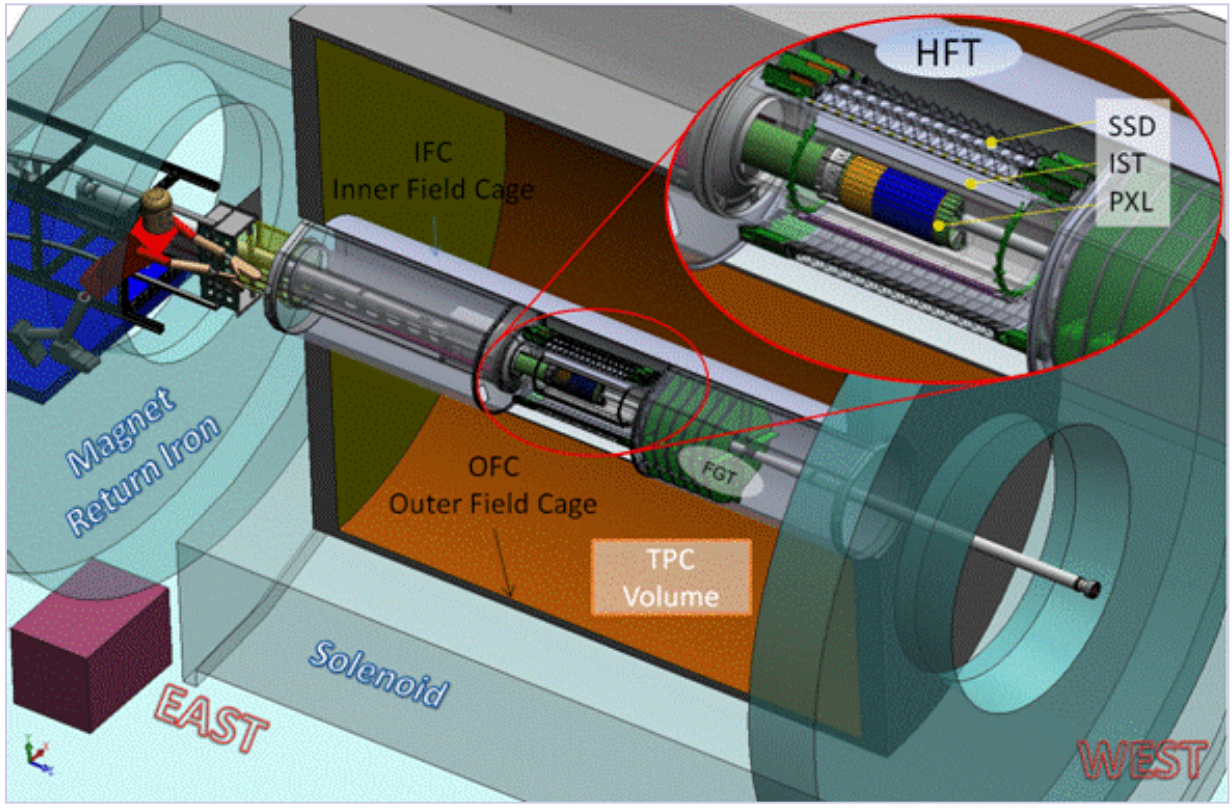


- *From STAR PXL (0.15 m²) ➔ ALICE-ITS (10 m²)*
  - *Tight schedule (2016 production) achievable thanks to accumulated knowledge on design and characterization of previous sensors*

Back-up slides

STAR Heavy Flavor Tracker (HFT) Upgrade

- *Identification of mid rapidity Charm and Beauty mesons and baryons through direct reconstruction and measurement of the displaced vertex with excellent pointing resolution*

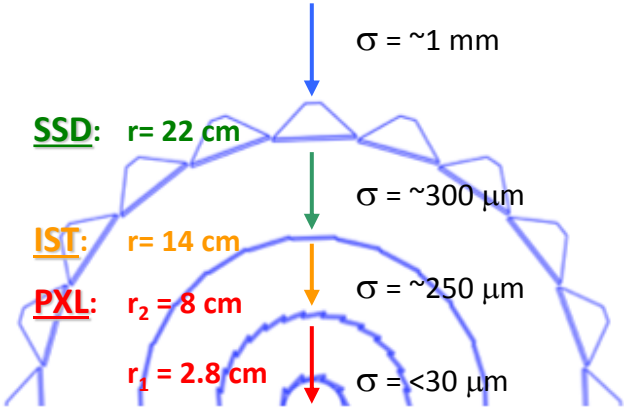


courtesy of L. Greiner / FEE-2014

TPC – Time Projection Chamber (main tracking detector in STAR)

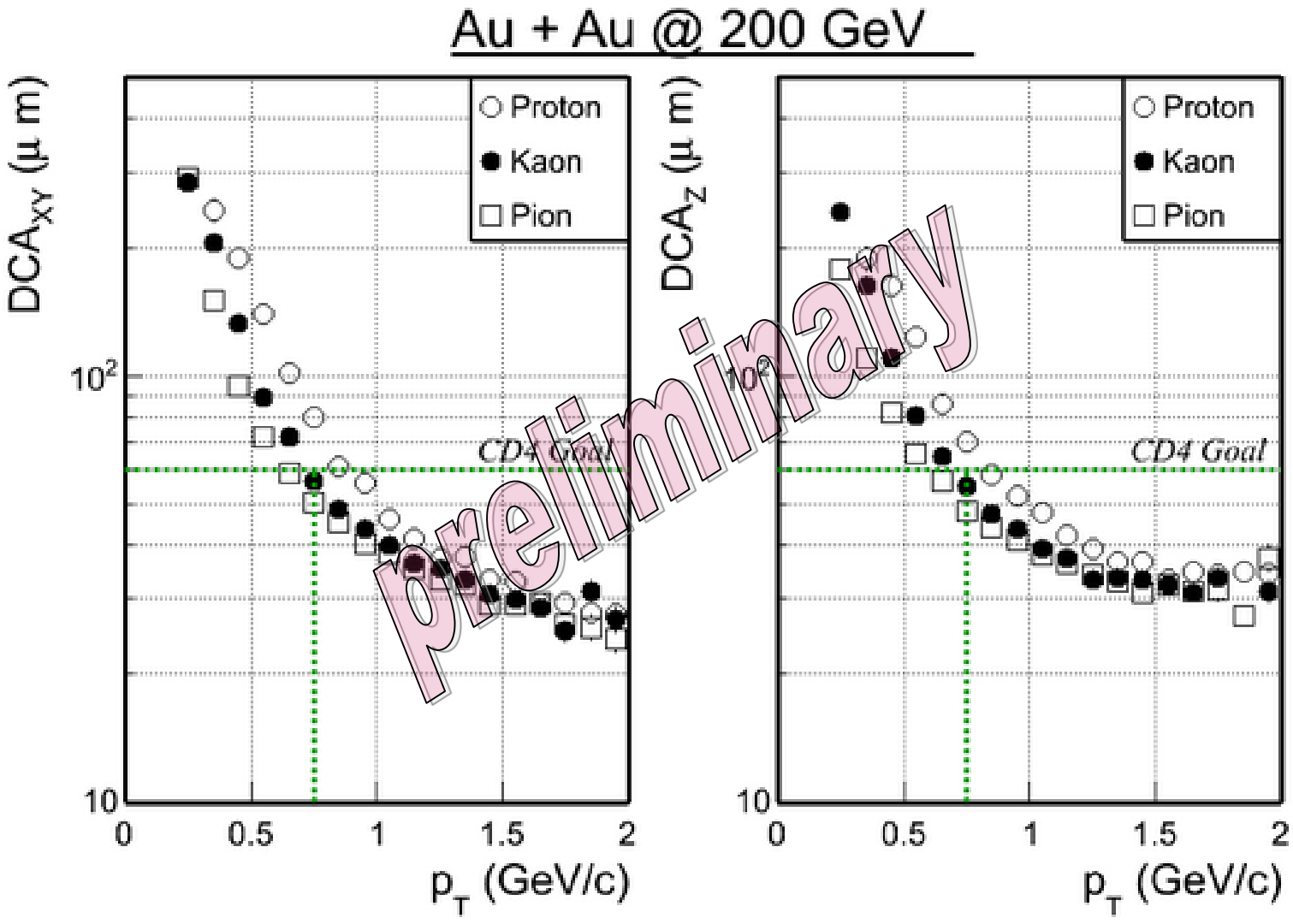
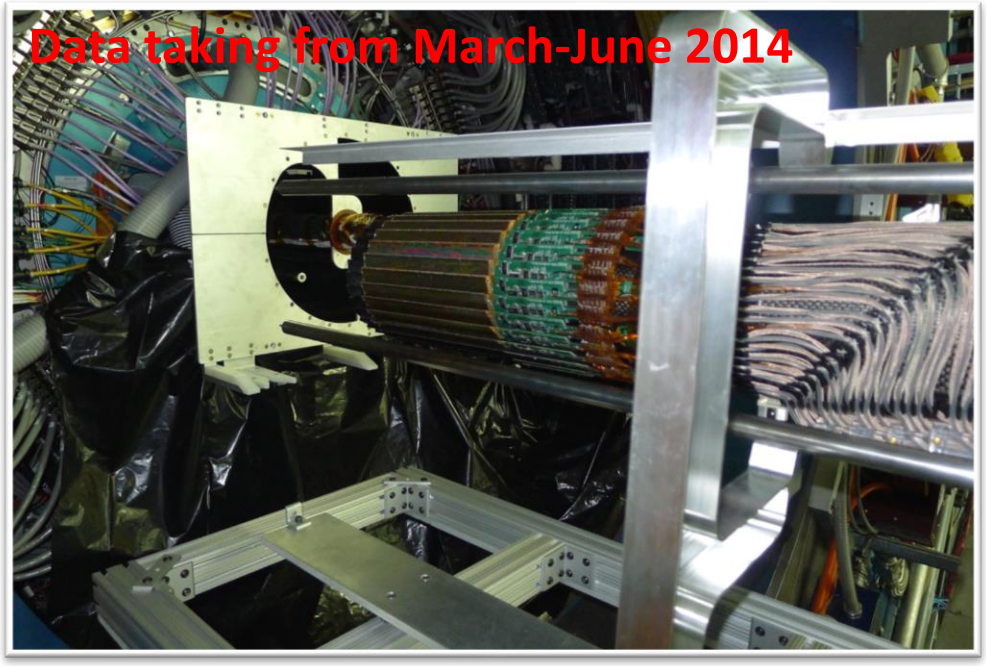
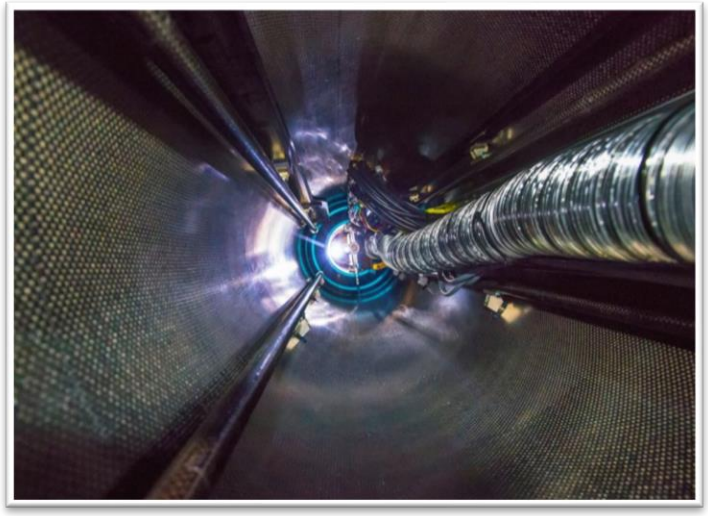
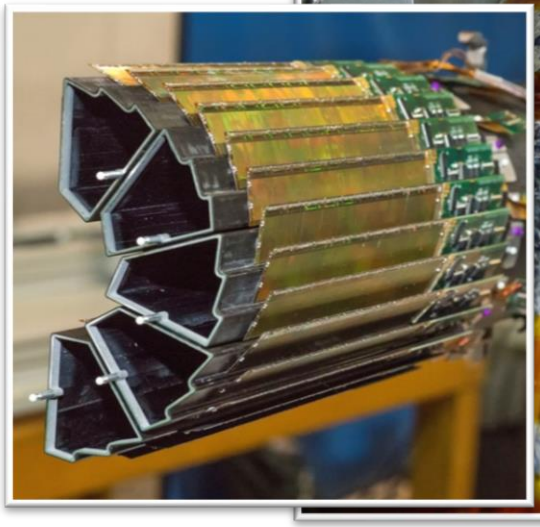
HFT – Heavy Flavor Tracker

- SSD – Silicon Strip Detector
- IST – Inner Silicon Tracker
- PXL – Pixel Detector (PIXEL)



We track inward from the TPC with graded resolution:

Distance of Closest Approach = DCA



Starting point: Ultimate chip in STAR