

TE-EPC-CCE Radiation Tests

2012-2013



Summary

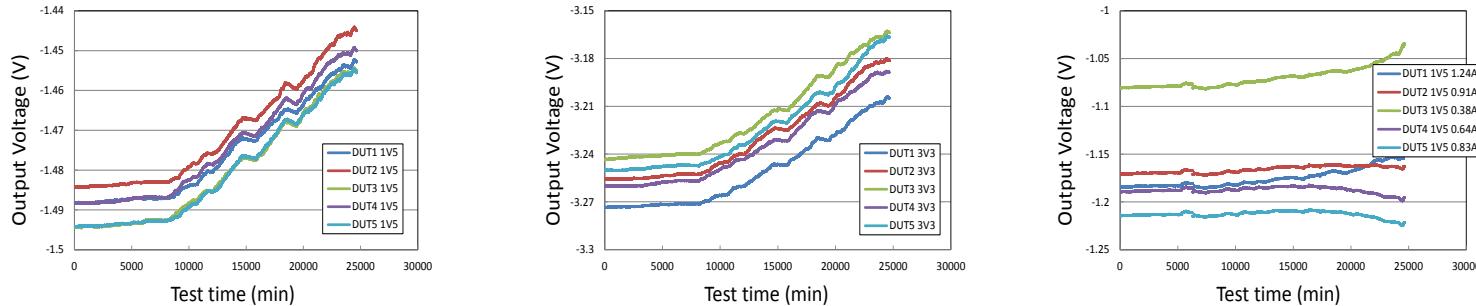
1. H4IRRAD 2012
 1. May: ADS1281, DS18B20, DS2401, SPLargeUHD9
 2. Jul: MAX5541, MIC37302
 3. Nov: MIC37302, FGClite
 2. ANDI Batch Tester
 1. ADS1271B (PSI – Apr/Oct 2013, TRIUMF – Dec 2013)
 2. ADS1281 (PSI – Oct 2013)
 3. MAX5541 (PSI – Oct 2013)
 3. HIDE Batch Tester
 1. R1LV1616R Renesas SRAM (PSI – Oct 2013, TRIUMF – Dec 2013)
 2. A3P250, A3P400, A3P1000, A3PE1500 (PSI – Oct 2013)
 3. FGClite Analogue Filter Design (PSI – Oct 2013)
- 
- RadWG Oct 2012

Components Identification and test setup description

DUT name	DUT type	Test Type	Samples tested	Package	Date code	Lot code
MIC37302	Low-dropout voltage regulator	TID, SEE	15	S-Pak-5	unknown	unknown

Low cost COTS adjustable low-dropout voltage regulator (RadDIM project)
 SEE and TID test for different output voltages 1V5 and 3V3 and different loads 0.1-1.2A

Results



No SEL detected: SEL cross-section upper level (90%) < $6.6 \times 10^{-13} \text{ cm}^2$

Voltage out degradation as a function of dose (irradiated up to $\sim 90\text{Gy}/\text{component}$):

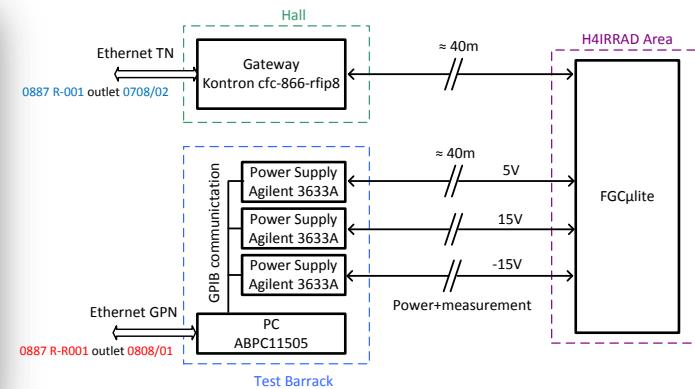
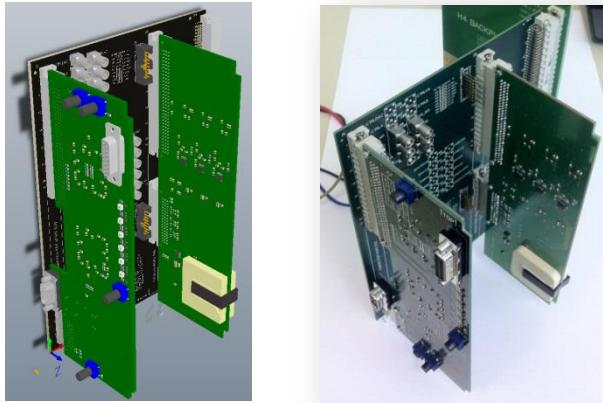
0.360mV/Gy (1V5, 183mA of load)

0.920mV/Gy (3V3, 100mA of load)

0.160mV/Gy (1V5, variable load)

PSI tests Sep 2013 done by EN-STI confirmed these results
 (no SEL detected, regulation ok until 300Gy, enable pin fails at 150Gy)

Test setup



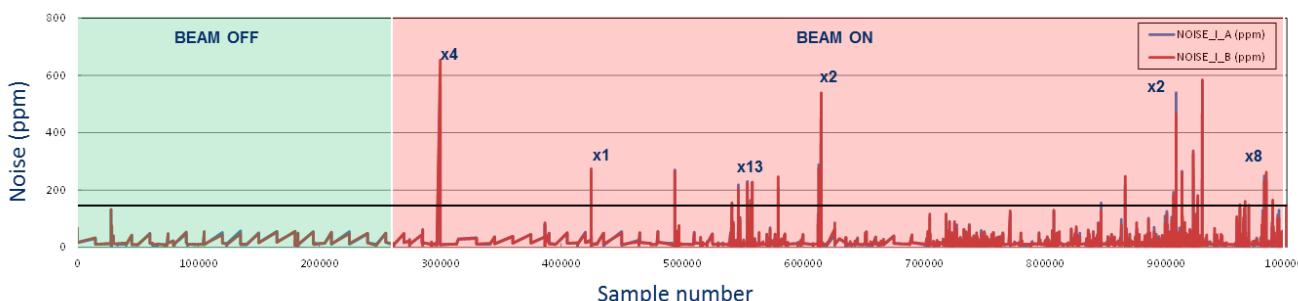
Results

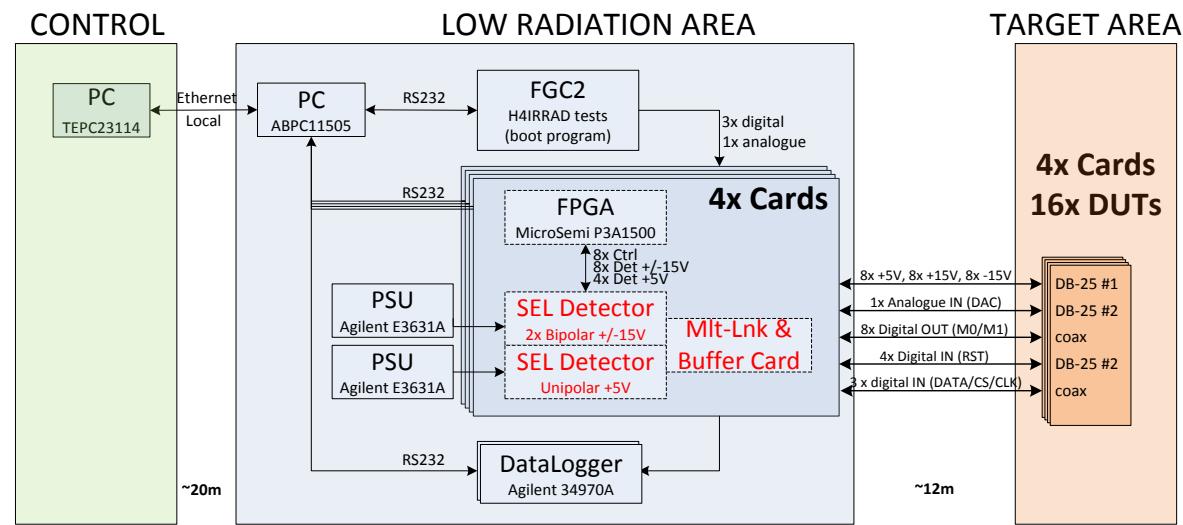
Time stamp	Cycle	Ref	Channel I_A	Channel I_B
22/11/2012 15:48:40.680	0x00402F12,0x7555	0x00783358,0x00783341,0x00783358	0x00782E5A,0x00782E4A,0x00782E5A	
22/11/2012 15:48:40.700	0x00402F13,0x7555	0x0078334D,0x00783346,0x00783358	0x00782E4E,0x00782E45,0x00782E59	

No SEL detected: SEL cross-section upper level (90%) < 1.6e-11 cm²

No radiation-induced effect were identified. No observable TID power consumption increase.

System has shown significant level of noise. Spikes in measurements >550ppm (spec <50ppm), not correlated with the beam (we suspect the EMC-induced noise)

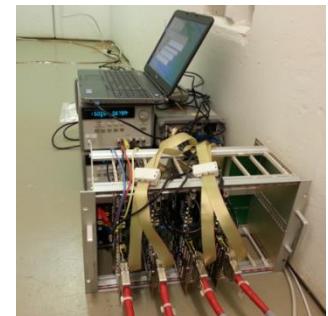
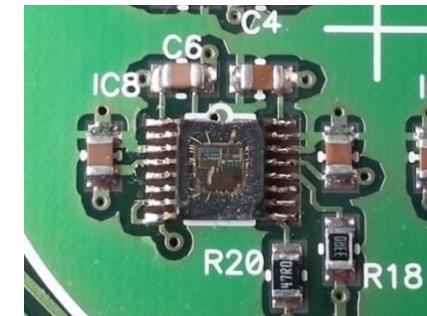




Allows the real time data analysis during the test

1. Generates input for DUTs
2. Analyses the outputs from DUTs
3. Actively performs the power cycle (SEL)
4. Records all measurements from DUTs

1. ADS1281
2. MAX5541
3. ADS1271B
4. Others...

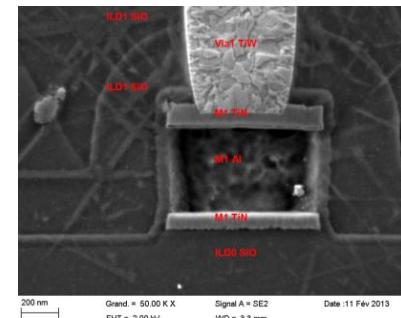


Context

SEL study and influence of high-Z materials on SEL cross-section

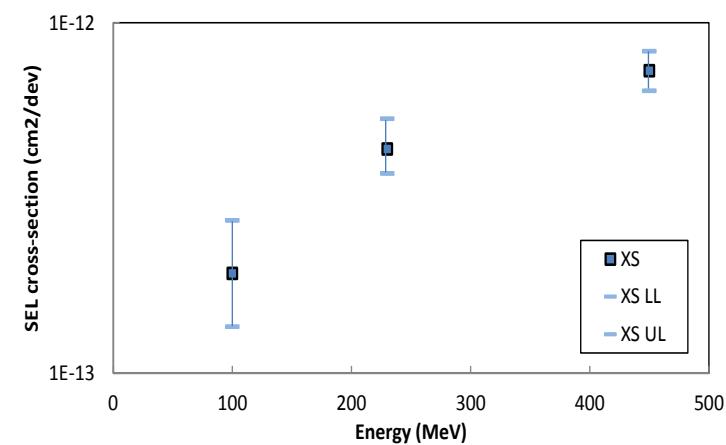
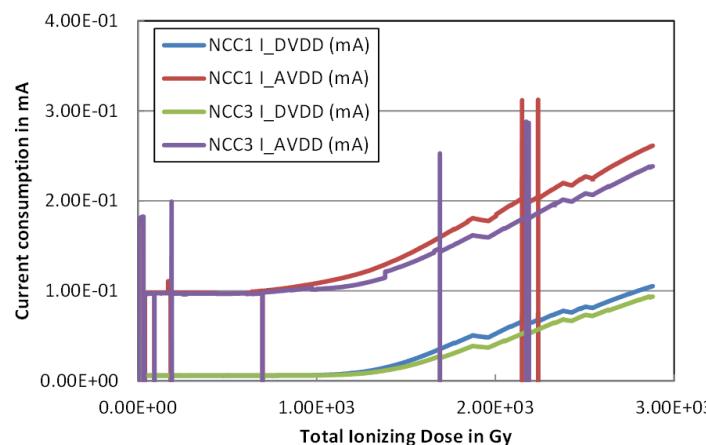
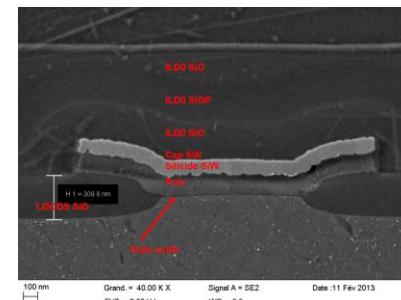
Significance of cross-section increase with energy

Margins to be applied on the 230MeV data when assessing the error rate in the LHC



Test results

Measurable SEL cross-section in range $1\text{e-}13$ to $1\text{e-}12 \text{ cm}^2$
 Increase of the cross-section with energy attributed to tungsten
 SEL current between 50 to 300mA (16mA nominal)
 TID limit $>2\text{kGy}$



Context

High precision delta-sigma ADC for FGClite
CERN Batch yielded from 3 Si wafers (4500 IC)

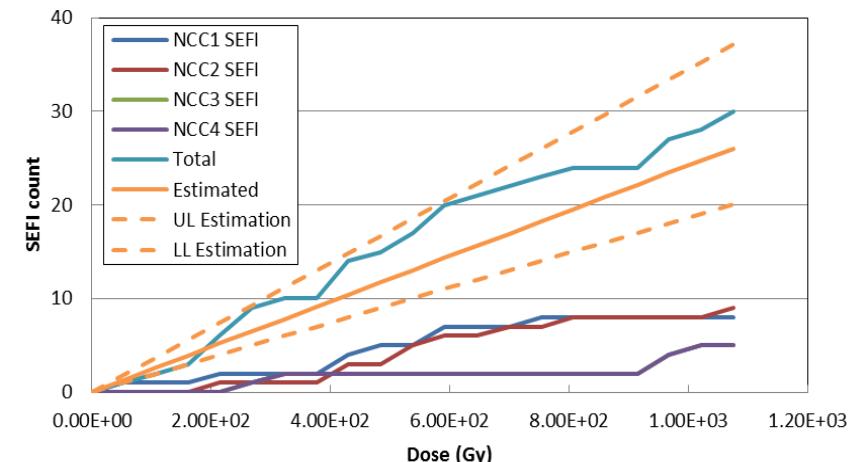
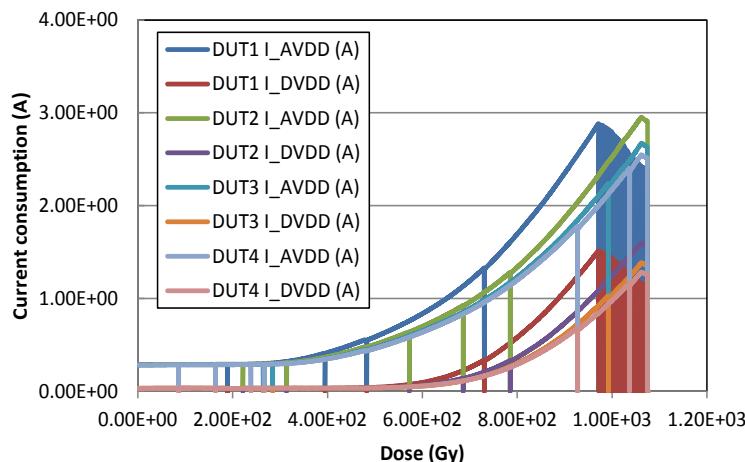
Test Set	DUT name	DUT type	Test Type	Samples tested	Package	Date/lot code
#1	ADS1281x4 DUT 1	High-Res ADC	SEL, SEFI	4x packaged	TSSOP-24	CERN reference
#2	ADS1281x4 DUT 2	High-Res ADC	SEL, SEFI	4x packaged	TSSOP-24	CERN reference
#3	ADS1281x4 DUT 3	High-Res ADC	SEL, SEFI	4x packaged	TSSOP-24	CERN reference
#4	ADS1281x4 DUT 4	High-Res ADC	SEL, SEFI	4x packaged	TSSOP-24	CERN reference

Test results

No SEL detected: SEL cross-section upper level (90%) < 7.2e-14 cm²

Modulator SEFI cross-section = 8.1e-13 cm²

TID limit > 1kGv



Context

16-bit DAC for FGClite

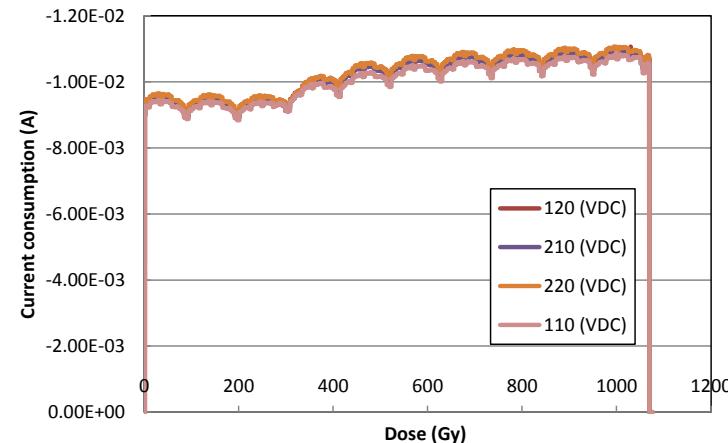
Test Set	DUT name	DUT type	Test Type	Samples tested	Package	Date/lot code
#1	MAX5541x4 DUT 1	DAC	SEL, SEFI	4x packaged	8-SO	1592369
#2	MAX5541x4 DUT 2	DAC	SEL, SEFI	4x packaged	8-SO	1592369
#3	MAX5541x4 DUT 3	DAC	SEL, SEFI	4x packaged	8-SO	1592369
#4	MAX5541x4 DUT 4	DAC	SEL, SEFI	4x packaged	8-SO	1592369

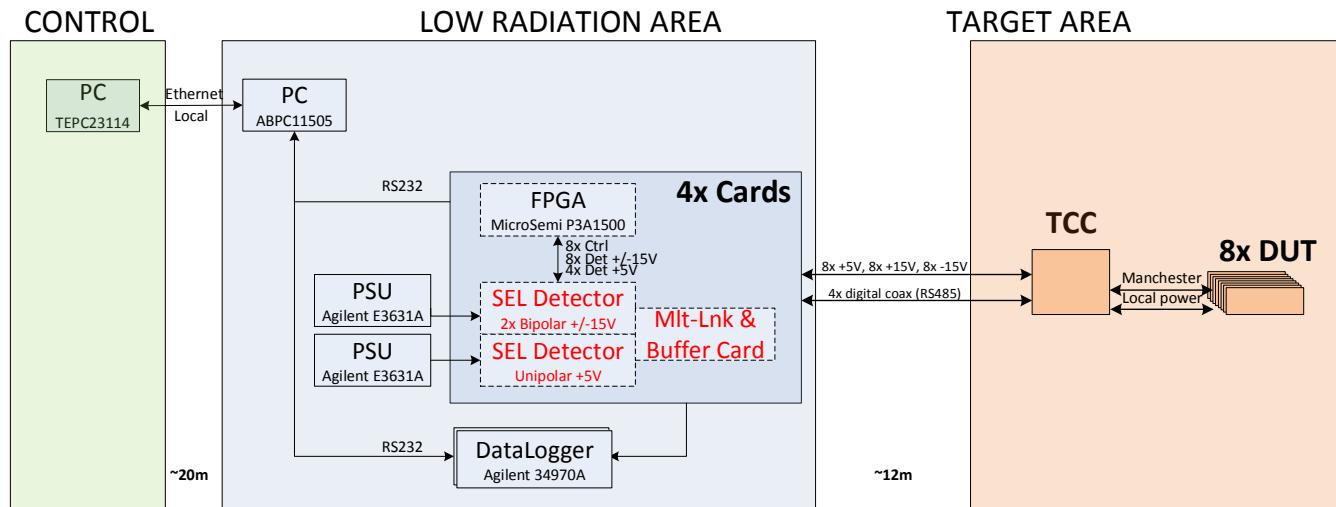
Test results

No SEL detected: SEL cross-section upper level (90%) < 7.2e-14 cm²

No SEFI detected: SEFI cross-section upper level (90%) < 7.2e-14 cm²

TID limit > 1kGy

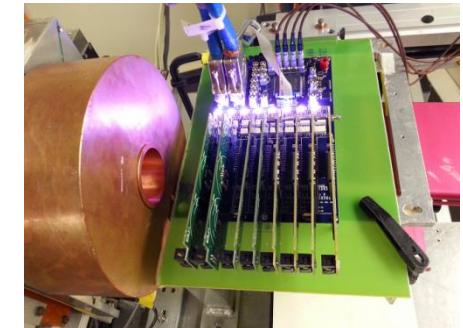
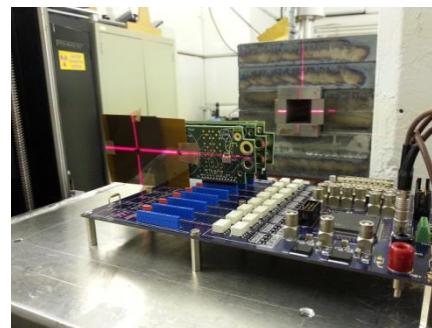




Allows the real time data analysis during the test

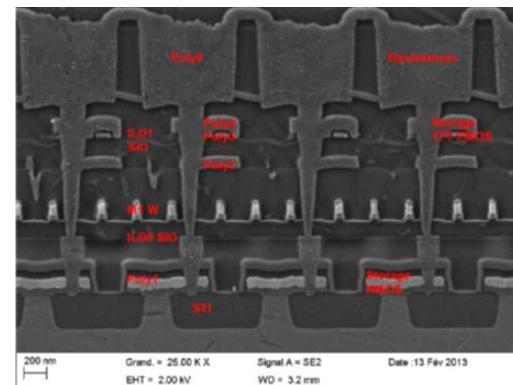
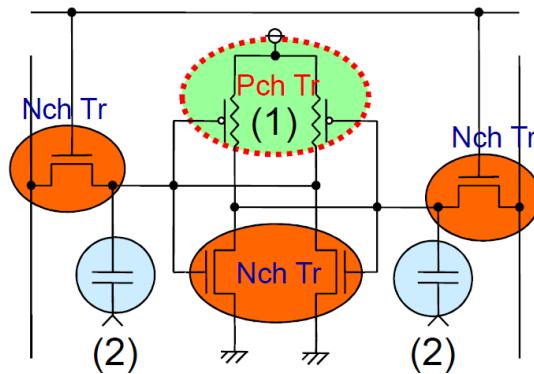
1. Generates input for DUTs
 2. Analyses the outputs from DUTs
 3. Actively performs the power cycle (SEL)
 4. Records all measurements from DUTs

1. FPGA
2. Memories (SRAM)
3. Others...



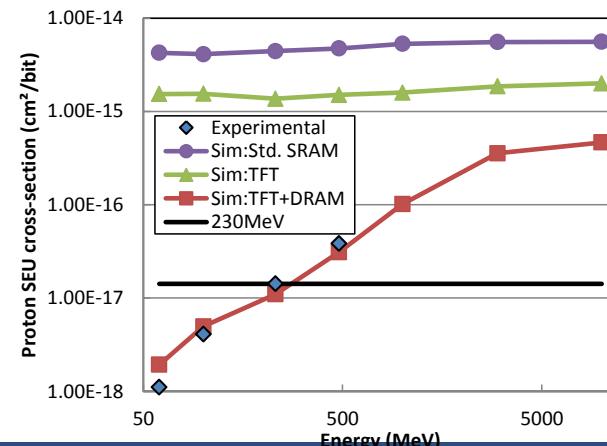
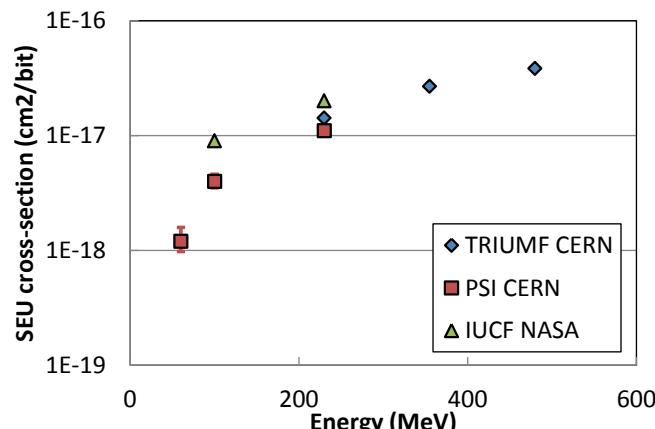
Context

16-Mbit SRAM memory for the FGClite
TFT + DRAM bit cell architecture
No SEL possible, very low SEU cross-section



Test Set	DUT name	DUT type	Test Type	Package	Lot Date Code (MSC batch)
#1	R1LV1616R DUT 1	SRAM	SEU/MBU	48-pin TSOP	1343 (2013430001)
#2	R1LV1616R DUT 2	SRAM	SEU/MBU	48-pin TSOP	1328 (2013280004)
#3	R1LV1616R DUT 3	SRAM	SEU/MBU	48-pin TSOP	1343 (2013430002)
#4	R1LV1616R DUT 4	SRAM	SEU/MBU	48-pin TSOP	1343 (2013430002)
#5	R1LV1616R DUT 5	SRAM	SEU/MBU	48-pin TSOP	1328 (2013280003)
#6	R1LV1616R DUT 6	SRAM	SEU/MBU	48-pin TSOP	1343 (2013430001)

Test results



Context

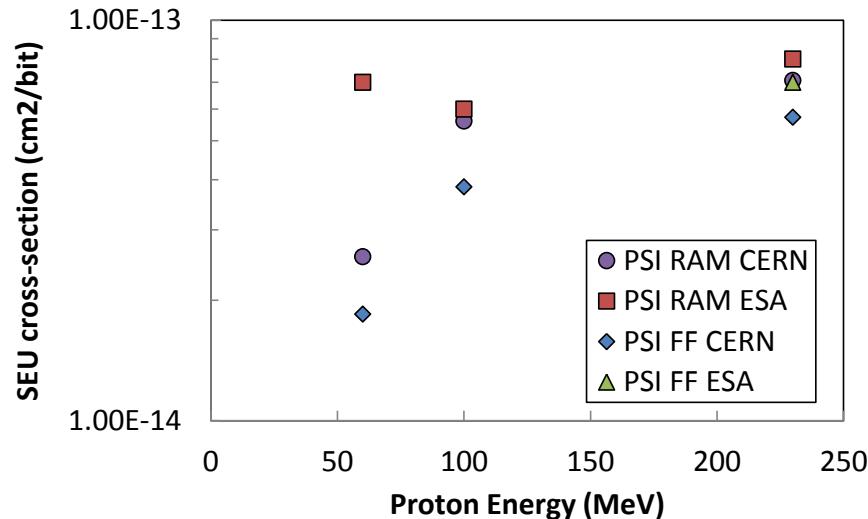
- Well-known ProASIC-3 radiation data (A3PE3000L published by ESA)
- Different FPGA sizes = Same radiation response?
- FF/block RAM SEU cross-section measurement

DUT	FPGA	Package
1	A3P250	VQ100
2	A3P250	VQ100
3	A3P250	VQ100
4	A3P250	VQ100
5	A3P400	PQ208
6	A3P400	PQ208
7	A3P1000	PQ208
8	A3PE1500	PQ208

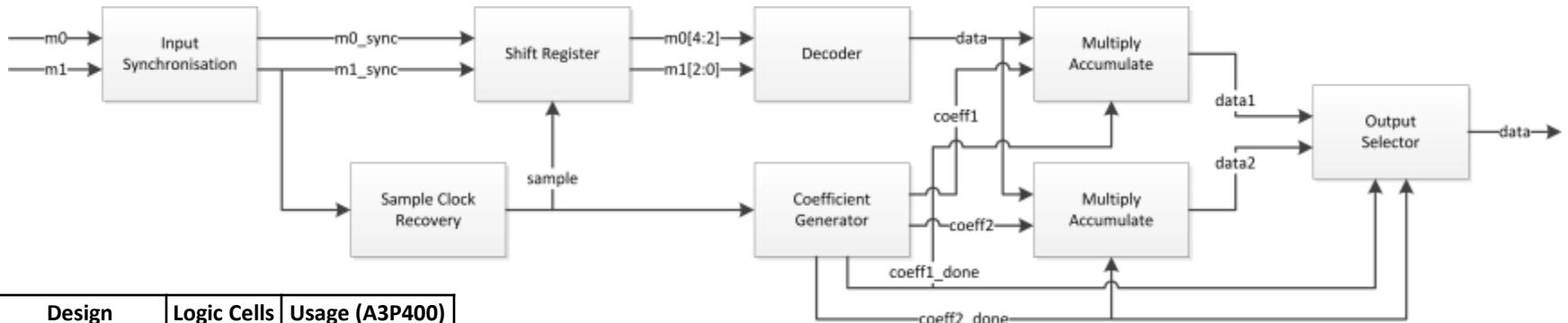
Test results

FF tests: 90% of all FF in each FPGA was used (shift registers)
 Test pattern influence <30% (all'0' most sensitive, all'1' least sensitive)
 Size influence <20% (250 most sensitive, A3PE1500 least sensitive)
 Frequency influence <15% (1kHz most sensitive, 1Hz least sensitive)

RAM tests: 100% of all blocks in each FPGA was used
 Test pattern influence <40% (all'0' most sensitive, all'1' least sensitive)
 Size influence <30% (250 most sensitive, A3PE1500 least sensitive)



Context



Design	Logic Cells	Usage (A3P400)
3 CHs	3,937	42.72 %
3 CHs w/ TMR	6,642	72.07 %

Test results

DUT number	Size	Design	Run1 1e11 p/cm ²	Run2 5e12 p/cm ²
DUT0	1000	noTMR		
DUT1	1000	TMR		
DUT2	1500E	noTMR		1
DUT3	1500E	TMR		
DUT4	400	noTMR	1	2
DUT5	400	TMR		
DUT6	400	noTMR		4
DUT7	400	TMR	1	2

We observed errors with TMR : Test setup limitation, TMR failing due to latching of SET, TID limit of components (400-500Gy)
 Further irradiations needed!