Wafer Procurement, Sensor Post-processing and Interconnect R&D

P. Riedler, CERN

Wafer procurement and QA

Choice of starting wafer material

- Used different high-res epi wafers in ER2013
- Final choice will depend on test results of prototype chips:
  - Select epi thickness
  - Select resistivity
- Procurement of the wafers for the production should start end of 2014/beginning of 2015

Goals for 2014:

- Finalize choice of high-res wafers by end 2014
- Finalize QA by end of 2014

Wafer procurement and QA

- Ordered new set of wafers to be available for the next engineering runs.
- Partially delivered (will be completed July 31, 2014)

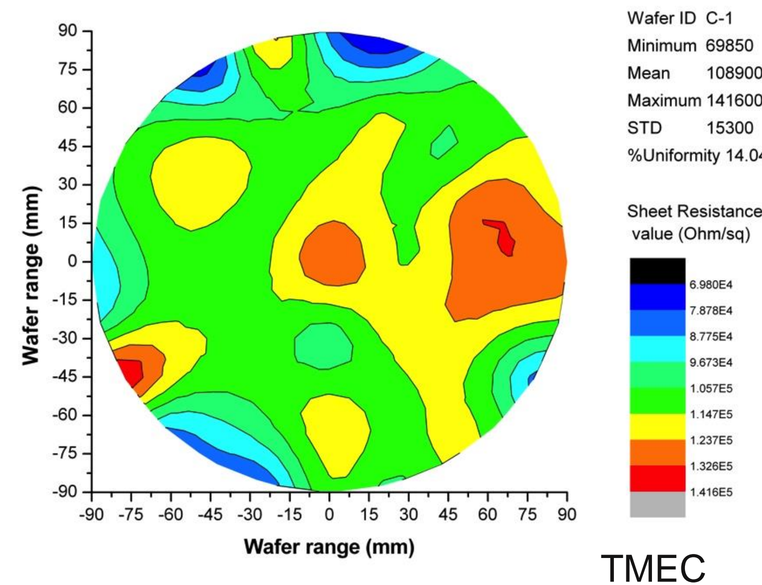
Epi thickness	Resistivity	# wafers	Status
20 µm	>1kΩcm	12	Delivered 9/6
25 µm	>1kΩcm	6	Delivery ~ 25/6
30 µm	>1kΩcm	12	Delivered 9/6
30 µm	>2kΩcm	25	Delivery ~ 31/6

Wafer QA before processing

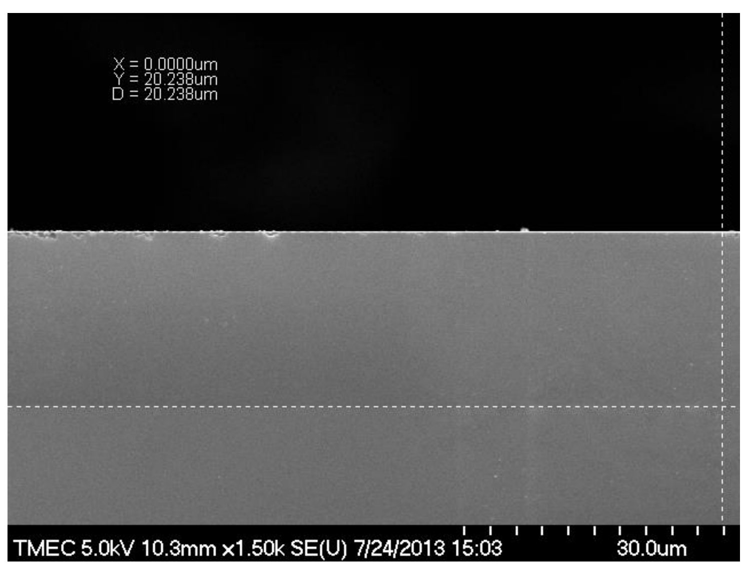
Data supplied by vendor for custom wafers: epi thickness, resistivity

QA activities with TMEC on sample basis:

- ✓ SEM cross-section inspection
- ✓ Surface resistivity measurement
- SRP measurement of resistivity profile in the epi layer
    - Ordering reference samples



TMEC



TMEC

Wafer Post-Processing List

Processing after delivery of CMOS wafers from the foundry:

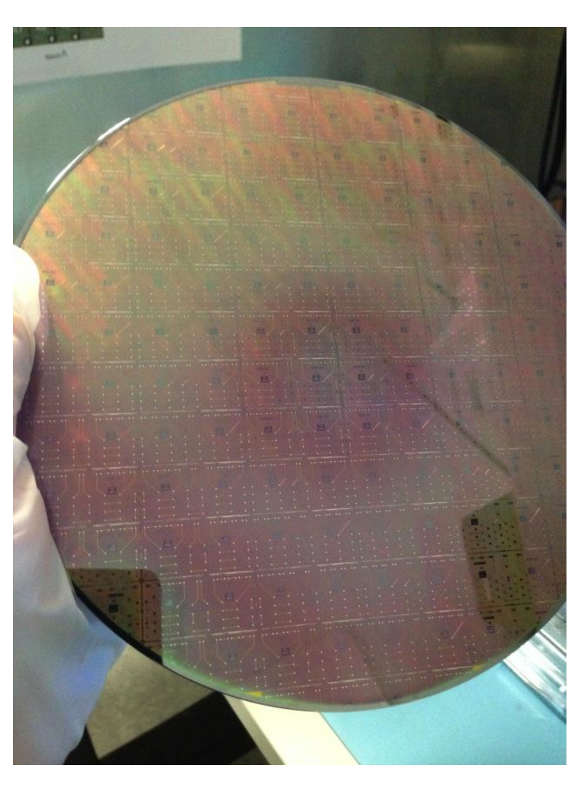
- **Plating (Ni/Au)**
- **Thinning&Dicing**

Several wafers presently in the pipeline for post-processing:

	# wafers	Ni/Au plating	DBG	Status
ITS2 - I	2 (high res)	PacTech	tbd	At PacTech
ITS2 - II	5 (high res)	PacTech	tbd	At PacTech
ITS_pad (50c)	7+1 (setup)	PacTech	tbd	At PacTech
ITS_pad (50c)	16	PacTech	tbd	At PacTech
Total	**31**			

Pad wafers with 50 contacts

To be used for assembly tests



Pad wafers with 50 contacts

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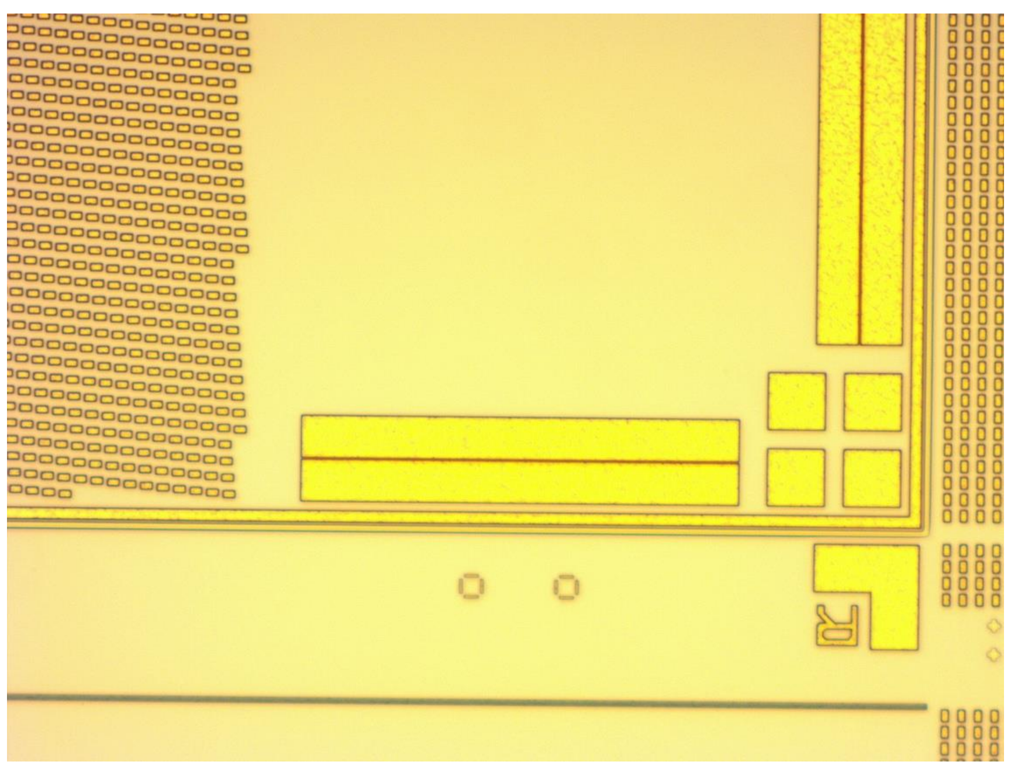
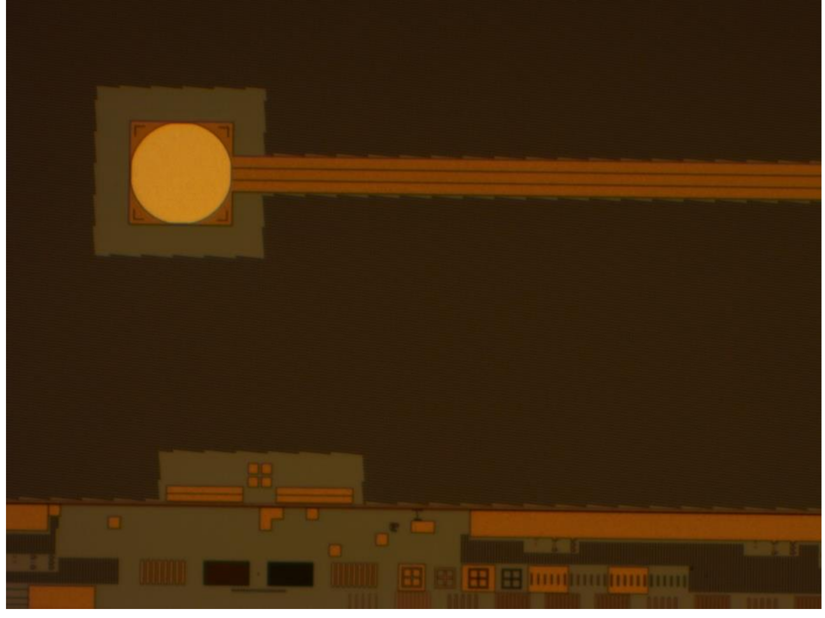


- M6+Passivation
- Produced by TowerJazz
- Scribeline (and test structures) as on full CMOS wafers → **can be used for thinning and dicing tests**

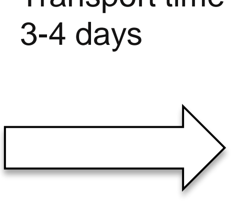


Post-Processing Schedules

Turn-around time is not negligible for complex DBG and Ni/Au plating → requires careful planning not to delay subsequent activities.

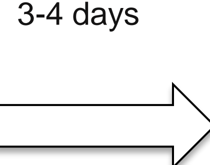
Ni/Au plating
(mask generation,
processing ~ 4 weeks)

Transport time
3-4 days



Dicing and grinding
~ 1 week (if slot is
available)

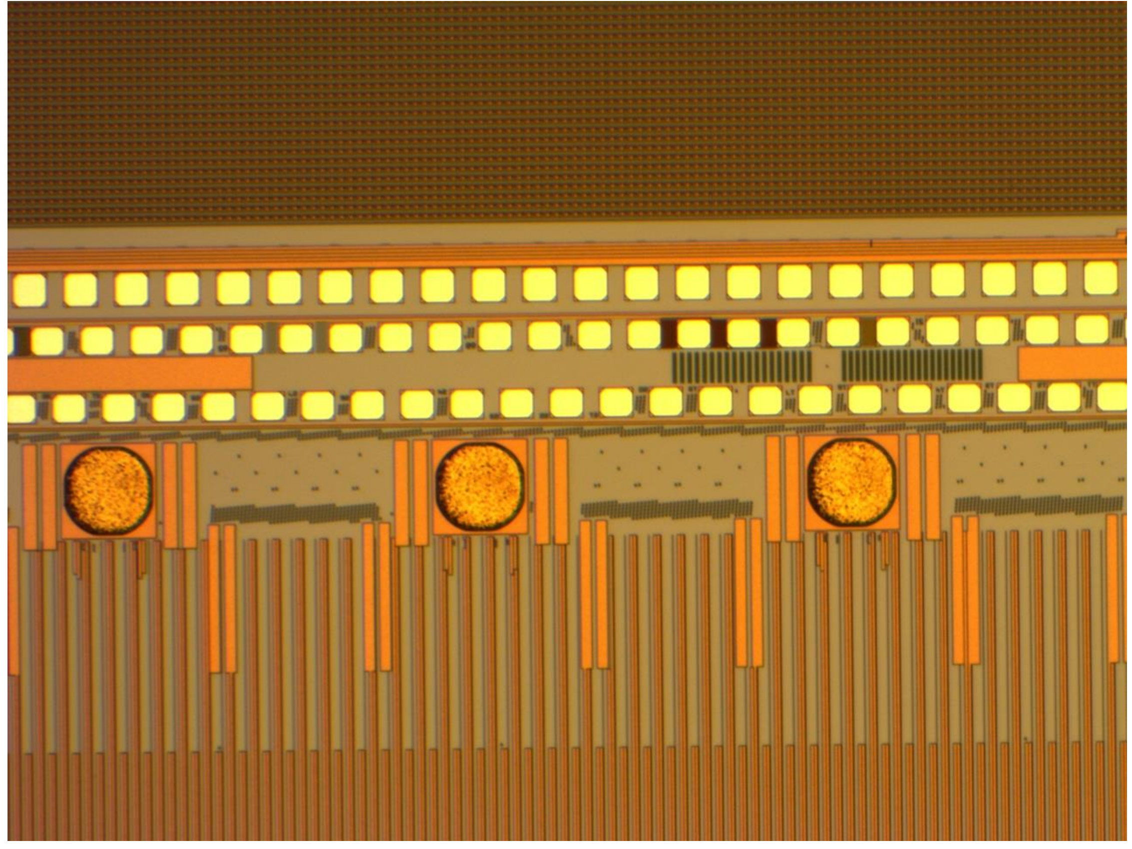
Transport time
3-4 days



Ni/Au plating

1 ITS2 pad wafer (8”) returned from plating at PacTech

Mask was applied to cover all areas except pALPIDEfs contacts, visual inspection before DBG:



Ni/Au plated ITS2 padwafer

Wafer sent for DBG – partially lost due to mishandling at the grinder.
Remaining dies will be delivered beginning of the week.

QA of this processing step needs to be defined, e.g:

- Visual inspection
- Solder test
- Height control (5 um Ni, 50 nm Au)

Ni/Au Plating – Next Steps

1**. Solder test** of chips from first wafer plated by PacTech

2. Next **2 wafers (ITS2 CMOS)** expected to be delivered back from PacTech end of June → visual inspection, DBG, solder tests

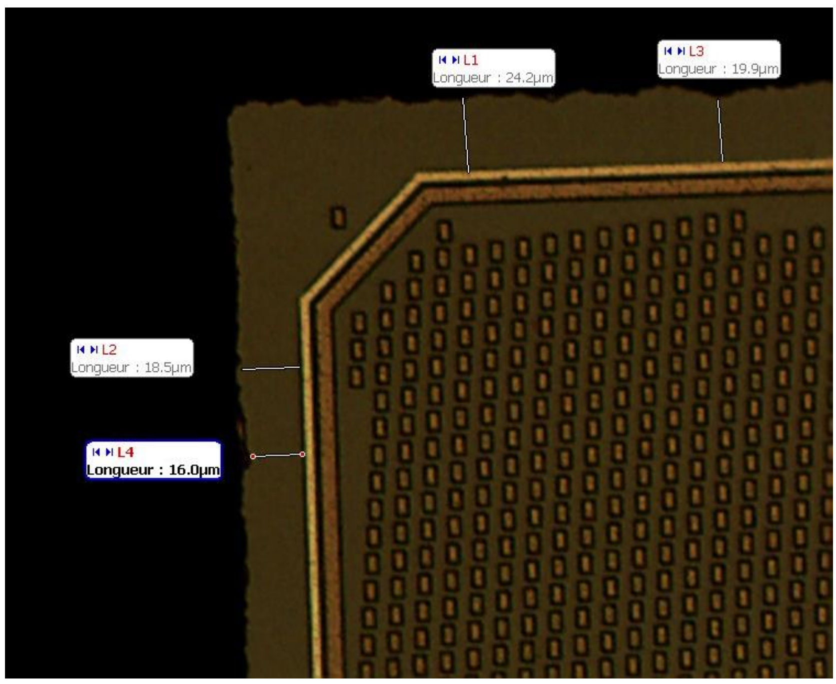
3. Preparing **market survey** for Ni/Au plating:

- Pre-meeting with purchasing officer (June)
- Aiming to complete market survey by the end of summer
- Should be completed before receiving new wafers later this year

Thinning & Dicing

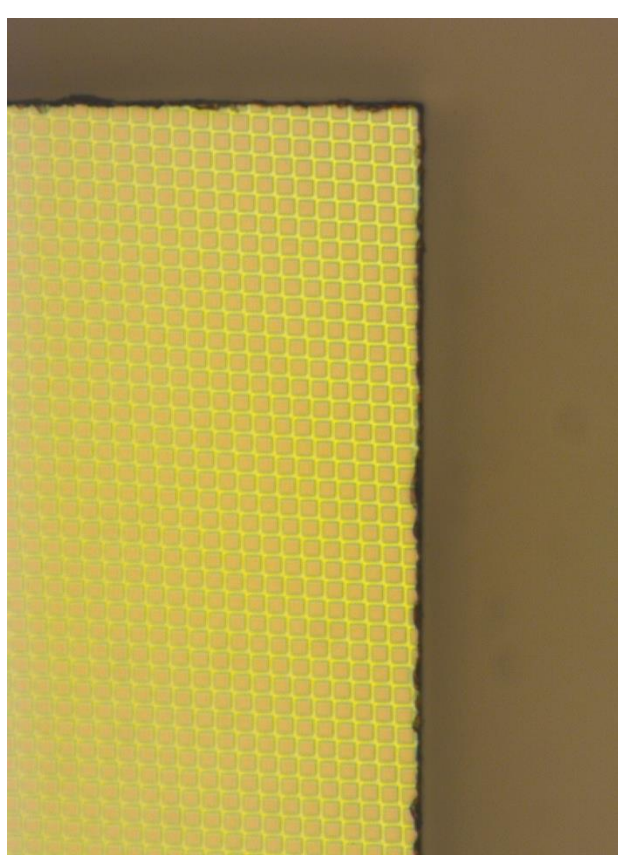
Definition of the criteria for thinning and dicing:

- Thickness: 50 um +/- 5 um
- Max. extent from seal-ring: +/- 30 um (20 um?)

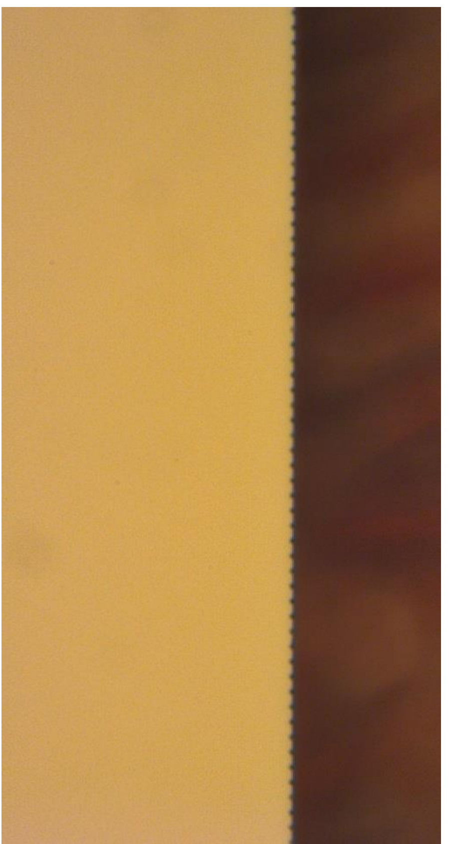


CMOS wafer

Blank wafer



ER2013 wafer
Diamond wheel dicing
(2000 mesh wheel)



Blank wafer
Laser diced by STARS
(front view)

Blank wafer
Laser diced by STARS

Stars Microelectronics (Thailand) Public Company Limited

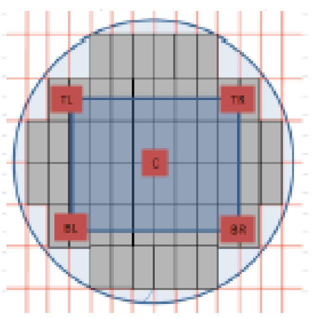
- Stars process flow

"Five STARS Customer Satisfier"

Stars Microelectronics (Thailand) Public Company Limited

- Product criteria control and result Stars Dummy.

Position	Criteria control		
	Wafer Thickness (50±5 μm.)	Die size X (3.00±0.004 cm.)	Die size Y (1.500cm.±0.004cm.)
TL	48.181	2.9998	1.4999
TR	50.188	3.0004	1.4996
C	50.184	3.0004	1.4997
BL	49.184	3.0005	1.5000
BR	50.941	2.9998	1.5000
Min	48.181	2.9998	1.4996
Max	50.941	3.0005	1.5000
Average	49.7356	3.0002	1.4998



Measurement position

- The Thickness requirement : 50±5µm. → Meet spec requirement.
- Die size X,Y requirement : X=3.0,Y=1.5±0.004cm.→ Meet spec requirement.

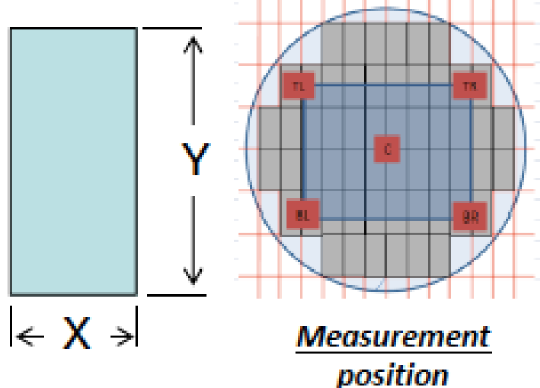
Remark : Test Saw 2 wafer and sort 1 wafer for measurement.

Stars Microelectronics (Thailand) Public Company Limited

- Condition and Laser saw result.

Process condition.
▪Reference STARS condition Laser Saw Products.

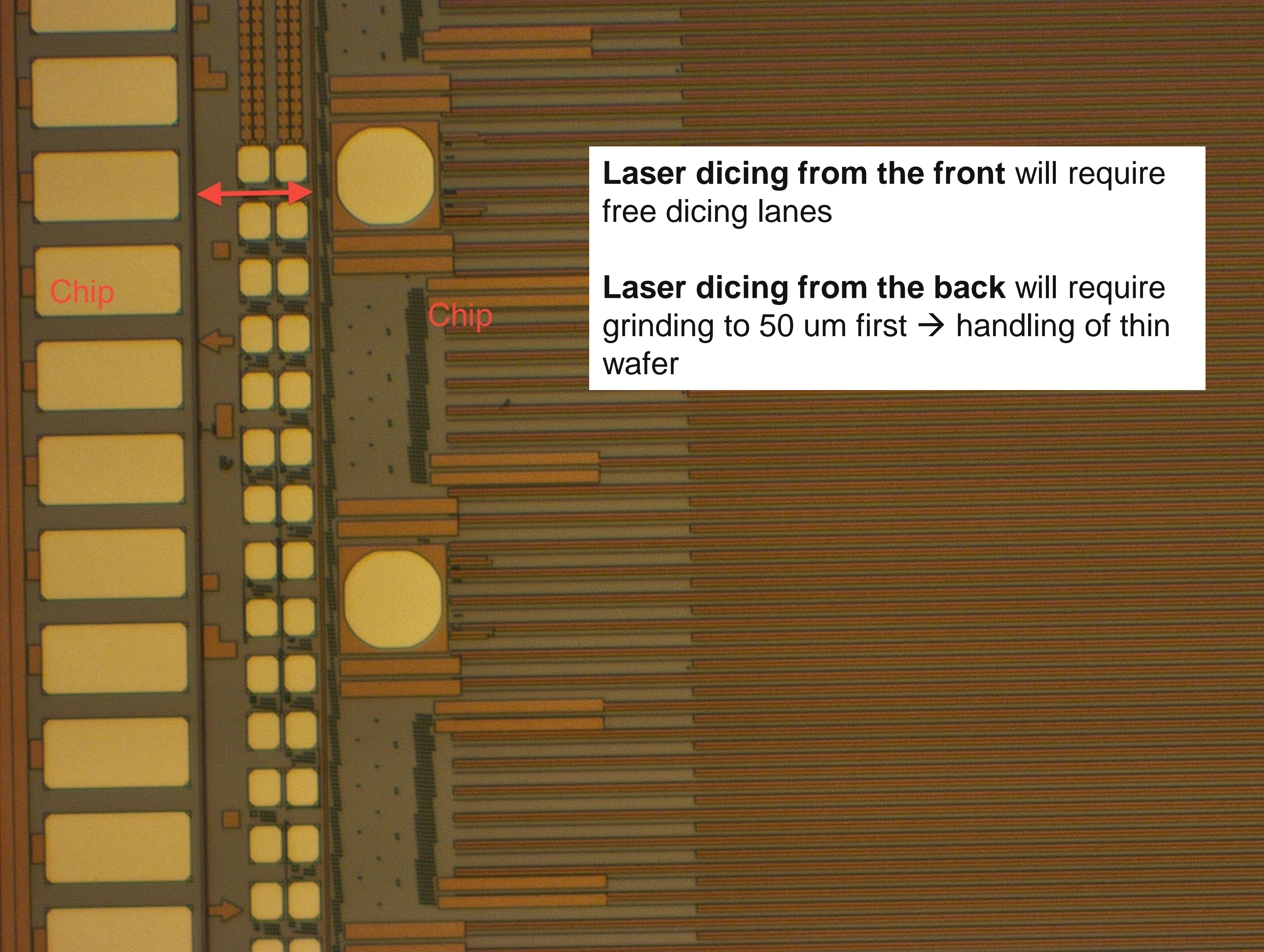
Result.
▪Die size X=3.0±0.004cm.(2.996~3.004cm.)
▪Die size Y=1.5±0.004cm. (1.496~1.504cm.)
➔ Meet spec requirement



Measurement position

No.Wafer	Die size Position	Die size X=3.0cm.,Y=1.5cm. (Spec ±0.004 cm.)					*Min*	*Max*	*Average*
		Center	Top left	Top right	Bottom left	Bottom right			
1	X	1.500	1.500	1.500	1.500	1.500	*1.500*	*1.500*	*1.500*
	Y	3.000	3.000	3.000	3.000	3.000	*3.000*	*3.000*	*3.000*
2	X	1.500	1.500	1.500	1.500	1.500	*1.500*	*1.500*	*1.500*
	Y	3.000	2.999	3.000	3.000	3.000	*2.999*	*3.000*	*3.000*
3	X	1.500	1.500	1.500	1.500	1.500	*1.500*	*1.500*	*1.500*
	Y	3.000	2.999	3.000	3.000	3.000	*2.999*	*3.000*	*3.000*

Measurement criteria : Measuring Hi-power micro scope 50X. and counter display.


Laser dicing from the front will require free dicing lanes
Laser dicing from the back will require grinding to 50 um first → handling of thin wafer
Chip
Chip

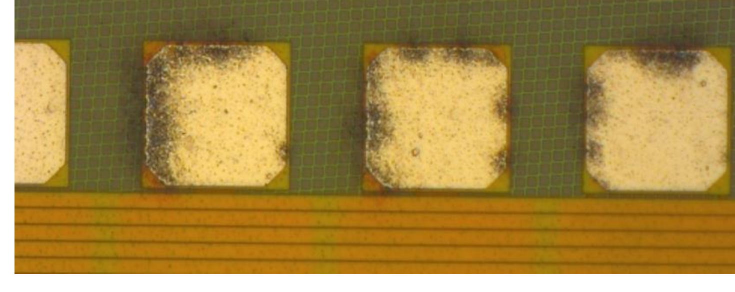
Thinning & Dicing Status and Next Steps

- **STARS** is preparing a pick-up tool: news beginning of July → test dicing of real CMOS processed pad wafer?
- Asked offers from **DISCO** for blade and laser dicing: die picking not provided – evaluating
- **Rockwood** investigated grinding accident with ITS2 pad wafer: origin found
- Need to prepare **market survey** as for the plating: meeting with purchasing office in the next weeks.

Wafer QA after processing

Main task: **Basic visual inspection on the wafers, i.e. the connection pads**, prior to

- Post-processing and/or
- Thinning and dicing



Rockwood carried out visual inspection on recent wafers following SEMI standard: provide pictures and summary report for each wafer.

Need to define procedure for production (cost, time, etc.).

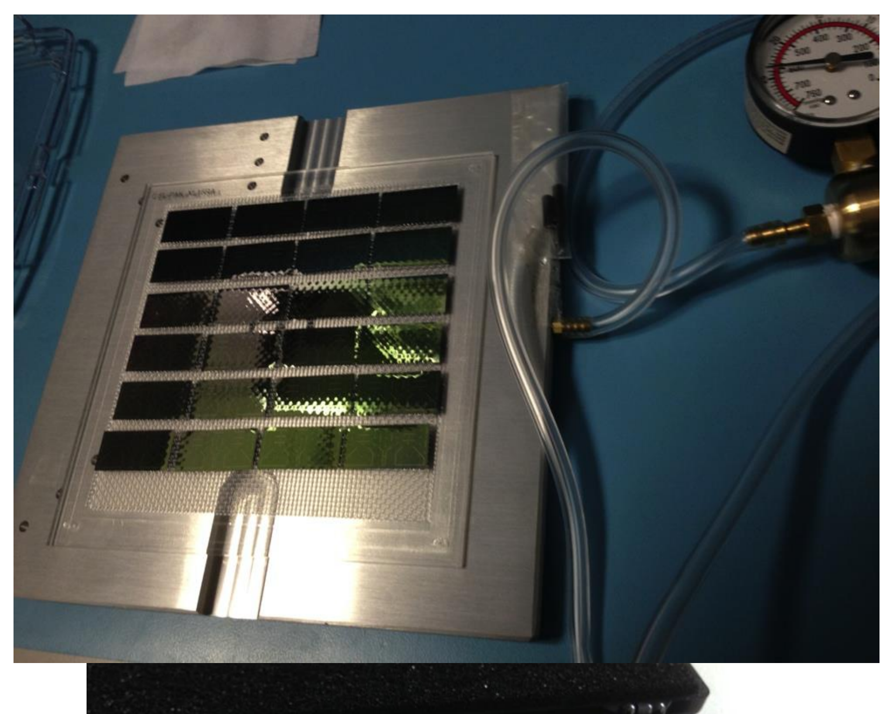
Transport and Storage

Planned transport test involving a number of institutes: i.e. IPHC, Pusan, Liverpool, …

Prepared **gel-pak boxes** with 50 um dummy chips and 50 um thick STAR HFT pixel chips

ALICE

Chip Transport



- Used identical large gel-paks to return pad chips (TMEC) from Rockwood (2 x 24 chips)
- **Chips cannot be removed applying vacuum**
- Cut out chips freed from gel by using HF-acid – limited use due to oxidation on the pads

Chip Transport

Discussion with Rockwood ongoing to identify whether the problem is due to one of the processing steps.

Short term solution: ordered and received foam boxes

Alternative solutions:

- Foam box: needs improvement (flakes, dust, counter-pieces)
- Waffle packs: requesting offer, investigating how to fix chip in the compartment

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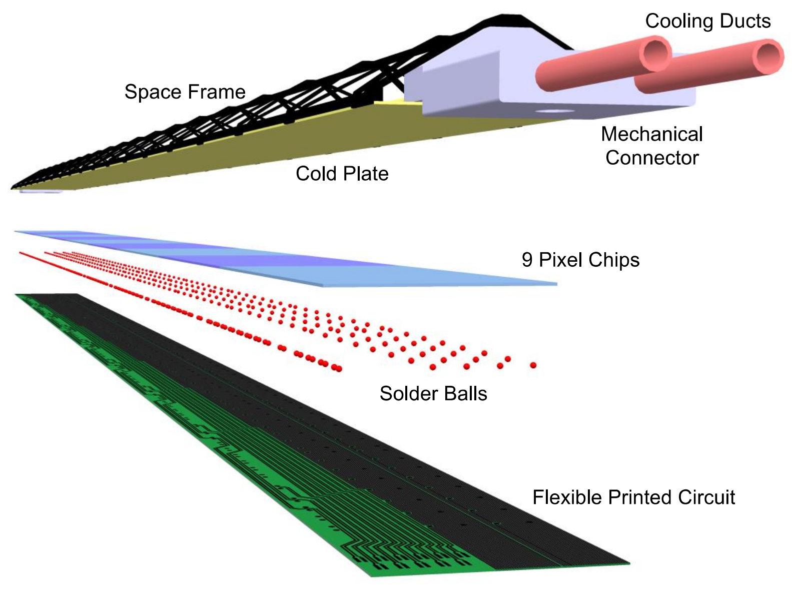
Interconnect R&D

- Direct flux-free laser soldering on silicon chip
- Solder balls (diameter 200 um)



Interconnection R&D

Number of single chip assemblies soldered with very good yield:

	Sample	Flex	Poly thickness	chip	contact	gas	daisy-chain resistance
1	04022014-SA1	Test 15, new Ni/Au	75 µm	TMEC new Ni/Au	50/50	N/H	125 Ω
2	04022014-SA2	Test 15, new Ni/Au	75 µm	TMEC new Ni/Au	50/50	N/H	115 Ω
3	07022014-SA1	Test 15, new Ni/Au	75 µm	TMEC new Ni/Au	50/50	Vacuum	160 Ω
4	10022014-SA1	Test 15	75 µm	TMEC new Ni/Au	50/50	Vacuum	84 Ω
5	10022014-SA2	Test 15	75 µm	TMEC new Ni/Au	50/50	Vacuum	80 Ω
6	12022014-SA1	Test 11 new production	50 µm	TMEC new Ni/Au	50/50	Vacuum	94 Ω
7	12022014-SA2	Test 11 new production	50 µm	TMEC new Ni/Au	50/50	Vacuum	74 Ω
8	13022014-SA1	Test 11 new production	50 µm	TMEC new Ni/Au	50/50	Vacuum	60 Ω
9	13022014-SA2	Test 11 new production	50 µm	TMEC new Ni/Au	50/50	Vacuum	46 Ω
10	13022014-SA3	Test 11 new production	50 µm	TMEC new Ni/Au	50/50	Vacuum	59 Ω
11	19022014-SA1	Test 11 new production	50 µm	TMEC new Ni/Au	48/50	Vacuum	
12	24022014-SA1	Test 11 new production	50 µm	TMEC 3 produc	50/50	Vacuum	39 Ω
13	26022014-SA1	Test 11 new production	50 µm	TMEC new Ni/Au	49/50	Vacuum	

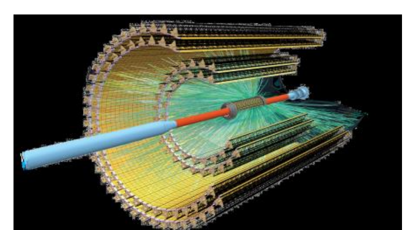
650 solder contacts
3 failures (understood)

Can **correlate good soldering quality with integrated laser power** value
→ no need to cut the sample → first step in defining quality procedure

Interconnection R&D

- **2 IB modules built with 50 contact pad chips (TMEC)**
- Alignment done fully manually
- Vacuum box leaking (missed 7 contacts out of 450 due to oxidation)
- Daisy chain resistance value ok

Next: waiting for plated chips to assemble pALPIDEfs and pad chip modules



Al-FPC design

A. Di Mauro
B. A. Junique

Openings for chip position measurement

1 mm

1 mm

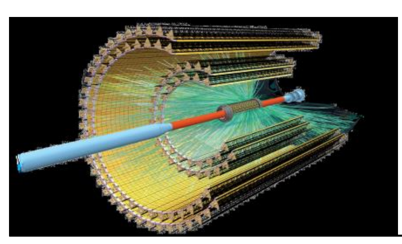
0.4 mm

1 mm

1 mm

1 mm

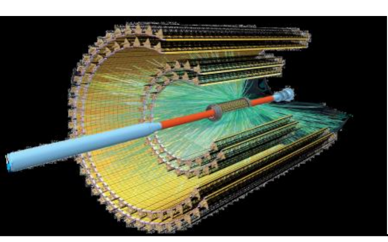
0.4 mm



Al-FPC manufacturing

Al coating	Etching	Status
LERMPS (F)	Chemical etching (CERN - R. De Oliveira)	• Al quality OK: roughness 0.39 μm, surf. index 1.06, resistivity ~ 0.22 Ω/cm • Machine capability (guaranteed Al layer homogeneity): 0.1x1 m^2 • Delivered 2 samples (9-chip): 1 daisy chain + 1 with signal tracks
DEPHIS (F)		• Al quality not OK: too porous (roughness 0.62 μm, surf. index 1.2) and too high resistivity ~ 0.7 Ω/cm • Investigation is ongoing, setting up of machine to reproduce LERMPS parameters (machine capability: 0.5x1.5 m^2)
FHR (DE)		• Best Al quality: roughness 0.14 μm, surf. index 1.007, resistivity ~ 0.16 Ω/cm • Issue with presence of fibres and particles embedded in Al layer under investigation • Machine capability: 0.5x1.6 m^2 • Delivered 2 samples (9-chip): 1 daisy chain + 1 with signal tracks
IREIS/HEF (F)		• Leader "surface engineering" French company • Machine capability 4 x 1x0.30 m^2 • Al coating tests this week

- LERMPS baseline solution, mass production affordable (~ 18 batches of 6 FPC)
- Tests with other companies driven by R. De Oliveira to find alternative supplier, very often LERMPS delivery time quite long



Laser etching (Swiss Micro Laser)

- Optimized laser parameters
- Delivered 9-chip FPC prototype (on old DEPHIS foil)

Mass Test – Probecard Preparation

Probecard for the pALPIDEfs prepared by Youngil Kwon (Yonsei):

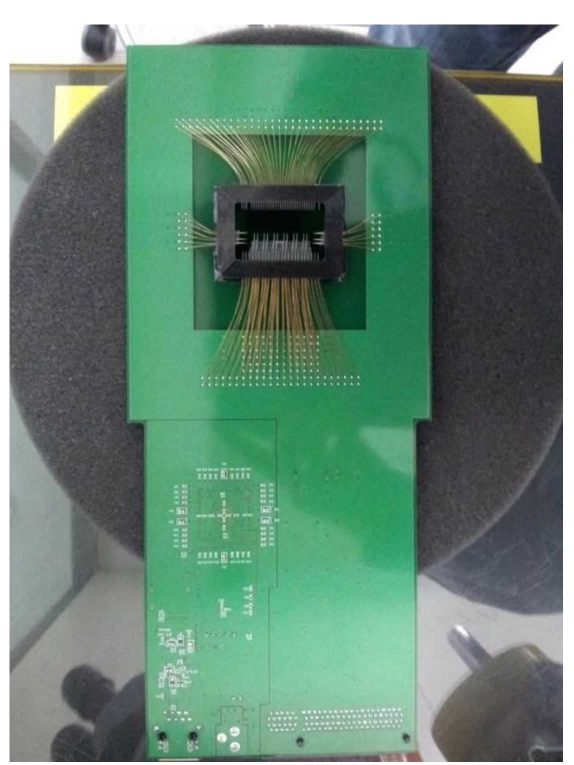
- Double needles for the contacts to check contact quality automatically
- Complex probecard needle matrix with double needles reaching into the contact window from 4 sides.

Card was delivered at CERN early May:

- Mechanical test on prober
- Contact test on ITS2 CMOS wafer (pad wafer and real CMOS wafer)
- **Now:** connecting to pALPIDEfs test system – work ongoing

2. Probe Card Pin Contact Analysis

2.1 Probe card Contact



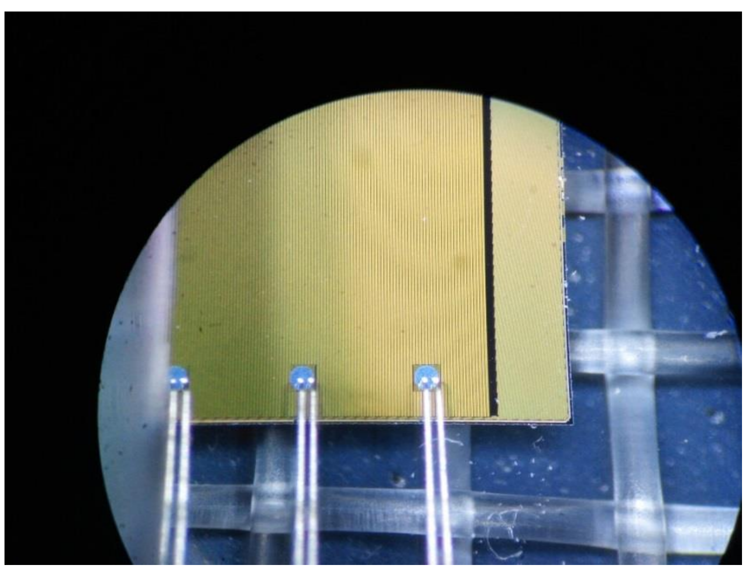
206pin Top/Bottom

Youngil Kwon

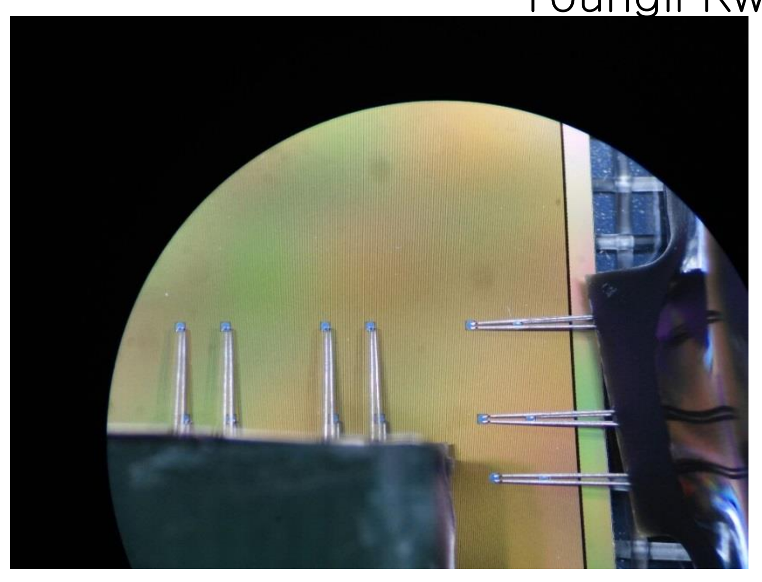
2. Probe Card Pin Contact Analysis

2.2 Probe card Contact

Youngil Kwon



Wafer 우측 하단向 Position



Wafer Center 우측向 Position

Pin 數	206pin(1Pad 2Pin)	
Pad Size	224*224um	Pad Pitch 874um
Needle thickness	80um	
Band Length	290~310um	

Pictures from mounting test at CERN

As

Summary

- **Blank wafer** status: wafers for next runs procured, work on QA ongoing
- **Interconnect R&D:** spTAB bonded pALPIDEfs assembly in preparation, waiting for plated chips for laser soldering of modules
- **Ni/Au plating of present wafers ongoing**
- **Dicing and thinning** of plated wafers in the next weeks
- **Probe-card** installed at CERN prober; connection tests with pALPIDEfs test system ongoing
- Investigations and alternatives for **chip transport** boxes ongoing

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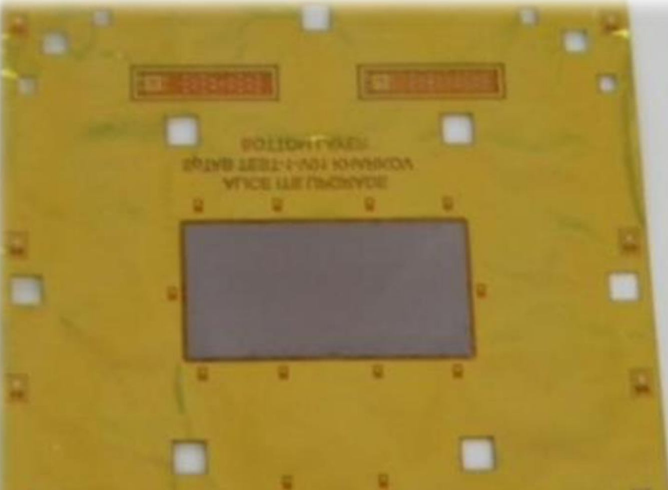
Assembled prototype of the FPC

View from FPC side

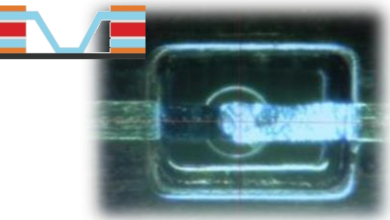
View from chip side



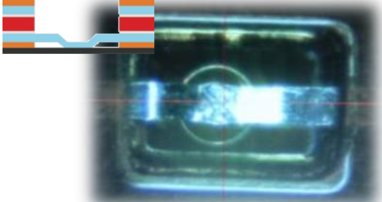
FPC prototype with mounted chip in TAB-70 technological frame

Different types of bond joints

Top layer-to -chip



Bottom layer-to-chip



Interlayer connection

Assembled FPC prototype was electrically and visually tested -results are OK!

(all 60/60 TAB joints are OK, chip is OK).

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