WP1 - Common Microelectronic Technologies for HEP

A. Marchioro /PH-ESE

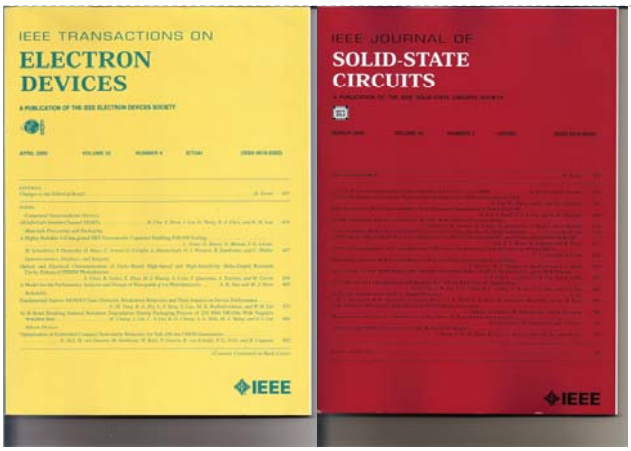
Agenda

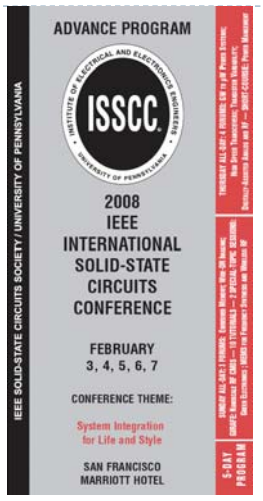
- Context of the "Technology" project
  - Review of past activities
- Plans for the future
  - Proposed objectives for next generation
  - Challenges
- Summary

The scope and the problem

- Microelectronics is a technology with enormous and perhaps unique potential for the construction of integrated detectors and systems. Think about:
  - Multi-Million elements Pixel detectors
  - 2-300 m^2 Silicon Trackers
  - New low-cost gaseous detectors
  - Massive calorimeters
- … but:
  - Has very high entrance fees
  - Can be risky
  - Requires strict and structured design organization and methodology
  - Requires years of continuous investment and training in tools and people
  - Is not driven by HEP

The references here are:





What is needed to design chips for HEP?

- Given the costs, risks and difficulties associated with new microelectronic technologies, a common approach is necessary to:
  - Qualify and select technologies
  - Specify, use and re-use common design blocks
  - Share expertise and resources in the area of microelectronics technology
  - Share tools, prototype and production costs
  - Maintain a minimal critical mass around projects

ASIC technologies for the community

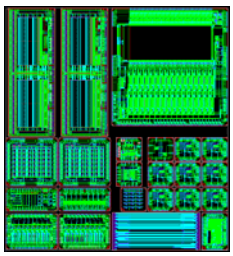
- ¼ µm CMOS introduced by CERN-MIC after qualification in 1999 as alternative to expensive "military grade" technology
- Qualification and validation of technology was done at CERN with internal resources
  - Radiation measurements
  - Radiation resistance monitoring
- Development of special add-ons:
  - Modeling for simulation of enclosed transistors
  - Extraction rules for modified layout
  - New digital library
  - Design support package
- Technology shared with external users from 2000

Human resources in Microelectronics at CERN

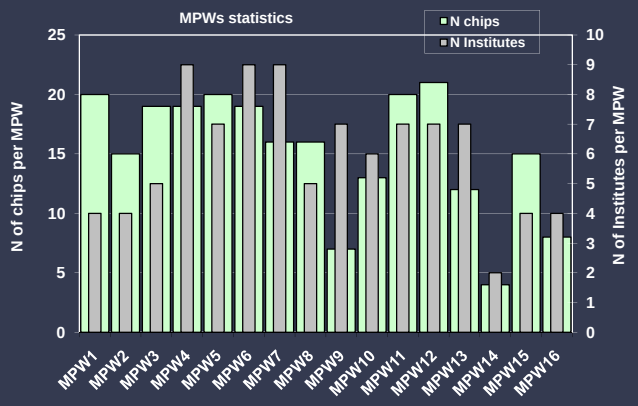
- One section in ESE group:
  - 12 Design engineers (mostly EE)
  - 13 Students/Fellows
    - Contracts: > 6 months, < 3 years
  - 3 Technicians + 1 Software Support

Some HEP design labs

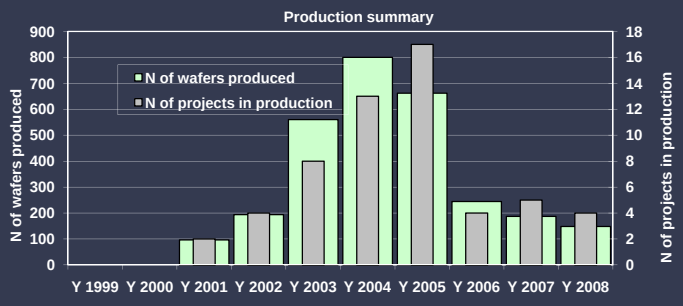
- France:
  - Orsay, Marseille, Strasbourg, Saclay
- Germany:
  - Bonn, Heidelberg, Munich, Desy
- UK:
  - RAL, Liverpool
- Italy:
  - Bari, Torino, Cagliari, Firenze, Padova, Pisa
- Netherlands:
  - NIKHEF
- Poland:
  - Warsaw, Cracow
- US:
  - Berkely, Penn-State, Columbia, Ohio State, FNAL, SMU

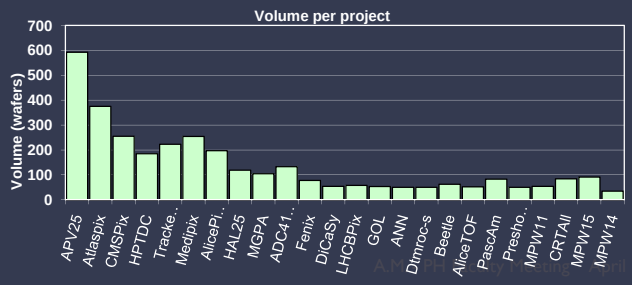


Multi-Project-Wafer (MPW) activities

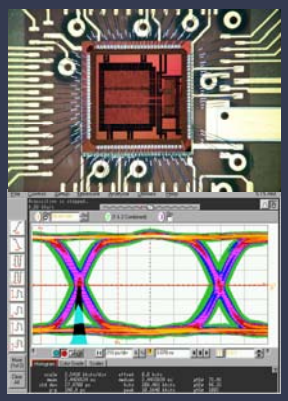


Support Activities: Submissions



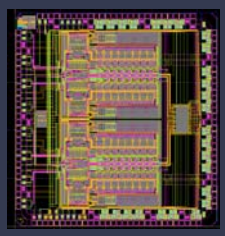


Microelectronics Projects @ CERN

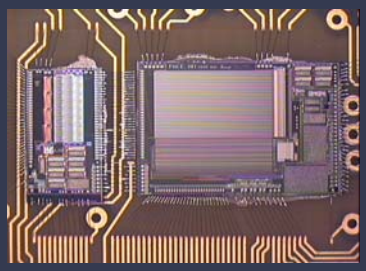


GOL: 1.6Gb/s serializer

K-Chip



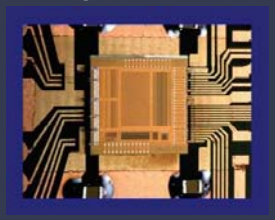
4*40 Ms/s ADC



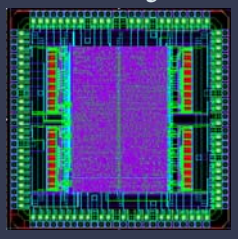
PACE: Pre-shower readout

TTCrx

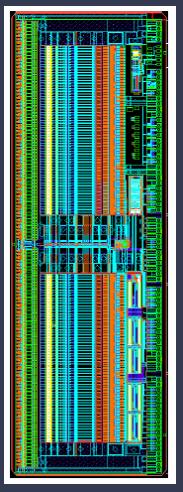
Projects from HEP community



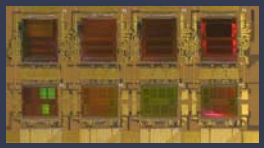
APV25: RAL & IC



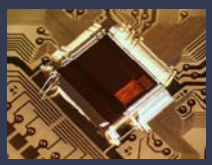
Carlos: INFN Bologna



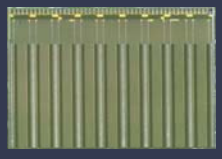
HAL25: Strasbourg



Pascal &Ambra: INFN To



Beetle: Heidelberg



Atlas Pixel: LBL

Plans for the future

How to reach our common objectives

- Facilitate adoption of advanced technologies by sharing expenses
  - Offer common technology platform(s)
  - Provide shared tools and library blocks
- Provide a central "strong" design group that can work as "example"
- Organize common training and information sessions
  - Specific Microelectronics User Group (MUG) meetings (also attached to annual TWEPP event)
  - Piggy-back on numerous European initiatives
    - Training funds are dearly needed !!!
- Present a common interface to industry
  - Each HEP Institute is too small to attract any attention from the big industrial guys
  - Only together we can reach a critical mass to "get noticed"

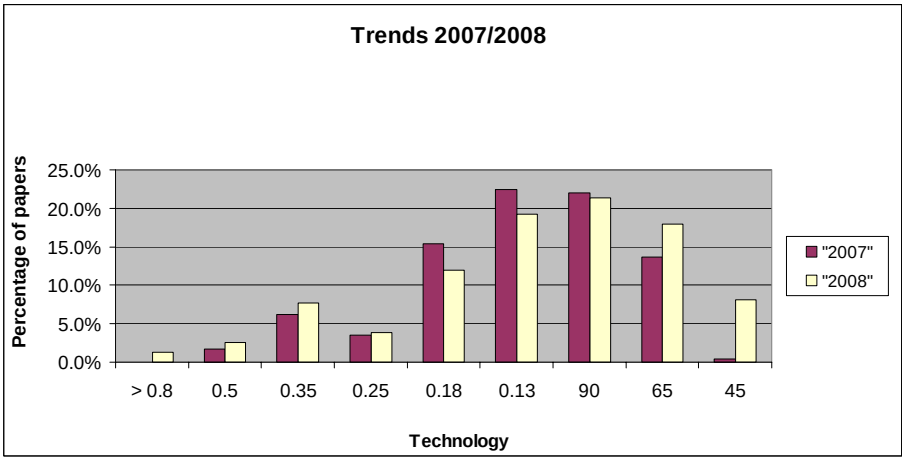
What do these nm mean anyway?

Lithography	Micros (# trans / MHz)	DRAM Memories (for a ~100 mm2 die)	Devices
1.0 um	386DX (270K / 3M)		
0.6 um	486DX4 (1.6M / 100)	16 Mb	
0.35 um	Pentium II (7.5M / 233)	64 Mb	
0.25 um	Pentium III (9.5M / 500)	128 Mb	
130 nm	Pentium M (77M / 1600)	512 Mb	
90 nm	Pentium 4 (125M / 3000)	1Gb	
65 nm	Core Duo (>1B / 2200)	4 Gb	

Technology Support for the future

- FE electronics for key LHC upgrades and SLHC will be based at least on 130 nm technology and below
  - To ameliorate detectors, substantial improvements are necessary in the power/ch characteristic of FE ASICs
  - New detectors become conceivable when better technologies become available.
    - Examples:
      - New ADCs with very low power consumption (100x better) allow radically new calorimeters
      - A Gigatracker in just not conceivable in anything less than 130 nm
- Current CERN responsibilities
  - Interface (technical and commercial) with foundry supplier
    - Contract for entire community
  - Organization of common and dedicated submissions
    - Share mask costs whenever possible
  - Technical support
    - Design kit for full design flow: analog and digital
    - Library
    - Tools
    - Design assistance

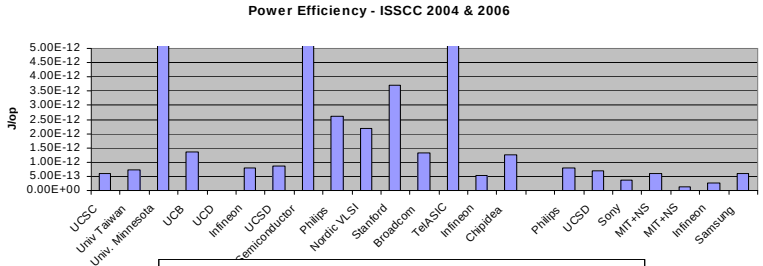
Technologies at ISSCC



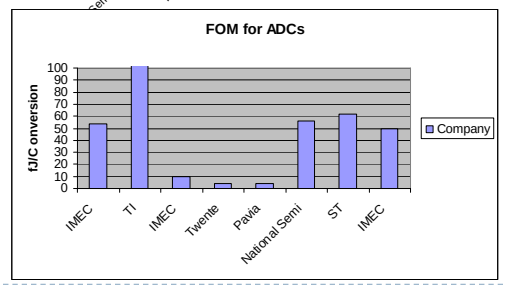
ADC example

- Terminology:
  - Figure of merit: Energy necessary for one conversion
  - Example: An 11.2 effective bits ADC at 40 Msamples/sec with 100mW has a FOM of: 1.06 pJ/Conversion

AD Converters Evolution



2008



If 130 nm is good, why is 65 nm better?

- Take a calorimeter with 15 M channels, where 14 bits (13 eff bits) at 100 MHz samples are desired:
- Today's very good ADC (0.25 um) gives:
  P_{tot}= 1.5 10^7 * 1pJ/C * 2^{13} * 10^8 = 12.3 MW
- Tomorrow's ADC (65 nm) can give:
  P_{tot}=1.5 10^7 * 50 fJ/C * 2^{13} * 10^8= 0.6 MW

Challenges

- Large chips will require to extend design efforts across different Institutes
  - ASIC designs can't be fixed after manufacturing
    - "Perfect" coordination needed at design time
    - Synchronization of tools, libraries, methodologies
- Radiation Hardness is required for (S)LHC but this "technology" is considered as "a military asset" in some countries
  - Very delicate negotiations are ongoing with the US in order to allow unimpeded participation in scientific research programs for our US collaborators

How is the WP money going to be spent?

- Fund common technology evaluation and qualification
  - One mask set
    - 130 nm ~ 350K$
    - 90 nm ~ 600K$
    - 65 nm ~ 1M$
- Provide essential central services for CERN and the community
  - MPW organization and coordination
  - Design tools and training
  - Information sharing
- Common instruments
  - IC Tester (~600K$)
- Design IP blocks of common interest (1 FTE assigned at CERN)
  - Validated and characterized digital library
  - Analog blocks
  - Digital block
  - IO blocks

Summary

- μ–electronics is a key enabling technology for modern detectors
- The reference environment in this technology is industry and (unfortunately) not the HEP physics labs
  - We need to have well trained people capable of speaking industry's language
    - to maintain respectability in their world
    - to translate their technologies into useful HEP applications
- HEP must maintain a few strong labs with enough critical mass to
  - Provide tools and technologies for the community
  - Serve as catalyzer for common projects
  - Be accepted as reliable (and commercially non-negligible) partners by industry