Radiation-Hard Optical Link for Experiments

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Outline

- Introduction
  - LHC upgrade (SLHC)
  - The Past Diversity of Link types
  - Optical Link Project Objectives
  - Project organisation
- Optical Link Components - Versatile Link
  - Lessons from currently-deployed links
  - Commercial Transceivers
  - The Versatile Transceiver
- The GigaBit (GBT) Transceiver chip set
  - GBT link architecture
  - The GBT chip set
  - The GBT “collaboration”
- Summary

LHC upgrade (SLHC)

- Increased luminosity implies:
  - More Data to Read out
    - More complex DAQ/TTC/SC systems (higher bandwidth required)
  - Higher radiation doses
- Higher bandwidth links required at (if possible):
  - No radiation-length penalty due to increased material
  - No penalty on power consumption
- The viable solution is to:
  - Increase and optimize the use of the bandwidth available per optical link
    - This increases the bandwidth available to the user
    - Reduces the number of optical fibre links
- Benefits:
  - Focusing the engineering effort on a common solution
  - Lower mass overall due to link components
  - Possible overall reduction of power consumption
  - Lower installation and maintenance costs

Link Diversity - Historical Perspective

- Running HEP experiments takes 3(+) systems:
  - Data Acquisition (DAQ) systems
  - Timing, Trigger and (fast) Control (TTC) system
  - Slow control (SC) systems
- Data transmission links for these systems have different requirements
  - E.g. speed, latency, number
- In the past specific data transmission links have been custom developed for each of these applications:
  - Multiple Driver/Receiver ASICs
    - TTCrx (10k installed)
    - GOL (30k installed)
    - CCU (9k installed)
    - LLD (40k installed)
  - Multiple Optical Link Types
    - TTC
    - ATLAS, CMS have 1 per subdet
    - LHCb achieved single type
    - ALICE has 2-3 types
    - Overall ~100k links installed
- This was justified by:
  - The specificity of the application being targeted
  - Technological limitations

Optical Link objectives

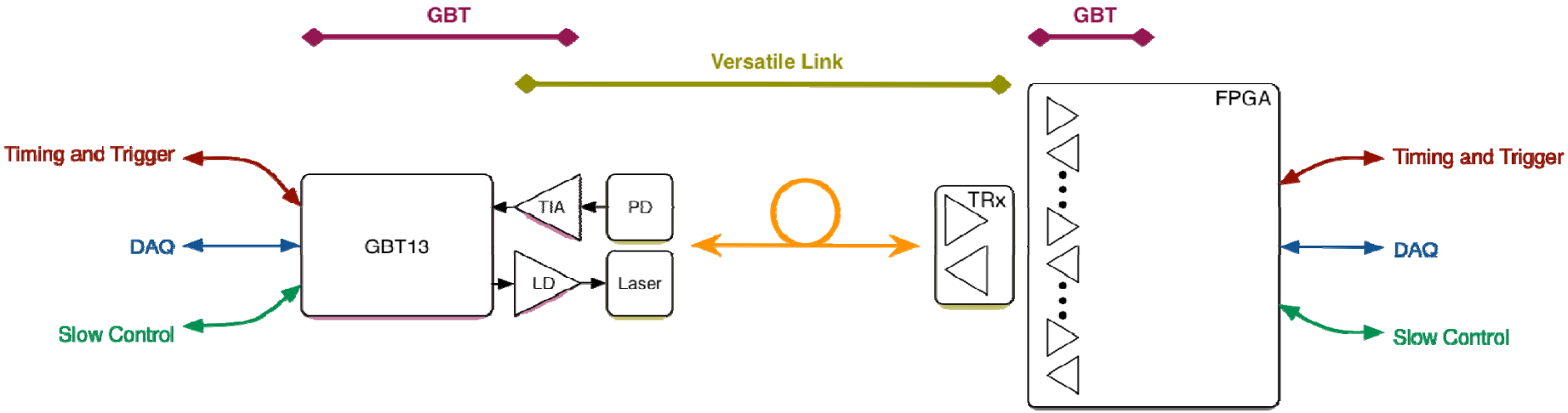
- The Optical Link project aims to develop ASICs to enable a general purpose optical-fibre link which can simultaneously serve:
  - DAQ *and* TTC *and* SC
- To partner these ASICs it also aims to develop a radiation-hard optical transceiver that can be used with the two most popular installed optical fibre types:
  - Multimode fibre at 850nm and Singlemode at 1310nm
- The maturity of today's Optoelectronics and CMOS technologies enables such a development
- There are several obvious advantages:
  - R&D effort concentrated on a single project
  - Single type of components needs to be:
    - Developed
    - Qualified
    - Produced
    - Installed
    - Maintained
  - Reduction of the overall number of optical links installed:
    - The channel bandwidth is increased
    - DAC/TTC/SC data transits over a single fibre.
- A common digital link development has been acknowledge as an appropriate common project by the electronics coordinators on the ACES of the for LHC experiments

DG white paper “Work Package 3-1”

- “Work Package 3-1” defined in the “DG White Paper”
  - WP3-1: Radiation Hard Optical Link:
    - Objective:
      - Development of an high speed bidirectional radiation hard optical link
    - Deliverable:
      - Tested and qualified radiation hard optical link
    - Duration: 4 years (2008 – 2011)
    - Budget:
      - 2008 approved
      - Forecast for the coming years

Project Organisation

- Two Major Themes
  - The opto-electronics, its radiation and functionality testing plus packaging
    - This work is carried out in the context of the Versatile Link
    - Project Leader: Jan Troska
  - The ASIC design, verification and packaging
    - This work is carried out in the context of the GBT
    - Project Leader: Paulo Moreira



On-Detector
Custom Electronics & Packaging
Radiation Hard

Off-Detector
COTS
Custom Protocol

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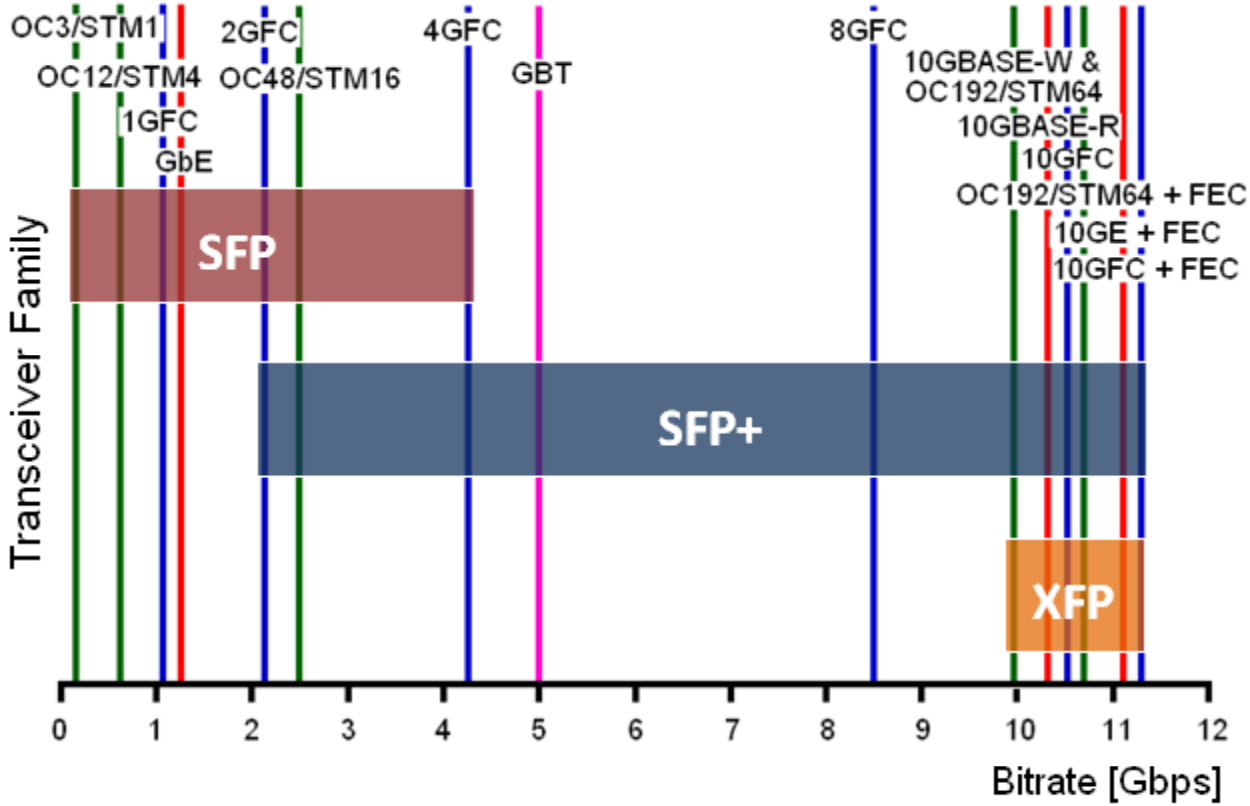
Optoelectronic Link Components

- Lessons Learned from current systems
  - Currently installed systems (ATLAS & CMS) are of high quality
    - Dead channels below the per mille level, mostly due to broken fibres
    - Avoid pigtailed devices in future
  - Cost per link for the customized developments of ATLAS and CMS Trackers ~300CHF/link in spite of early claims of cheap links by some groups
    - Customization is costly - stick close to COTS designs
    - Major part of the cost is in the active components
  - Installation of on-detector components often carried out by technicians not trained in the handling of fragile fibres and miniature connectors
    - Stick to well proven and widely-used connector designs
- Thus our goal is to develop a transceiver based on a proven industrial design
  - Customizing only those aspects that are absolutely necessary
  - Leveraging packaging know-how of the optoelectronics industry

Commercial Transceivers

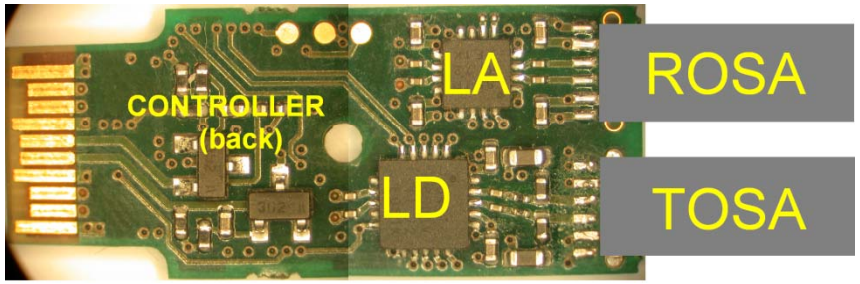
- COTS components target standardized data-rates used in Telecom and Datacom applications
  - Can we find such standards that meet our needs?

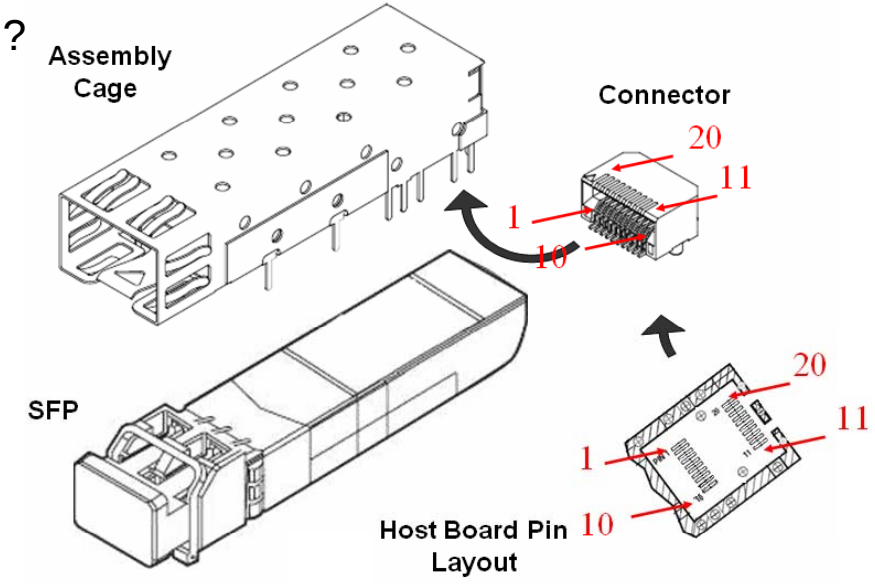
Standards
Ethernet
1GE: 1.25 Gbps
10GE (10GBase-W): 9.953 Gbps
10GE (10GBase-R): 10.3125 Gbps
10GE + FEC: 11.10 Gbps
Fibre Channel
1 GFC: 1.0625 Gbps
2 GFC: 2.125 Gbps
4 GFC: 4.25 Gbps
8 GFC: 8.5 Gpbs
10 GFC: 10.51875 Gbps
10 GFC + FEC: 11.3 Gbps
SONET/SDH
OC3/STM1: 155.52 Mbps
OC12/STM4: 622.08 Mbps
OC48/STM16: 2.488 Gbps
OC192/STM64: 9.953 Gbps
OC192/STM64 + FEC (G.975): 10.664 Gbps
OC192/STM64 + FEC (G7.09): 10.709 Gbps



From Commercial to Versatile

- From the previous picture, it looks the emerging SFP+ transceivers are worthy of attention
  - What needs to be customized?
  - Work with Industrial Partner





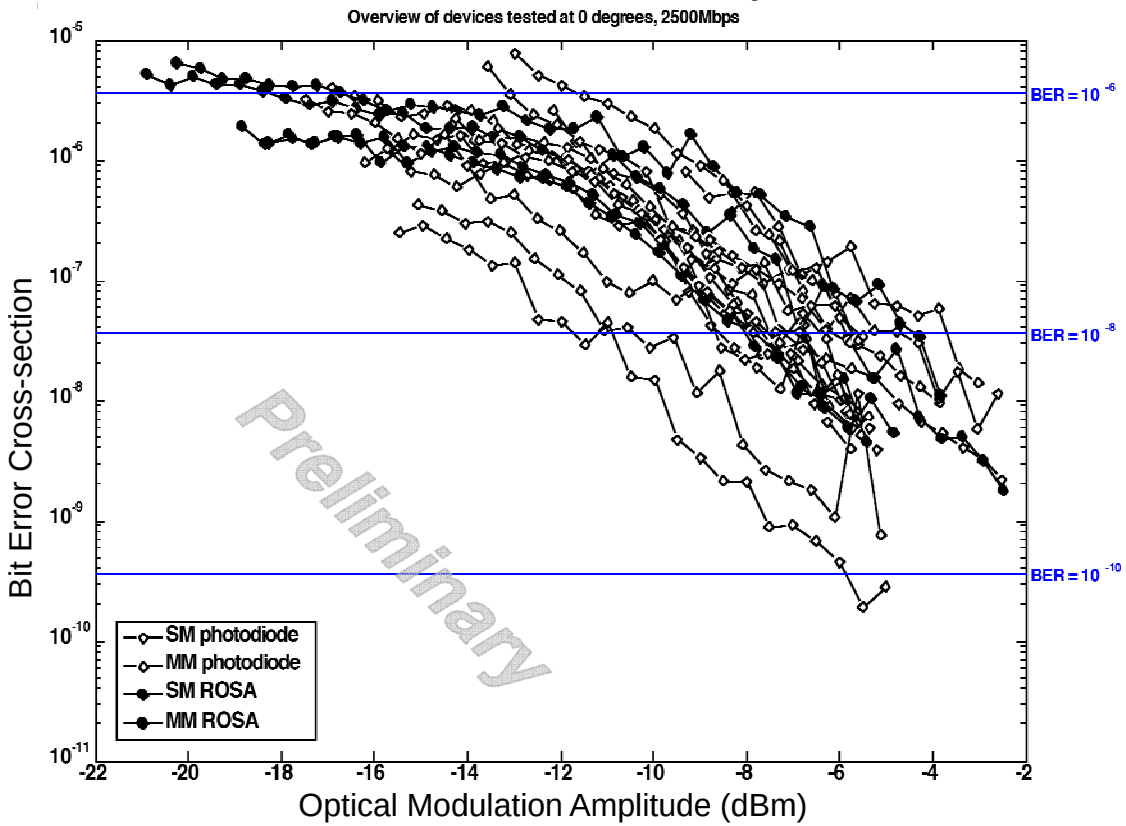
- Based on the (tentative) requirements, look at those items where commercial specs deviate
  - Radiation resistance - all ASICs, Lasers, Photodiodes
  - Magnetic field tolerance
  - Materials and dimensions
  - Low temperature operation

Versatile Transceiver Flavours

- Several currently installed systems may be constrained to re-use the fibres installed for LHC for SLHC
  - Installation has been a long and intricate process
  - Dismantling and replacing would impact on other services to systems not being upgraded
- This will require that the Versatile Transceiver be available finally in a number of flavours
  - For example:
    - Multimode 850nm
    - Singlemode 1310nm
  - Shortlist will be finalised as far down the road as possible to allow system designs to become fully mature

First Radiation Results: SEU Testing

- Expected Single-Event Upsets due to particle “detection” by Photodiodes used as optical link receivers to be a significant issue for high-speed links
  - Energy per transmitted bit decreases with increasing data-rate (and thus SEU sensitivity increases)
  - Carried out first survey of results in different devices in Dec.07



- 12 device types tested
- Similar results for almost all devices
- Confirmed that if Error-rates below 10^{-12} required for downlink then Error Correction is mandatory
- Measured Upsets lasting several bit periods for the first time

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  - GBT link architecture
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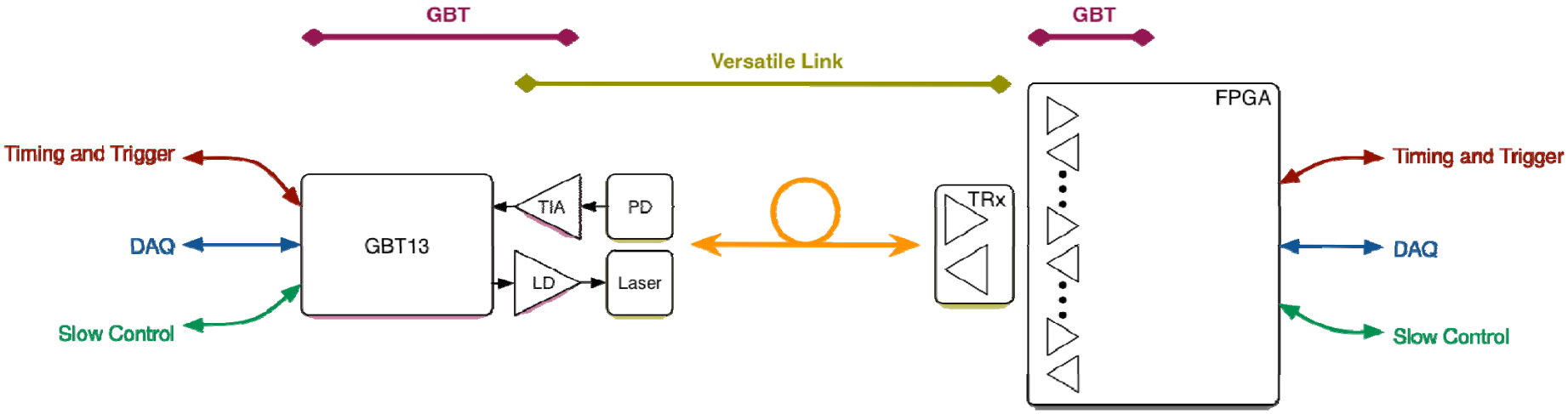
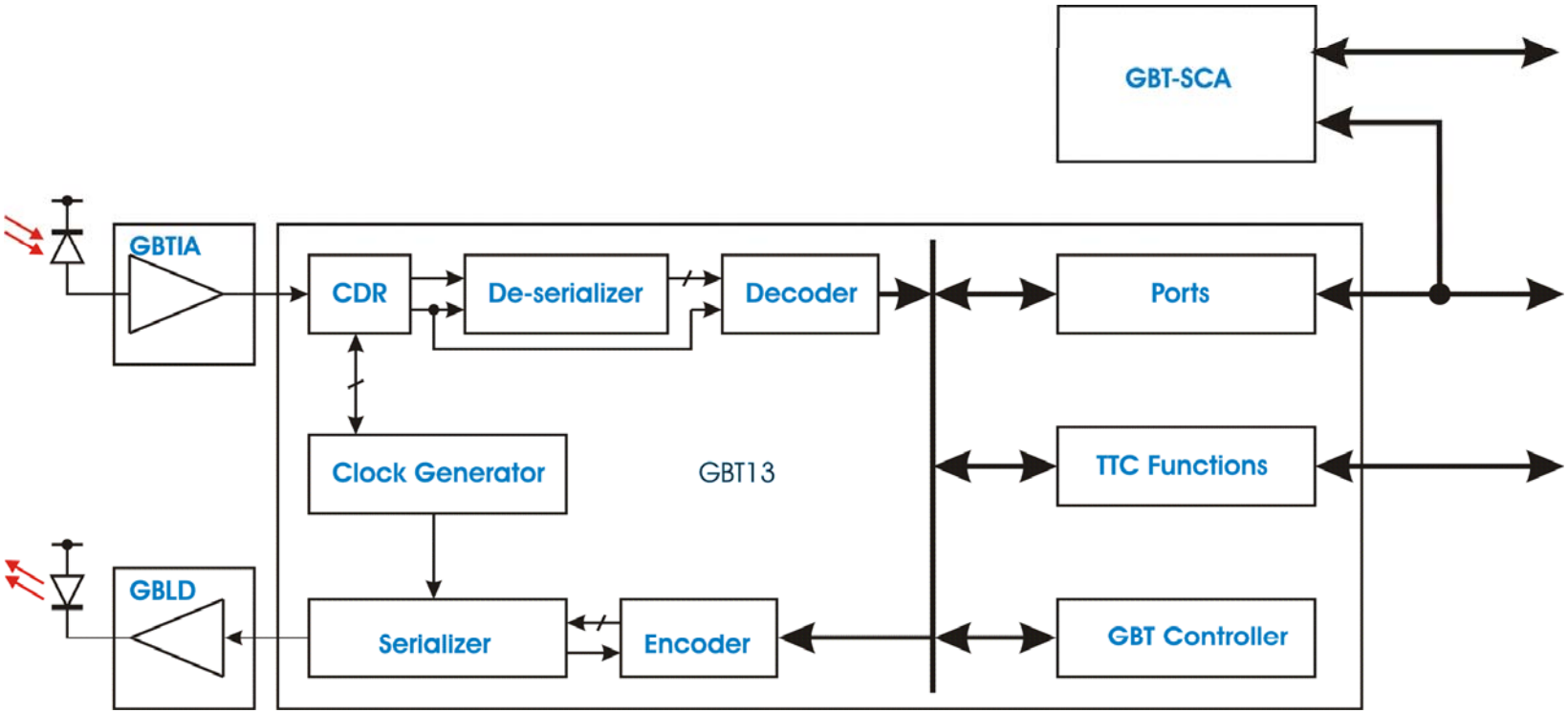
The GBT project



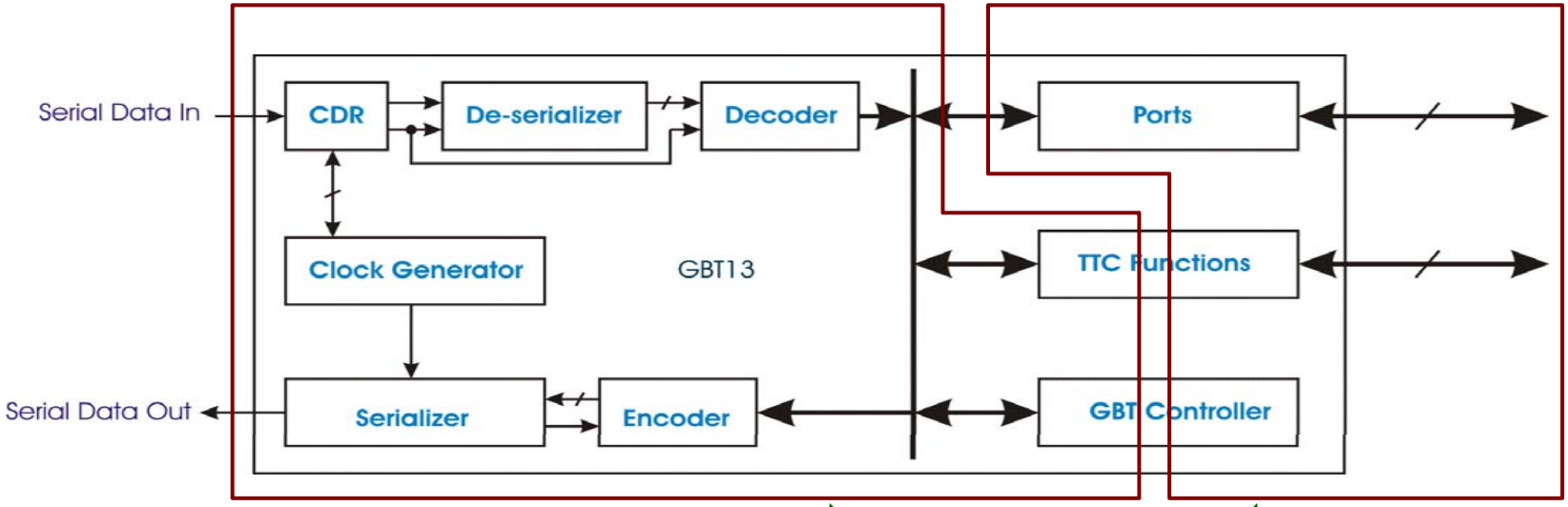
- Single link serves:
  - Readout (DAQ)
    - High speed unidirectional up-link
    - Trigger data
  - TTC
    - Clock reference and synchronous control (down-link)
  - SC/DCS/ECS
    - Modest bandwidth bidirectional link
- Custom ASICs in the detectors
- Cots in the counting room
  - FPGAs used to implement multi-way transceivers

The GBT chipset



- GigaBit TransImpedance Amplifier (GBTIA)
- GigaBit Laser Driver (GBLD)
- GigaBit Transceiver (GBT13)
- GBT – Slow Control ASIC (GBT-SCA)

GBT13 – GigaBit Transceiver (130 nm)

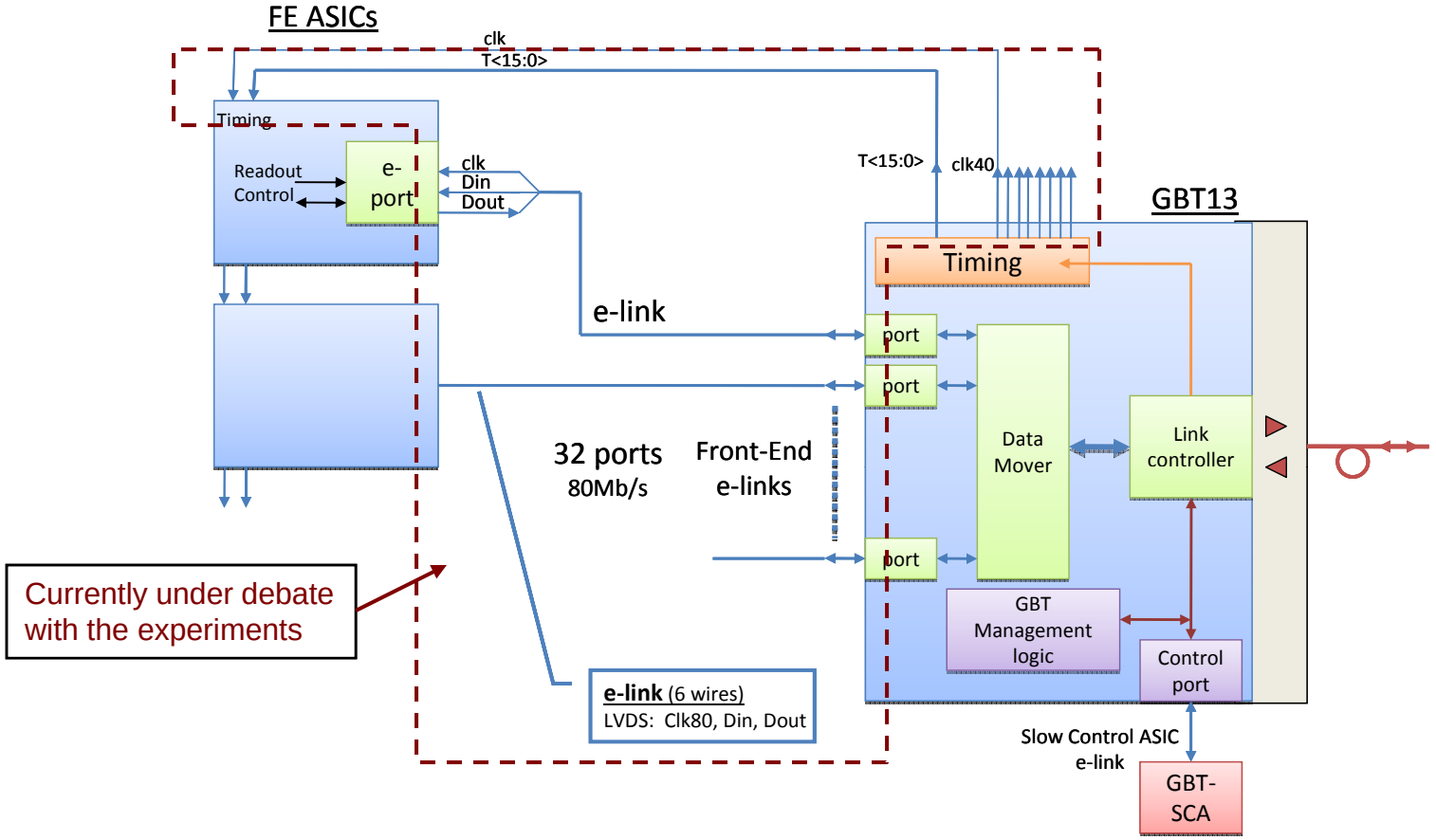


- Functionality:
  - De-Serializer and CDR
  - Serializer
  - Data CODEC with FEC
  - Timing and Trigger functions
  - Data and Slow control Links

Still in the early specification phase: must be designed according to the experiments needs!

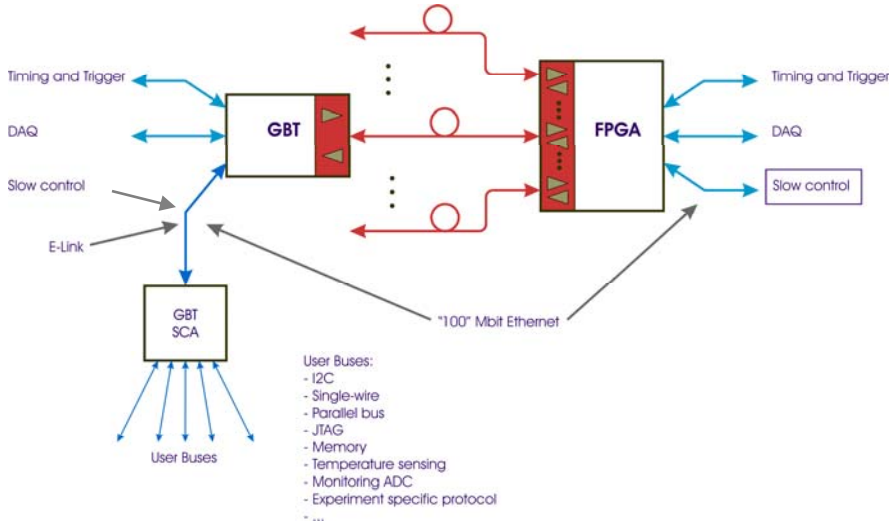
Standard serial communications building blocks, functionality well defined and “independent” of the overall architecture.

Possible GBT to front-end link topology



- GBT to Front-end links:
  - Bi-directional serial links (e-links) VS Parallel bus?
  - Several e-links can be grouped together to serve a single front-end to achieve high bandwidths
- **An E-Link Port Adaptor (EPA) "macro" will be available for integration in the front-end ASICs**

SCA – Slow Control ASIC



- Slow control functions are implemented by a dedicated ASIC: the GBT-SCA
- The chip communicates with the control room using an Ethernet like protocol carried (transparently) by the GBT
- The GBT-SCA interfaces with the GBT13 using a dedicated E-link port
- It will implement multiple protocol busses and functions:
  - I2C, JTAG, Single-wire, parallel-port, etc…
- It will implement environment monitoring functions:
  - Temperature sensing
  - Multi-channel ADC
- The specification work for this ASIC is now starting

Forward error correction (FEC)

- Objectives:
  - Correct burst errors:
    - Generated on the PIN-diode
    - Generated by particles hitting the transceiver (TIA/LD)
    - Generated in the fast SERDES circuits (can't use TMR)
    - Done with minimal latency
    - Done with good efficiency
    - Merge with line-coding
- Proposed code:
  - Compatible with FPGAs capabilities
  - Interleaved Reed-Solomon double error correction
  - 4-bit symbols (RS(15,11))
  - Interleaving: 2
  - Error correction capability:
    - **$2_{Interleaving} \times 2_{RS} = 4$ symbols $\cong$ 16-bits**
  - Code efficiency: 88/120 = 73%
  - Line speed: 4.80 Gb/s
  - Coding/decoding latency: one 25 ns cycle
- GBT frame efficiency: 70%
  - A line code is always required for DC balance and synchronization
  - For comparison, the 8B/10B frame efficiency is 80%

Project Collaborators

Institute	Project Mgmt.	System Design	ASIC Design	FPGA Design	Opto-Electronics	Passive Compnts.	Radn. Testing
CERN	x	x	x	x	x	(x)	x
CPPM Marseille			x	x			
INFN Bari			x				
INFN Bologna		x	x				
INFN Torino			x				
Oxford						x	x
SMU Dallas		x	x	x			x

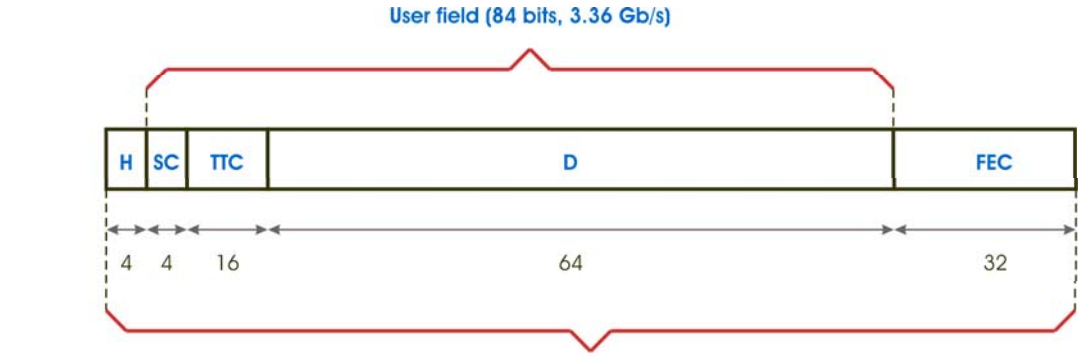
Tentative Schedule

- 2008
  - Design and prototyping of basic building blocks: TIA, laser driver, PLL, serializer, deserializer
  - First tests of optoelectronics components (e.g. to understand SEU in PIN receivers)
  - Start link specification meetings
  - First early version of a general link specification
- 2009
  - Design/prototype/test of basic serializer/deserializer chip
  - Design/prototype/test of optoelectronics packaging
  - Detailed link specification document
- 2010
  - Prototype of “complete” link interface chip
  - Final prototype of optoelectronics packaging
- 2011
  - Extensive test and qualification of full link prototypes
  - System demonstrator(s) with use of full link
  - Final production version of optoelectronics and link interface chip (strong dependency on time schedule of LHC upgrade program)

Summary

- We propose a “Single” Link solution for:
  - Timing Trigger Links
  - Data Acquisition Links
  - Experiment Slow Control Links
- The link is based on radiation tolerant components for on-detector use coupled to COTS devices in the counting rooms:
  - The GBT chip-set using radiation-tolerant design techniques:
    - GBT13, GBTIA, GBLB & GBT-SCA
  - Versatile Transceiver built from Radiation-Qualified Opto-electronic components
  - Commercial Optical Transceivers or Array Receivers
  - Commercial FPGAs with embedded Serializers and Deserializers
- Versatile Transceiver based upon Commercial Design as far as possible
  - Currently investigating the SFP+ format as the most promising
- Extensive radiation qualification of commercial laser diodes and photodiodes will be required to enable use in HEP environment, both for total dose/fluence and SEU
- Implement a error robust transmission protocol over an optical fibre
- Slow control and monitoring is implemented by a dedicated channel
  - Slow control is managed by the GBT-SCA
- The GBT/front-end electronics interface currently under discussion with the experiments
  - Forum is a discussion group containing representatives from the 4 (S)LHC experiments
- Developments are being carried out in collaboration with a number of external institutes

Link bandwidth



H - Header

SC - Slow Control (160 Mb/s)

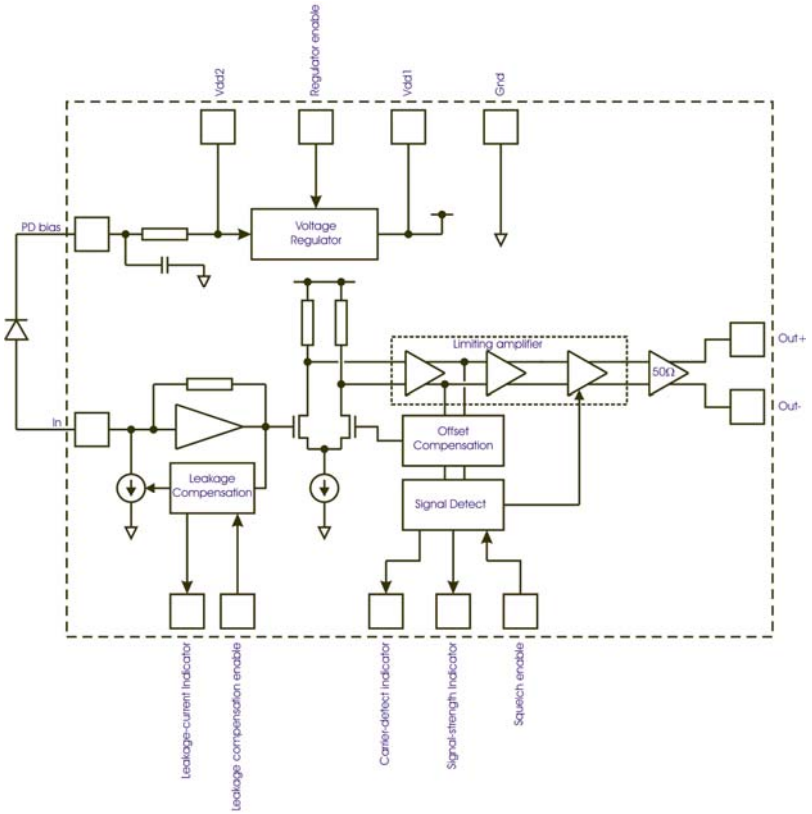
TTC - Timing Trigger and Control (640 Mb/s)

D - Data (2.56 Gb/s)

FEC - Forward Error correction

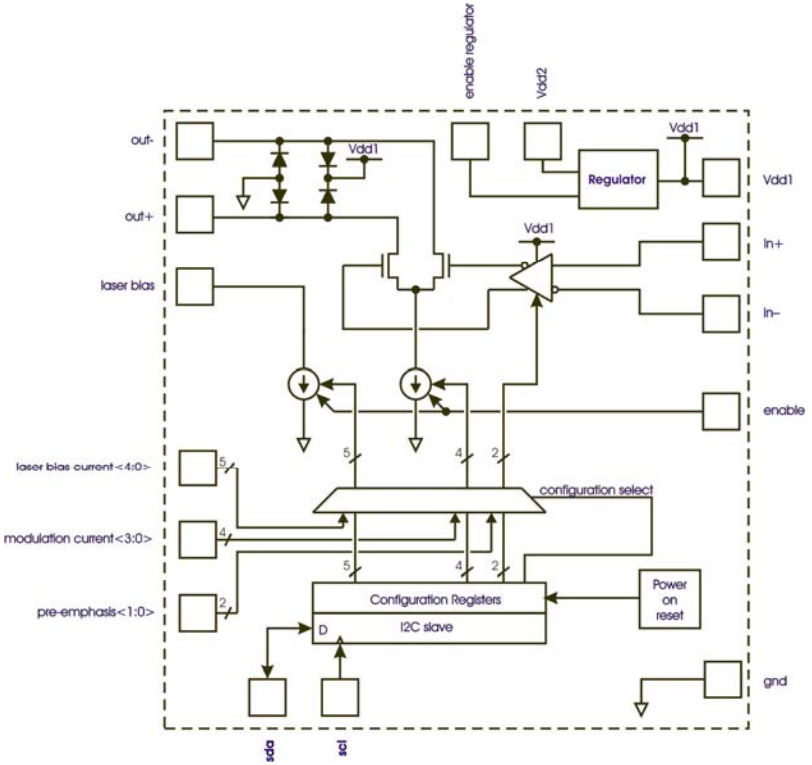
- GBT: 120-bits transmitted during a single bunch crossing interval → 4.8 Gb/s.
- 4 header bits
- User field of 84 bits → 3.36 Gb/s:
  - SC: 4-bits → 160 Mb/s
  - TTC: 16-bits → 640 Mb/s
  - DAQ: 64-bits → 2.56 Gb/s
- 32 forward error correction bits
- Bandwidth is fixed per frame but can be shared by the front-end devices

GBTIA - GigaBit TransImpedance Amplifier



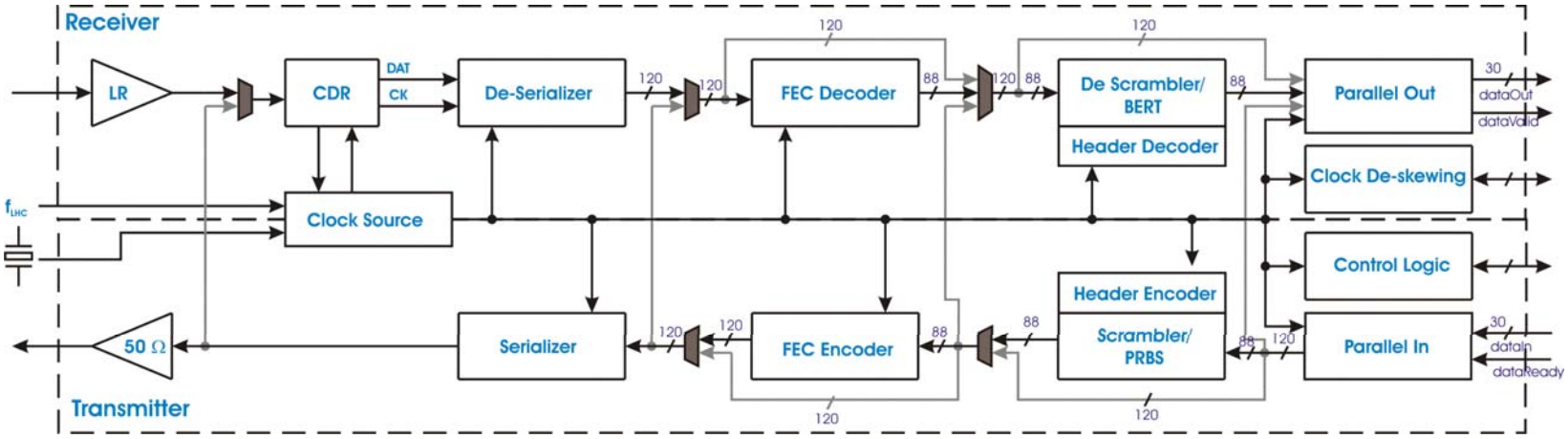
- Main features:
  - Data rate: 4.8 Gbit/s
  - Integrated pre-amp & post-amp
  - Photo-diode leakage current compensation
  - Limiting amplifier offset compensation
  - Internal RC filter for photodiode bias
  - Carrier-detect, leakage-current and signal-strength indicators
  - Leakage-current magnitude indicator
  - Squelch function
  - Internal voltage regulator
  - Power consumption: ~ 200 mW
- Packaging:
  - Chip and PIN-diode to be integrated on the same package
  - Package to be developed with an industrial partner

GBLD – GigaBit Laser Driver



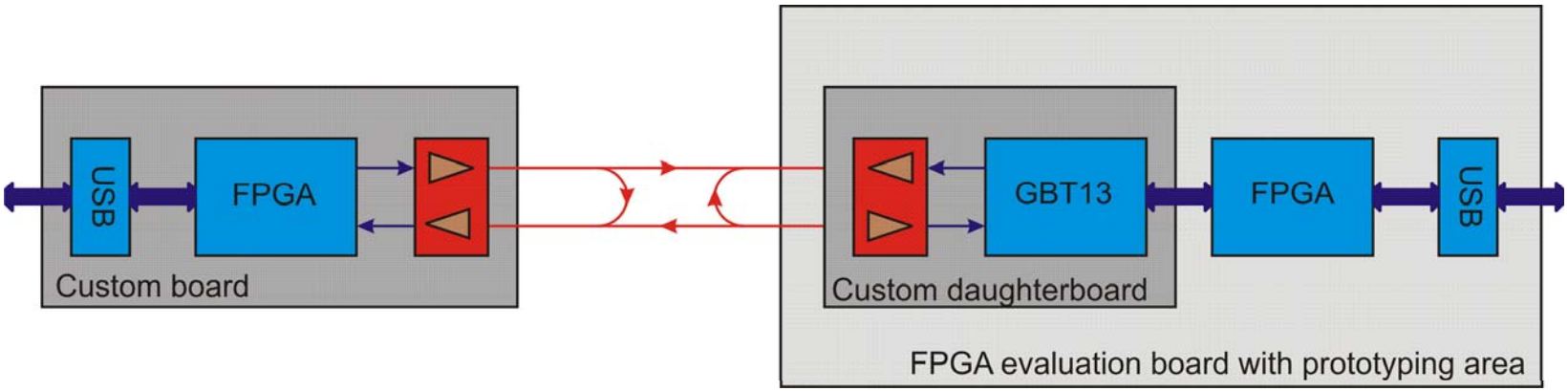
- Main features:
  - Data rate: 4.8 Gbit/s
  - Edge-emitter and VCSEL driver
  - Programmable:
    - Modulation current
    - Laser bias current
    - Pre-emphasis
  - I2C interface
  - Power consumption: ~ 350 mW (maximum current settings)
- Package:
  - QFN20 (4 mm × 4 mm)
  - Compatible with commercial products
  - Good high frequency characteristics
  - “Some” customization of the package is required

GBT13 – GigaBit Transceiver (prototype)



- GBT13 prototype:
  - De-Serializer and CDR
  - Serializer
  - Data CODEC with FEC
  - Clock phase shifter
  - Parallel IN/OUT bus
    - 30 + 30-bits @ 120 MHz
- Package:
  - C4 package (flip-chip)

The GBT in the counting room & testing



- In the counting room:
  - GBT transceivers will be implemented by FPGAs
  - The choice of the GBT encoding scheme was guided by the constraints imposed by today's FPGAs hardware
  - Designing an GBT-FPGA transceiver is thus crucial for the project
- Testing:
  - A working FPGA GBT transceiver is a key to test of the GBT13
  - The GBT FPGA transceiver must thus implemented and tested so that it can be used as a tests vehicle for the GBT13
  - A design team is now working at implementing the GBT protocol in an FPGA

Project collaborators

CERN –Geneva Switzerland:

S. Baron, J. Christiansen, O. Cobanoglu, F. Faccio, K. Kloukinas, A. Marchioro, P. Moreira, C. Paillard, J. Troska, F. Vasey, K. Wyllie

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Evaluation of Commercial Transceivers

- Measuring performance based on Eye-diagrams
  - Develop test methods applicable to evaluating Versatile TRx prototypes
  - Gives a basis for the choice of components for Versatile TRx
  - Aids the writing of specifications that will form the basis of working with industrial partners