FGClite Power Control

TE-EPC-CCE

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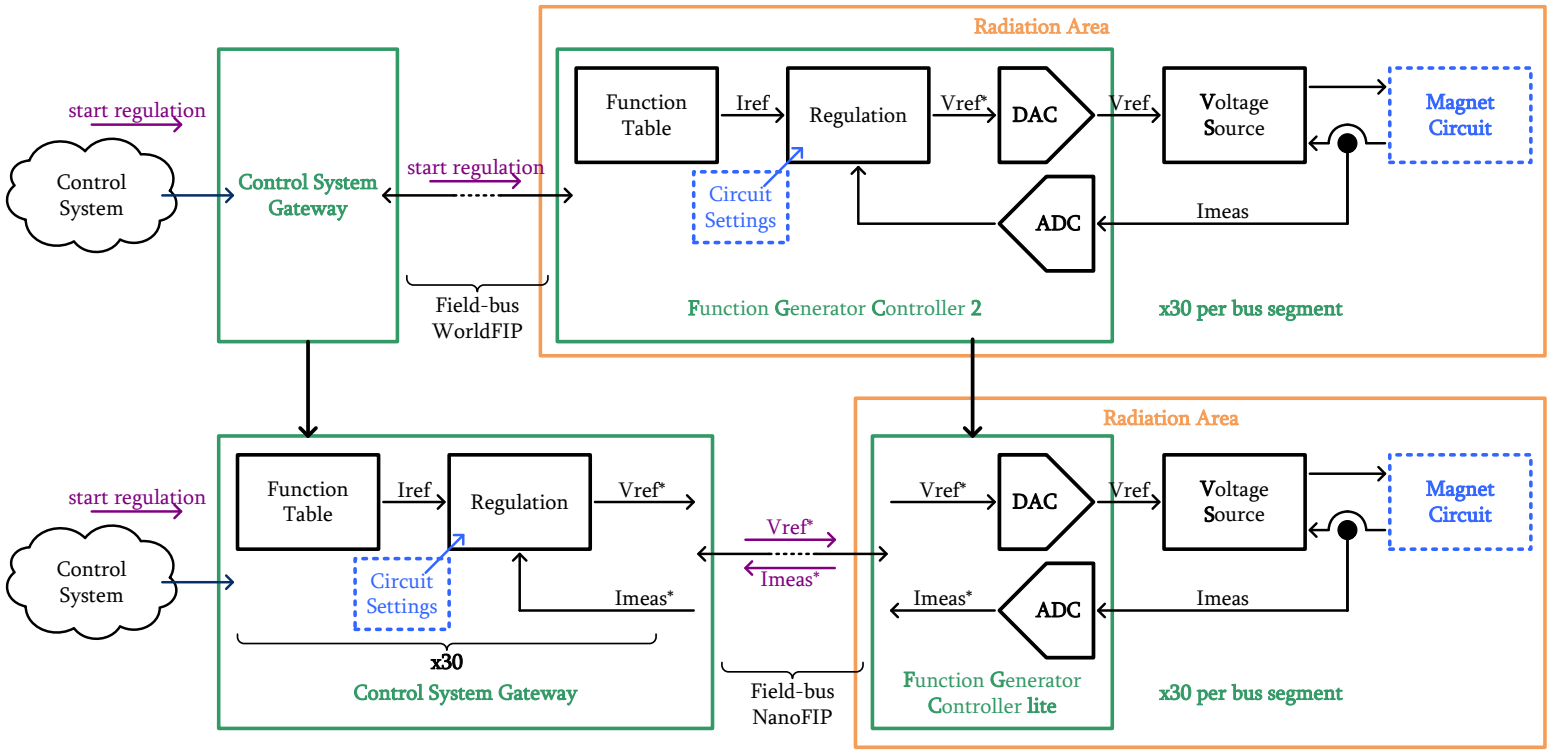
Outline

1. FGClite Introduction
2. Challenges
3. Power Control & Machine Protection Links
4. System Failure Modes
5. Power Cycle Procedure
6. Conclusions

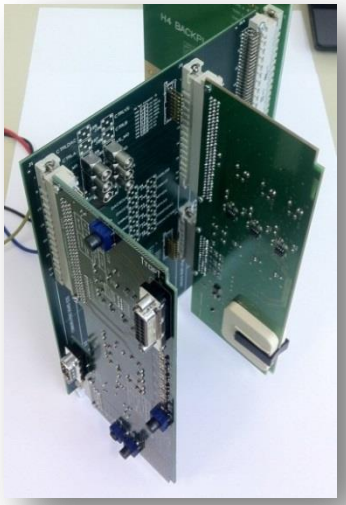
Converter Requirements			Quantity
Typical Use	Current	Voltage	
Main Dipoles	13000	190	8
Main Quadrupoles	13000	18	16
Individually Powered Quadrupoles/ Dipoles and Inner Triplets	4-6-8000	8	189
Orbit Correctors 600A Sextupole correctors	600	40	37
600A Multipole correctors	600	10	400
Orbit Correctors	120	10	290
Orbit Correctors	60	8	752
		Total	>1700



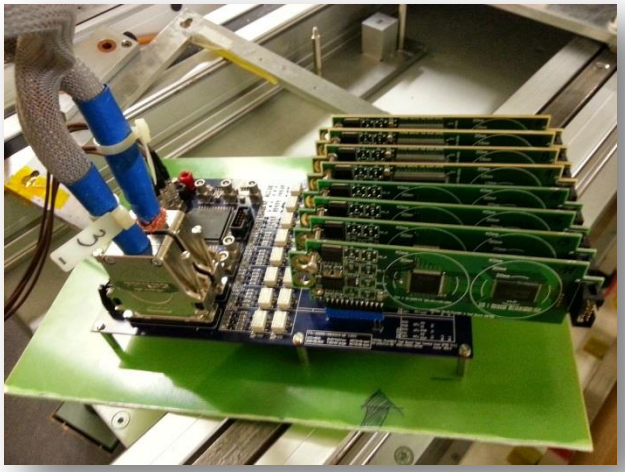
Dedicated design methodology:

1. No microcontrollers/DSP as computationally intensive tasks moved to the gateway
2. Extensive radiation testing to select/validate all electronic components
3. Highly available Gateway/FGClite communication required

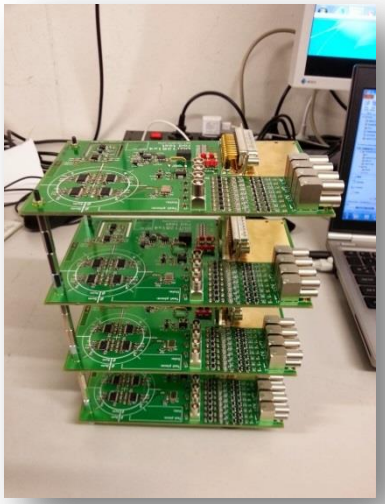
FGClite Introduction (3/4)
Project Timeline



Prototype



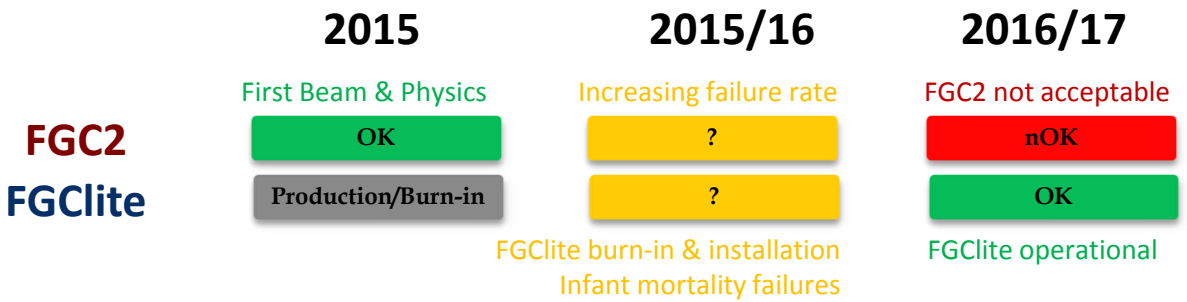
FPGA Type Tester

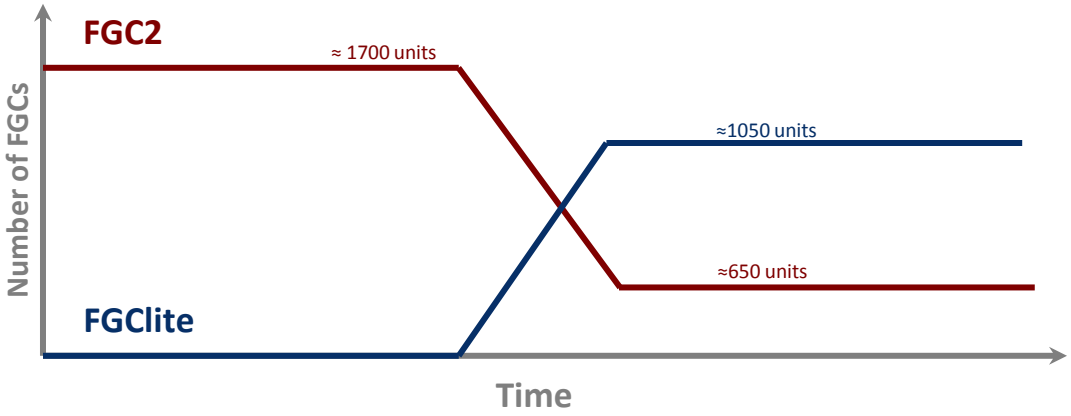


ADC Type Tester

2013 – Hardware design & component type testing
Q3/2014 – 10 fully validated FGClite proof-of-concept modules
Q3/2014 – Start of component batch testing using CHARM (PS East Area)
Q2/2015 – Series production

FGClite project planning



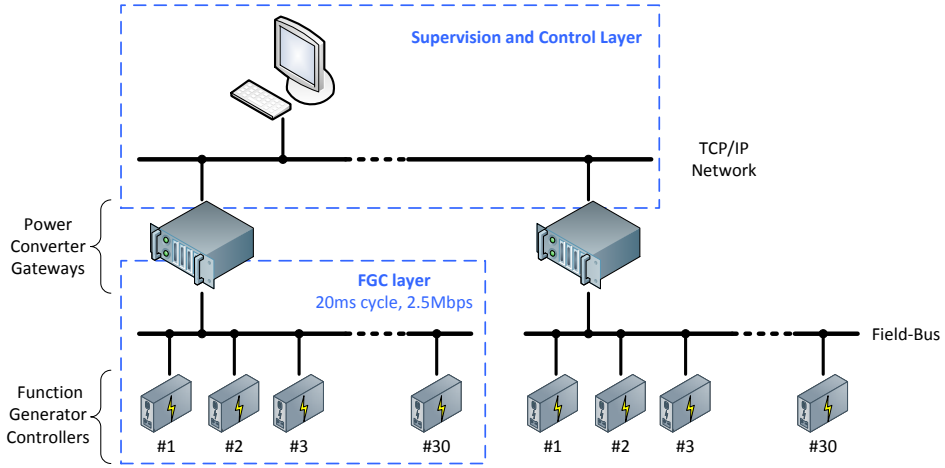


2015: FGC2 will be used after LS1 for the first months as its failure rate will be acceptable

2015/16: FGC2 will start failing due to increasing radiation levels thus FGClite will be installed

2016/17: Operational FGClite will exhibit much lower failure rate than FGC2 after infant mortality issues are addressed.

Reliable communication infrastructure



FGClite infrastructure (TE-EPC):

1. Robust FGClite hardware
2. Robust Gateway software and hardware

World FIP (BE-CO):

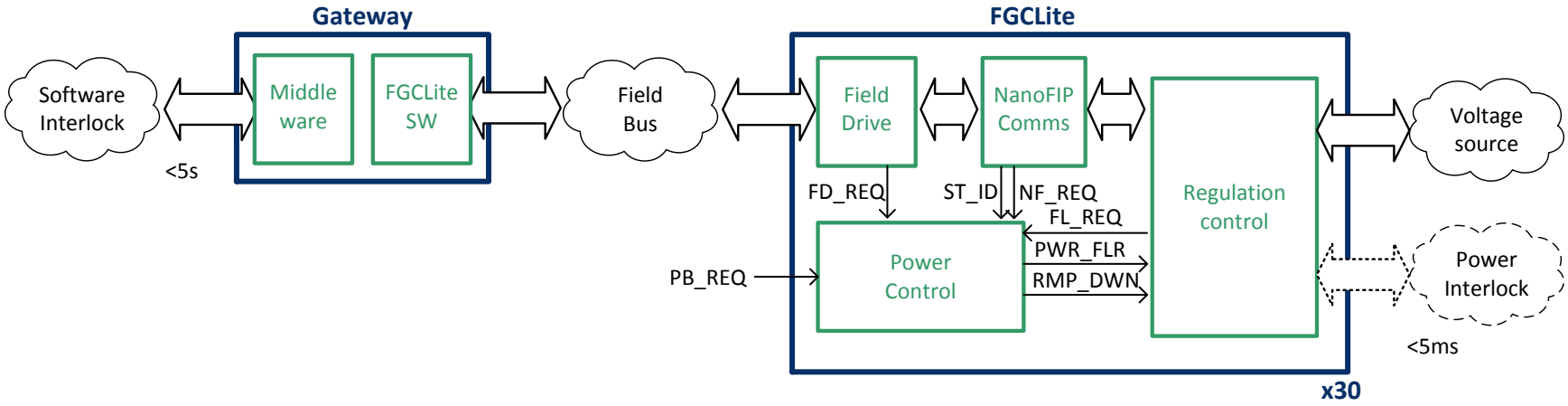
1. FGClite/Gateway communication modules
2. **Robust repeaters**, cabling, etc…

Field Bus functional tests (BE-CO):

- High speed, high temp, long cables, 30 days
- Not sufficient statistics

- Lost packet probability $<4.4\times10^{-9}$/packet
- FGClite system $<1.6\times10^{4}$ lost packets/year

FGClite system – links with machine protection

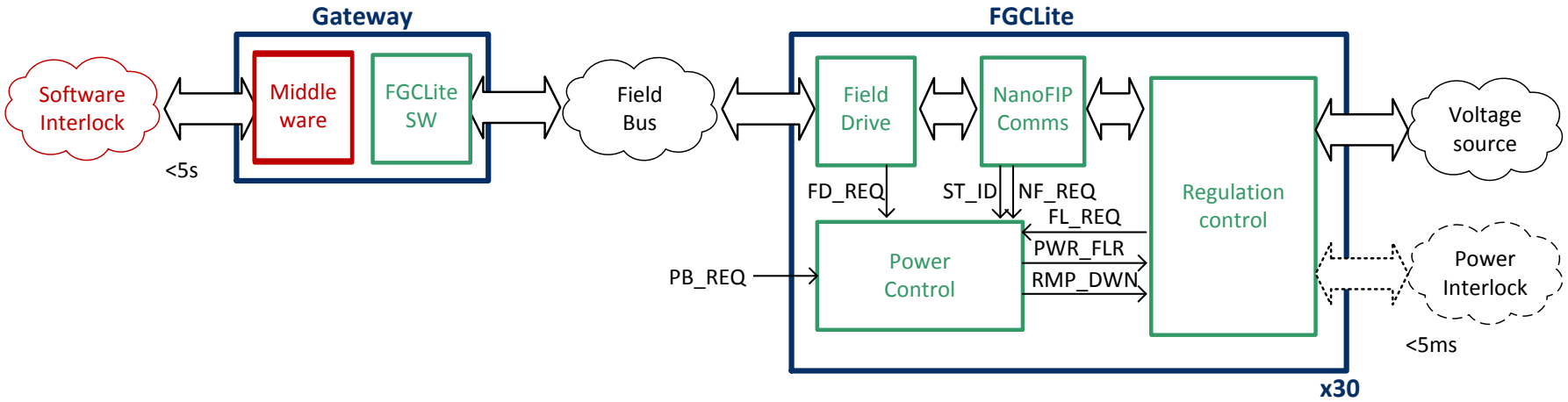


Power Cycle possibilities:

1. FD_REQ: Field Drive Request → Field Bus no carrier
2. NF_REQ: NanoFIP Request → Requested by Gateway via Field Bus
3. FL_REQ: FGClite Request → Requested by FGClite
4. PB_REQ: Push Button Request → Requested by operator from the front panel

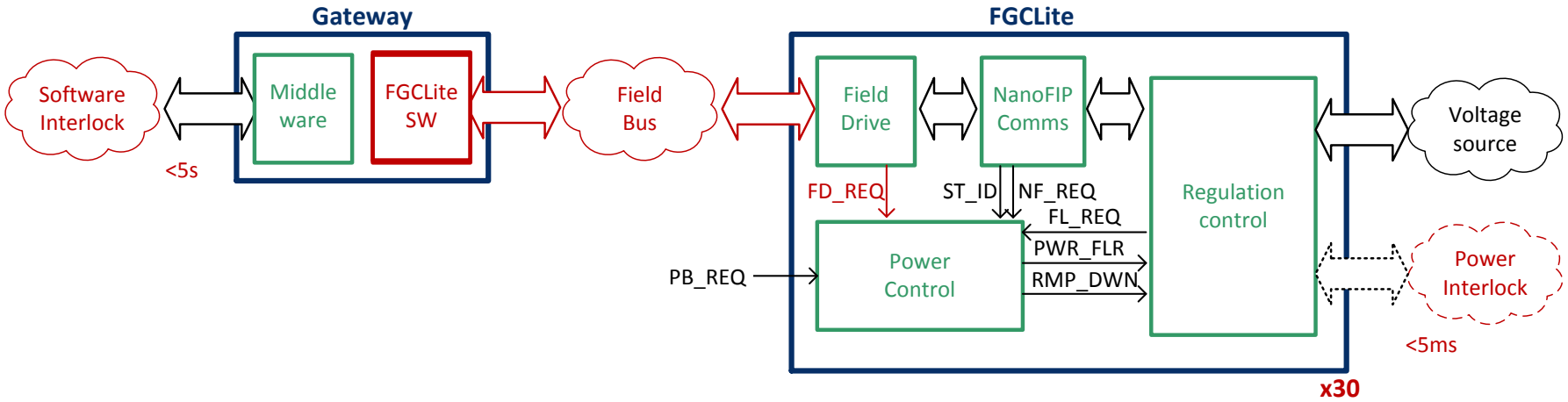
FGClite power cycle leads to power converter failure

Gateway/SIS communication fails but Fieldbus communication OK



FGClite will not power cycle
Software Interlock may decide to initiate protective action

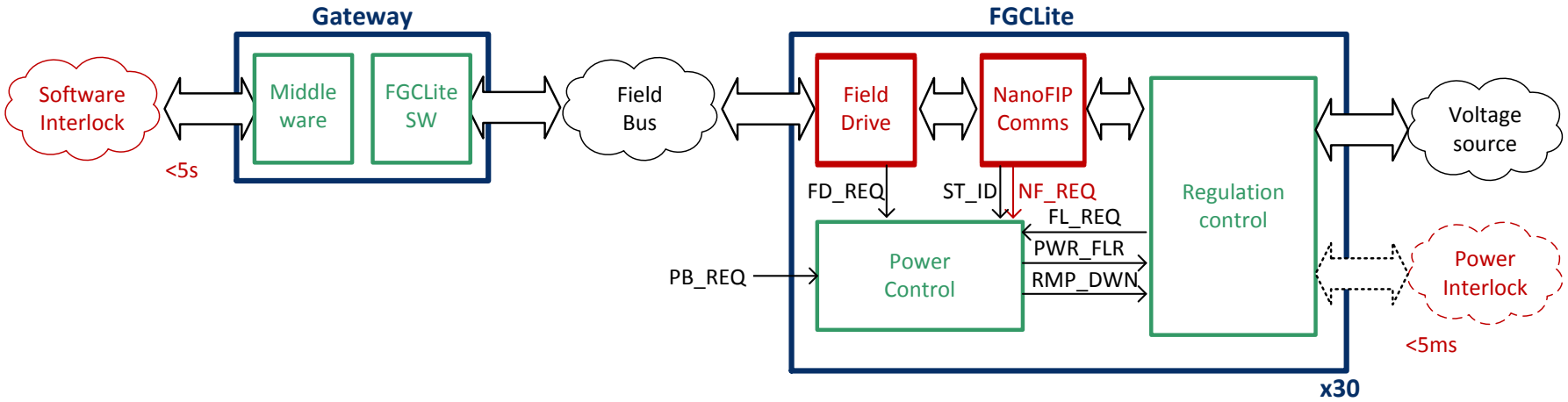
Gateway fails and Fieldbus communication fails



Failed communication = >1 lost FIP packet

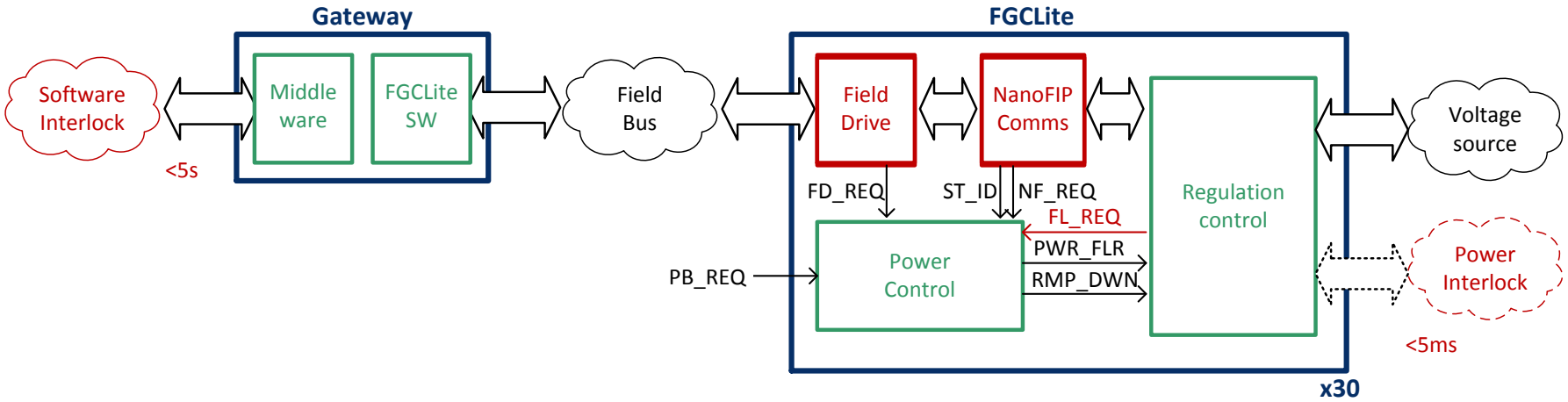
All 30 FGClites will power cycle (triggered by lack of communication with gateway)
Software Interlock may decide to initiate protective action
After the power cycle FGClites will wait for valid FIP communication

FGClite transmission failure



A single FGClite will power cycle triggered by the gateway
Software Interlock may decide to initiate protective action
After the power cycle FGClite will wait for valid FIP communication

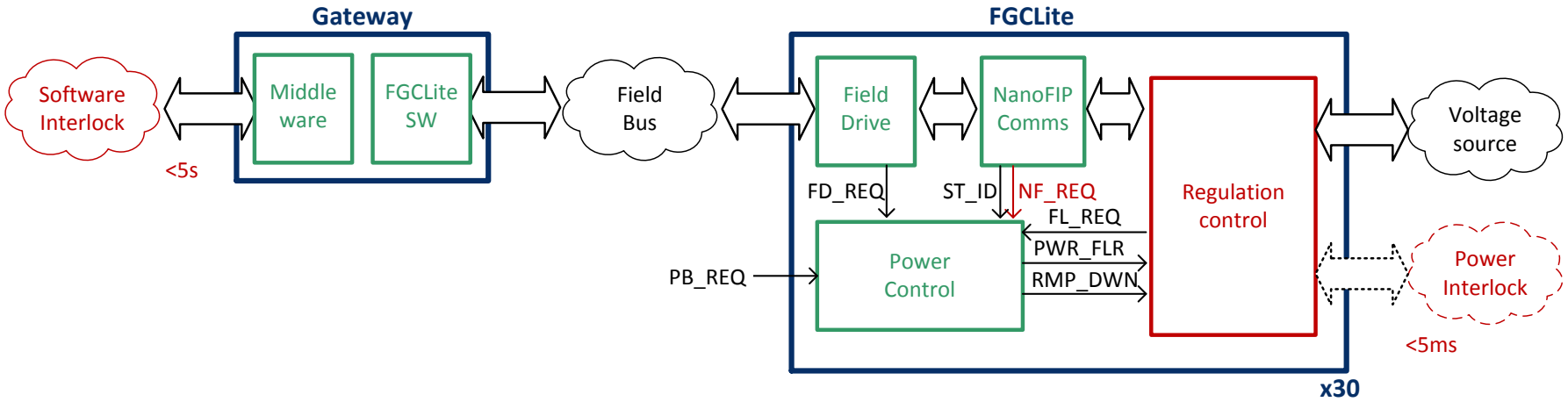
FGClite reception failure



Failed communication = >1 lost FIP packet

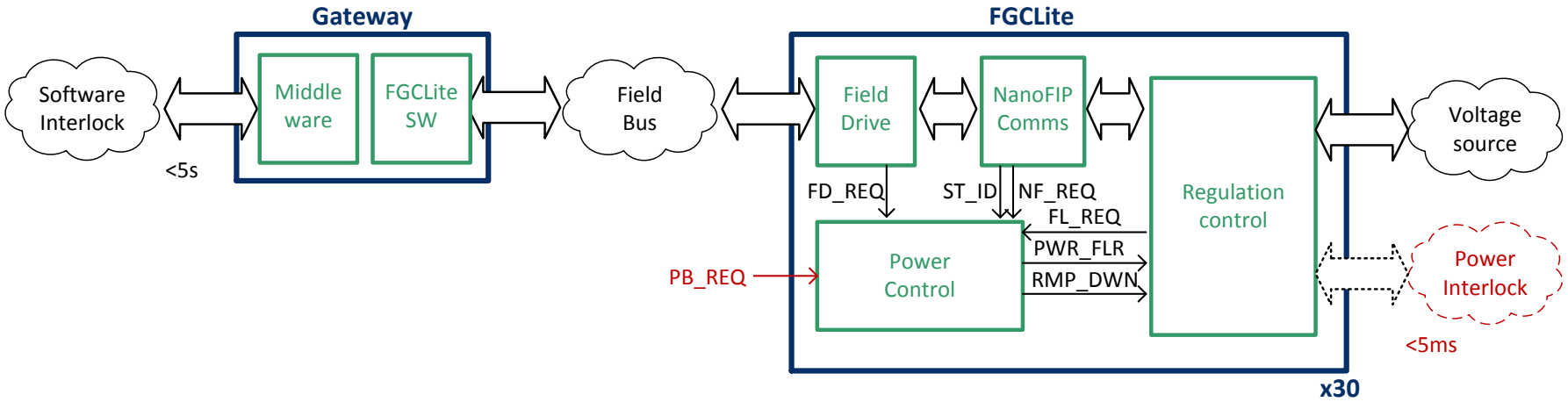
A single FGClite will power cycle triggered by the FGClite
Software Interlock may decide to initiate protective action
After the power cycle FGClite will wait for valid FIP communication

FGClite internal failure



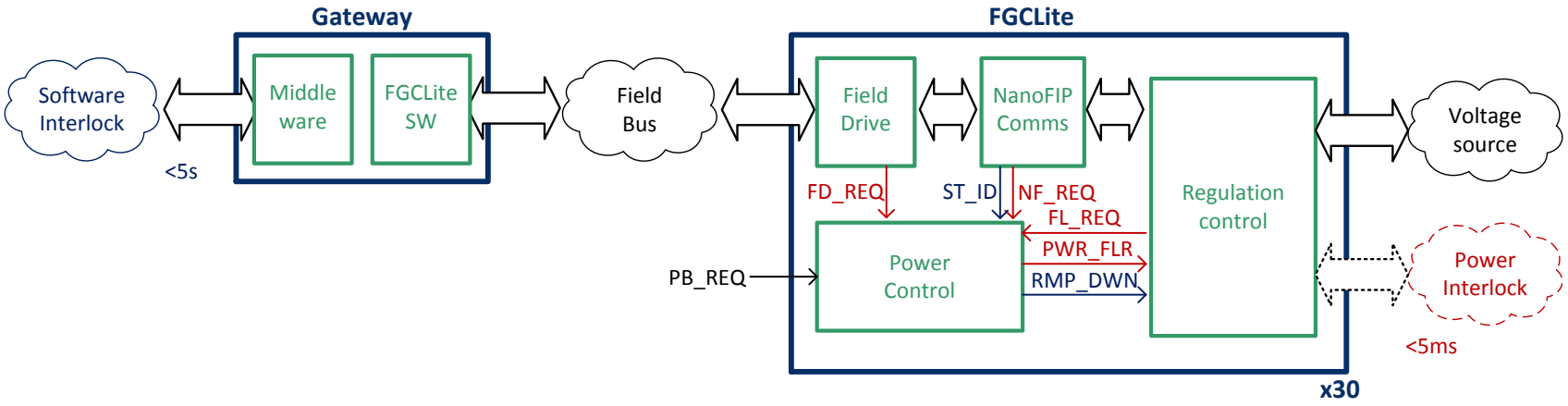
A single FGClite will power cycle triggered by the gateway
Software Interlock may decide to initiate protective action
After the power cycle FGClite will wait for valid FIP communication

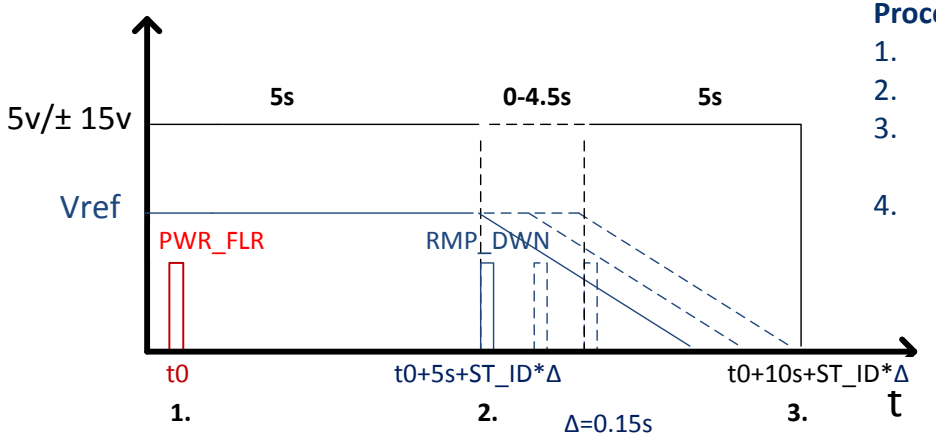
Push Button pressed



A single FGClite will power cycle triggered by an operator from the front panel
After the power cycle FGClite will wait for valid FIP communication

Remote Power Cycle (FD_REQ, NF_REQ, FL_REQ)

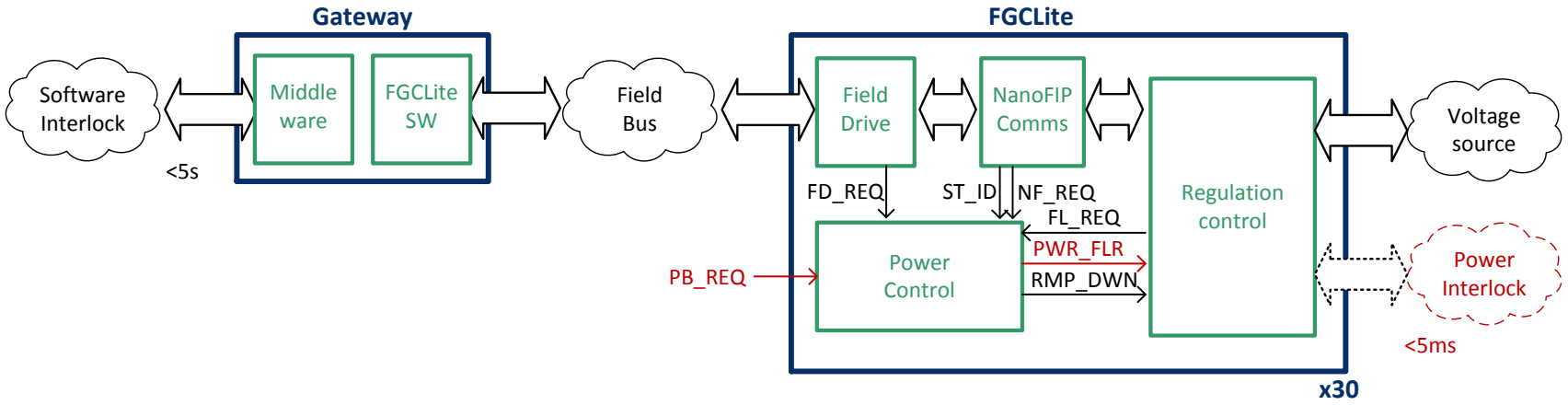




Procedure:

1. Communicate PWR_FLR
2. Maintain Vref (SIS time to react)
3. Start ramping down (spread time to avoid fast orbit changes)
4. Ramp down (to avoid QPS trigger) & switch off

Push Button Power Cycle (PB_REQ)



Procedure:

1. Communicate PWR_FLR
2. Switch off

FGClite relies on highly available Fieldbus communication

FGClite failure modes were identified and power cycle strategy was defined:

1. Gateway failure
2. Field Bus communication failure
3. FGClite transmission/reception failure
4. FGClite internal failure

Power cycle procedure was defined:

1. Information to Software Interlock/Power Interlock
2. Ramping down Vref in different times on the same Fieldbus sector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Dedicated R2E design/test methodology

Radiation Tests		
Component Class	Type Tests	Batch Tests
Class-2	6 (done)	3/6 (FPGA)
Class-1	21 (done)	3/21 (CHARM)
Class-0	x	14 (CHARM)
Total Done (all facilities)	**35**	**6**

Type Testing Status
Batch Testing Status

Electrical MTBF estimation

When the FGClite final prototype is finished the MTBF will be computed
These computations will be based on Military Handbook (MIL-HDBK-217F)
The eletrical MTBF will be compared with the FGC2 system (~1Mhours)

Fieldbus communication tests & burn-in

The first Fieldbus sector will be populated in Q3 2014
This will allow Fieldbus communication tests and its error rate measurement
First burn-in tests will be performed in Q4 2014