WG10: Online SW & Computing

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FCC-ee/TLEP physics workshop (TLEP7)

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Mandate

Work towards hardware & software solutions that will allow TLEP experiments to store interesting physics with high efficiency & redundancy (with minimum uncertainties or biases)

- For review of event sizes, trigger rates (and long list of questions) see FCC kickoff study talk:
  https://indico.cern.ch/event/282344/session/14/contribution/56/material/slides/0.pdf
- Emphasis today is on progress since FCC kickoff study meeting

Introduction

- Assumptions
  - ➢ Trigger input = trigger output = DAQ rate = interesting physics. In other words:
    - Signal efficiency ~ 100%
    - Background ~ not a major consideration
  - ➢ Rate of interesting physics: ~15 kHz (Z events) + 60 kHz (Bhabha)

(Vast gap in terminology between hadron and lepton collider people….)

Level-1 or HLT?

- ILC assumes DAQ with “trigger-less” design

- Main question for TLEP
  - Hardware-based (aka: Level-1) or software-based (aka: C++/HLT) trigger?
  - Examples of technologies involved:
    - Level-1: FPGAs
    - HLT: GPU or Many-Core

Level-1 or HLT?

- Why not stick to software/C++ and keep things simple?

- Detector choices can have an impact on trigger/DAQ, eg:
  - Tracking: a Time Projection Chamber (TPC) that cannot be read out every 20 ns
  - Calorimetry: with a fine-granularity & noisy calorimeter one may not be able to apply zero suppression at the trigger

Level-1 or HLT?

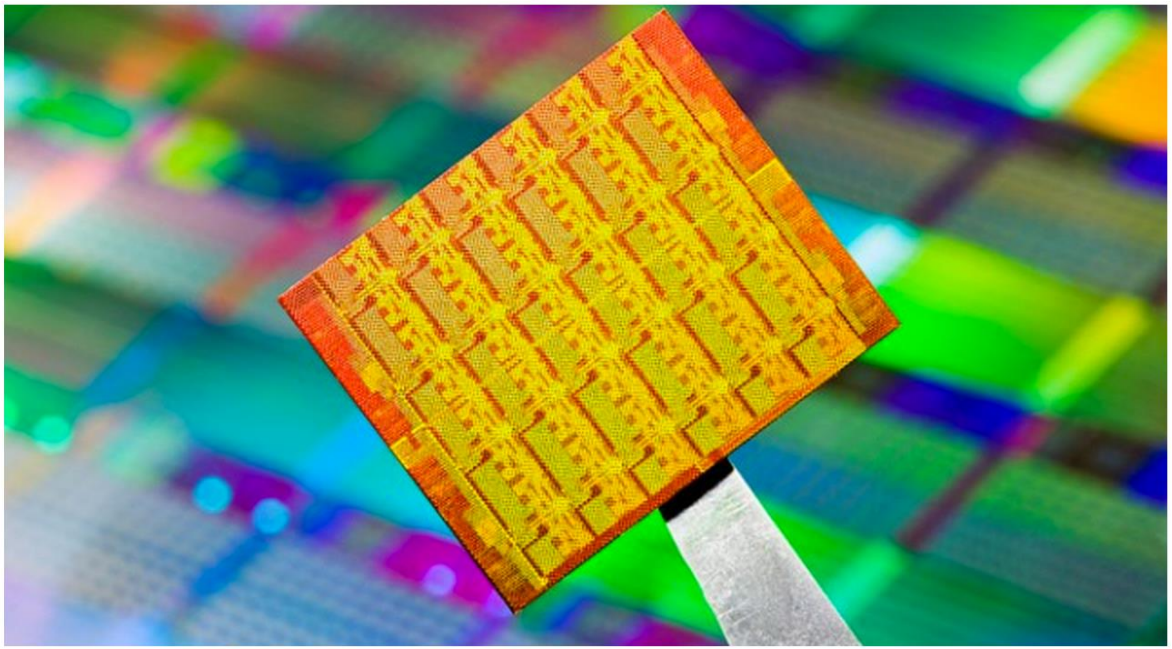
- Is it really that bad if we have to use a hardware trigger?

- No. We will survive
  - Code developent for GPUs is very similar to that for FPGAs. To a certain extent, a Level-1 based or C++ based trigger design could accommodate a GPU-like algorithm.

Xeon & FPGAs

Intel unveils new Xeon chip with integrated FPGA, touts 20x performance boost

By Sebastian Anthony on June 19, 2014 at 1:19 pm | Comment



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Late yesterday, Intel quietly announced one of the biggest ever changes to its chip lineup: It will soon offer a new type of Xeon CPU with an integrated FPGA. This new Xeon+FPGA chip will fit in the standard E5 LGA2011 socket, but the integrated FPGA will allow

WG10 prerequisites

- Physics studies: one can start from MC-truth particles, apply some smearing and carry out a feasibility study and/or expected measurement precision

- Experimental environment: need detector hits so we can evaluate event sizes, and put together reconstruction algorithms, study inefficiencies, latencies, biases, etc
  - ➢ WG10 prerequisite: simulation of detector hits (collaboration with WG9)

WG10 projects

- Begin with GPU or many-core development of physics-object reconstruction algorithms
  - ➢ Exact underlying technology (e.g. GPU vs Many-Core, OpenCL vs nVidia's CUDA) is not important to know
  - ➢ Main challenge: develop parallelizable algorithms (see Benedikt's talk from yesterday); algorithms can then “easily” get ported to another architecture if needed
  - ➢ Software experts that work very closely with detector and reconstruction experts

- Synergy with WG8 for evaluation/impact of synchrotron radiation, beamstralung, beam backgrounds

List of Tasks #1

- Define list of specific tasks that can be assigned to (and studied by) individuals and small groups

Examples:

- Algorithmic inefficiencies, impact on asymmetries, etc
- Algorithmic redundancy
- Zero-suppression at trigger compatible with potentially noisy calorimeter?
- Beam background's impact on rates, event size

Collaboration with object reconstruction, beam experts

List of Tasks #2

- Studies to be carried out for
  - Different detectors designs (sizes, granularity, etc)
  - Accelerator parameters