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## Radiation tests of pixel readout chip designed in 40nm CMOS technology

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The tests with gamma rays were performed on the pixel detector readout chip designed in TSMC 40nm CMOS technology. The ASIC works in single photon counting mode, consists of both analog and digital blocks including charge sensitive amplifier, two shapers, two discriminators, two separate counters and more supporting blocks. For the purpose of radiation hardness tests different radiation doses were applied from 140 Mrad to 2540 Mrad. The biasing transistors' characteristics, both for p-mos and n-mos types, were measured for the following radiation doses: 140 Mrad, 240 Mrad, 440 Mrad, 880 Mrad and 2540 Mrad. The characterization of the ASIC, including DC offset correction and gain measurements, was performed before and after radiation for the dose equal to 140Mrad.

### Summary

Certain changes of the biasing transistors' characteristics are observed after the irradiation. The behavior of the transistor varies depending on its type (p-mos or n-mos). The irradiation also changes the gain (decrease) and the DC offsets in each pixel, however the channel architecture allows for effective correction and returning the nominal conditions without noticeable change.

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