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Investigation of total ionizing dose effect and displacement damage in 65 nm CMOS transistors exposed to 3 MeV proton

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DIPARTIMENTO DI FISICA E ASTRONOMIA 'GALILEO GALILEI'

Outline

- Introduction
- Experiment and devices description
- Results and discussion
- Conclusion

Introduction

- Under the HEP environment:
  - Low energy electrons and photons => TID
  - Neutrons, high energy protons, other particles => DD

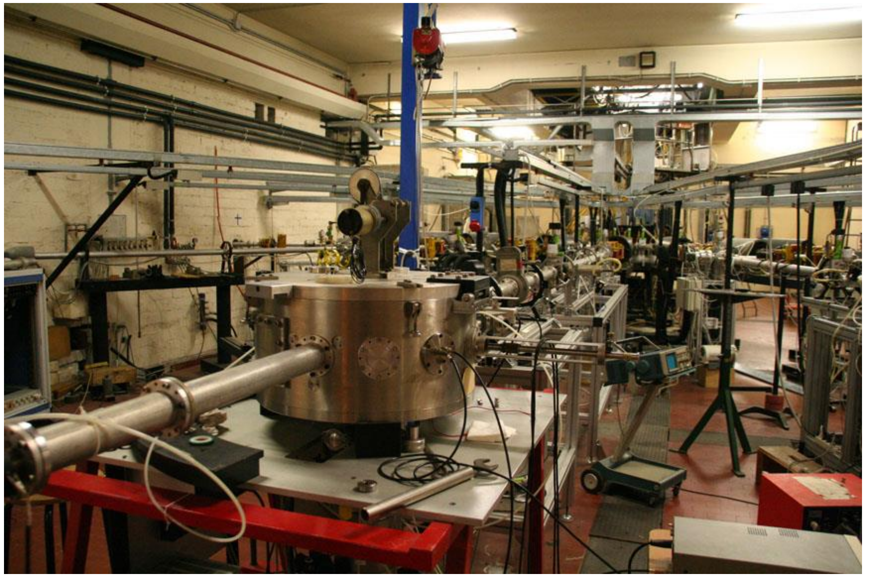
Fluence (3MeV proton)	***Deposited dose***	***1 MeV neutron equivalent fluence***
7×10^{14} p/cm^2	1 Grad(SiO_2)	10^{16} n/cm^2

* LET in SiO_2: 9.3×10^{-2} MeV·cm^2/mg
* NIEL in Si: 5.2×10^{-5} MeV·cm^2/mg

- 3 MeV proton: a good candidate of evaluating the radiation damage under the mixed radiation environment.

Experiment and devices description

- Irradiation environment: 3 MeV proton
  - CN accelerator, INFN-Laboratori Nazionali di Legnaro
  - Samples were mounted in the vacuum chamber and biased during irradiation
  - Maximum proton beam current: 1 μA
  - Maximum flux: 2×10^{13} p/cm^2/s



Experiment and devices description

- Preparation
  - Beam uniformity was checked before irradiation:
    1. Gafchromic radiology film was exposed to the beam for few seconds to provide the lateral distribution of beam intensity;
    2. The beam was carefully aligned to make sure that the sample could be placed in the uniform beam region.
  - Beam intensity was monitored before and during irradiation:
    1. Before irradiation, a Faraday cup was used for measurement;
    2. During irradiation, the current on the sample was monitored, then the exposure time could be adjusted according to the relative fluence.

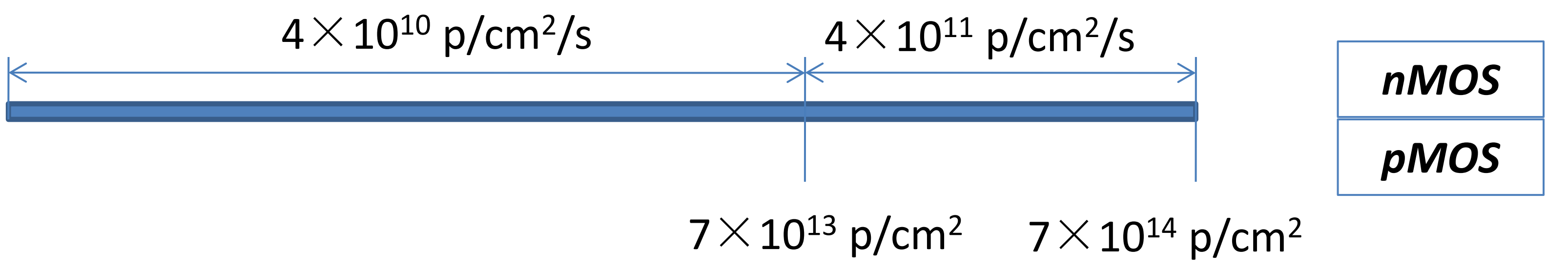
Experiment and devices description

- 65 nm MOS transistors
  - Designed by CERN, fabricated in TSMC, tested in Padova, size of the die: 1 mm × 3 mm
  - Wire-bonding performed by INFN-Padova (DIP28)
  - T_{ox}: 1.8 nm, V_{DD}=1.2 V

Geometry No.	**1**	**2**	**3**	**4**	**5**	**6**
nMOS transistors	600 nm /60 nm	480 nm /60 nm	360 nm /60 nm	240 nm /60 nm	120 nm /60 nm	
pMOS transistors	1 µm /60 nm	600 nm /60 nm	480 nm /60 nm	360 nm /60 nm	240 nm /60 nm	120 nm /60 nm

Experiment and devices description

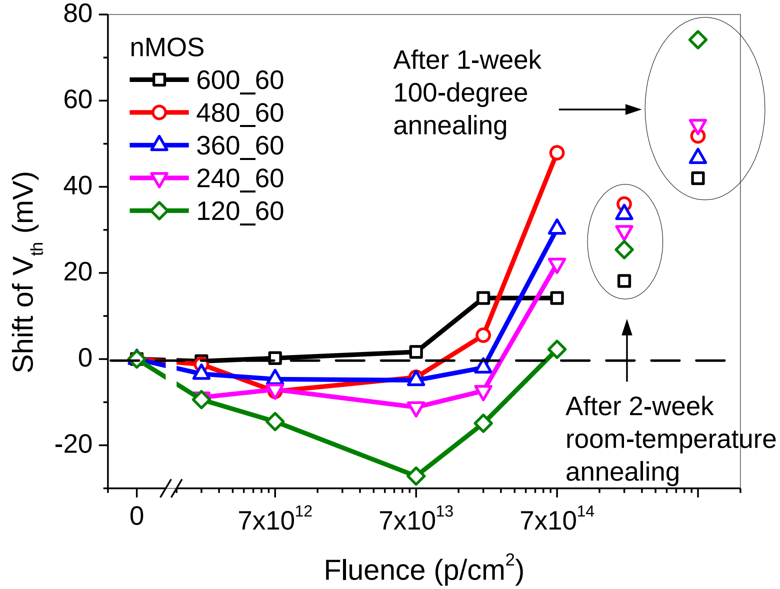
- Flux setup:



- Bias during Irradiation (worst-case for TID):
  - $V_G=V_{DD}$, $V_D=V_S=V_B=0$ V (nMOS)
  - $V_G=V_D=V_S=V_B=0$ V (pMOS)
- Annealing setup:
  - 2-week room-temperature annealing
  - 1-week high-temperature annealing (100 °C)

Results and discussion: 3 MeV proton

- nMOS transistors:

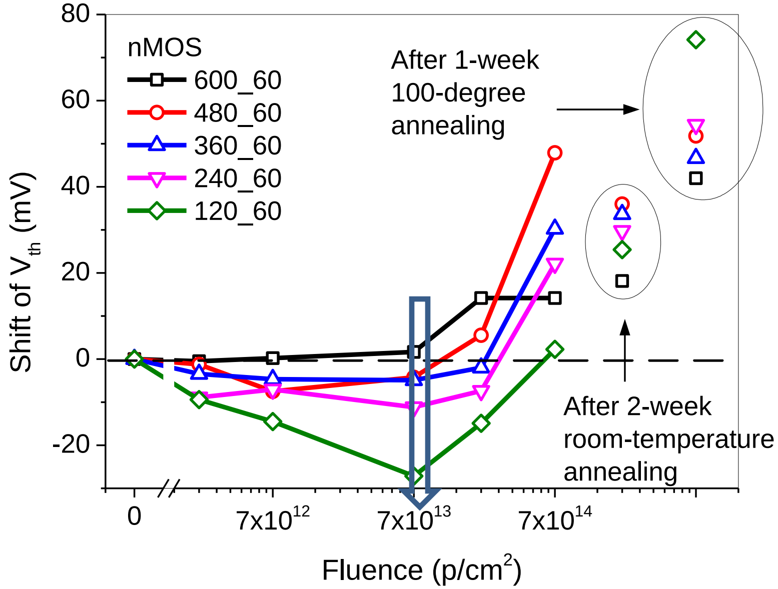


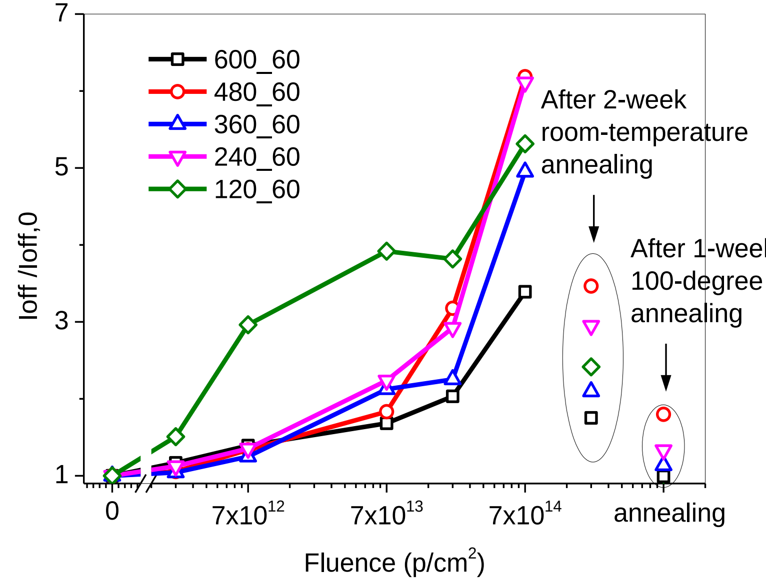
➢V_{th} shift during irradiation and after annealing for different nMOS transistor size.

  – During irradiation, a negative peak was shown in V_{th} shift, which is consistent with the TID mechanism in nMOSFET and due to the competition between the positive oxide trapped charge (N_{ot}) and the negative interface traps (N_{it}).
  – After annealing, both N_{it} & N_{ot} decreased, due to the faster decay of N_{ot}, ΔV_{th} is inclined to keep increasing.

Results and discussion : 3 MeV proton

- nMOS transistors:

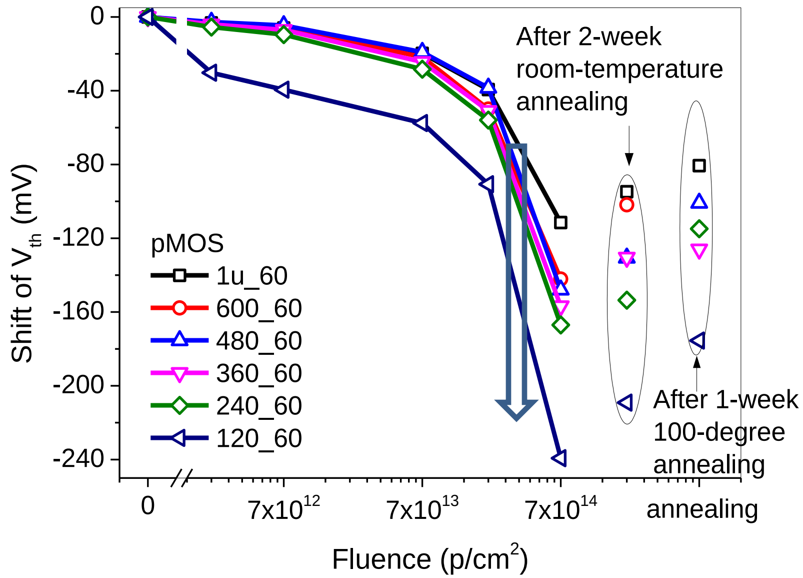


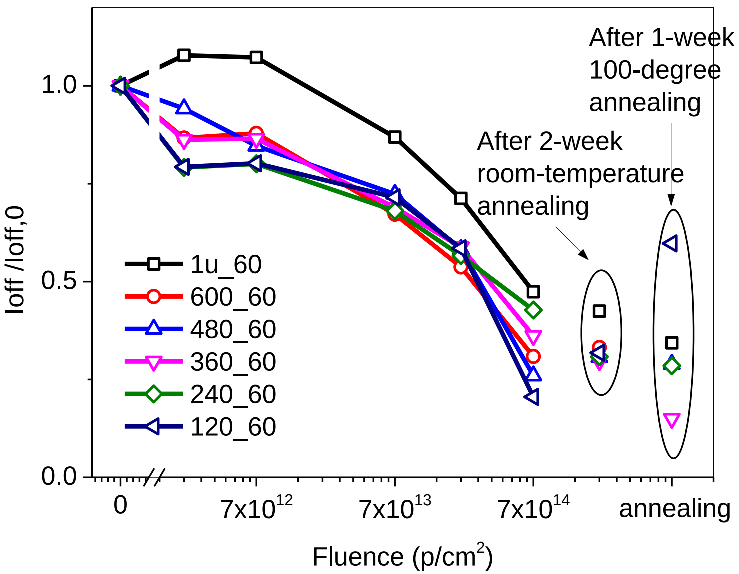


  - Radiation-induced narrow channel effect could be observed, suggesting the charge trapping in the STI oxide was the main mechanism.
  - I_{off} increased during irradiation and recovered after annealing, due to the charge balance in the STI oxide.

Results and discussion : 3 MeV proton

- pMOS transistors:

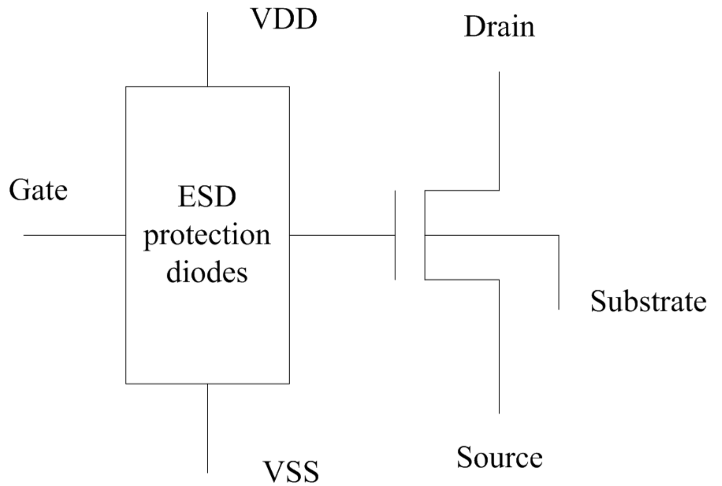


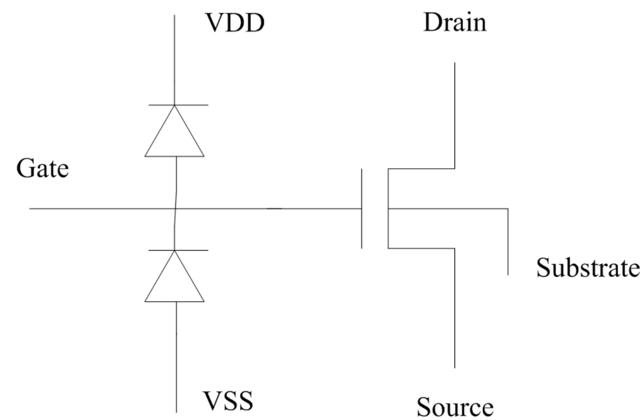


  - V_{th} shifted toward one direction during the whole procedure.
  - Radiation-induced narrow channel effect could be observed.
  - Decrease in I_{off} during irradiation could be observed.
  - The main mechanism was due to the positive N_{ot} and the positive N_{it} accumulated in the STI oxide;

Results and discussion: DD study

- From the results above, TID is the dominant radiation damage for 65 nm CMOS transistors under 3 MeV proton environment.
- It is difficult to evaluate the degradation level of the transistors only due to DD.



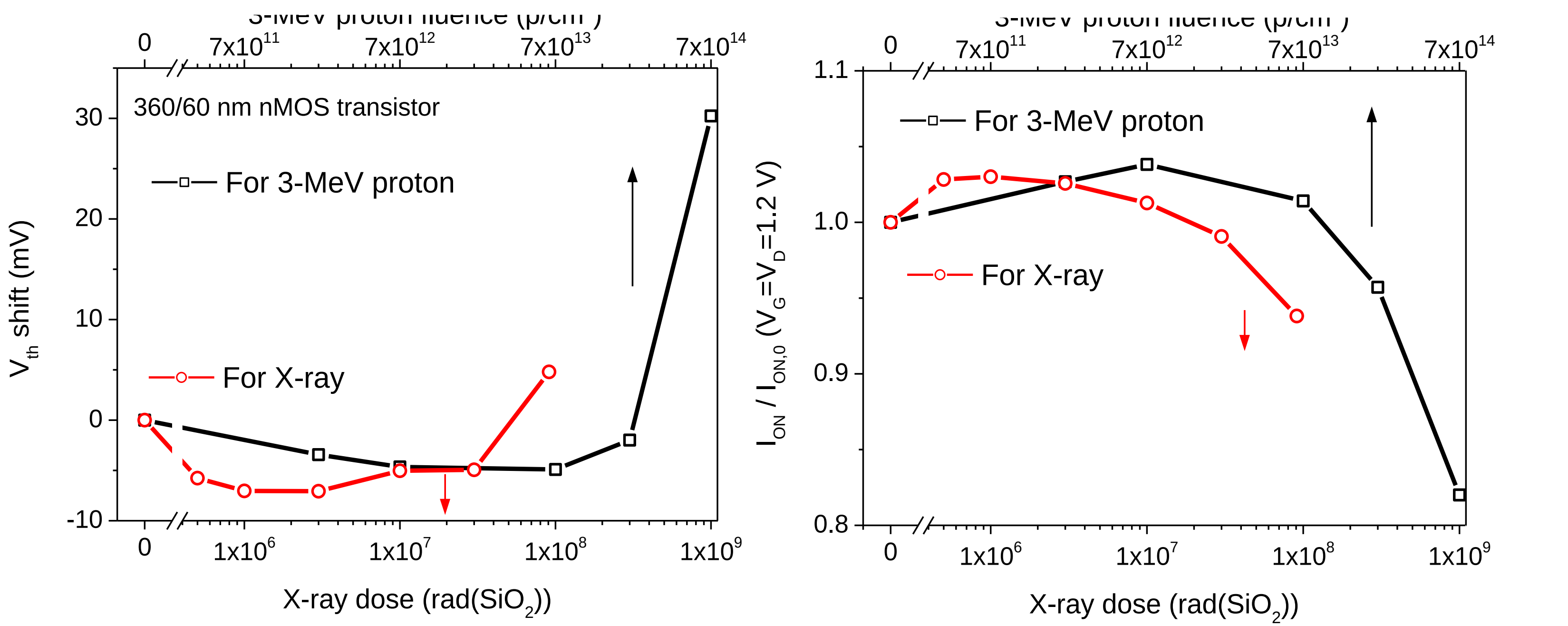


➢Schematic of ESD protection diodes.

- I_G was monitored to detect possible DD, the measured value was the sum of the real MOSFET gate current and the diodes leakage.

Results and discussion: proton v.s. X-ray

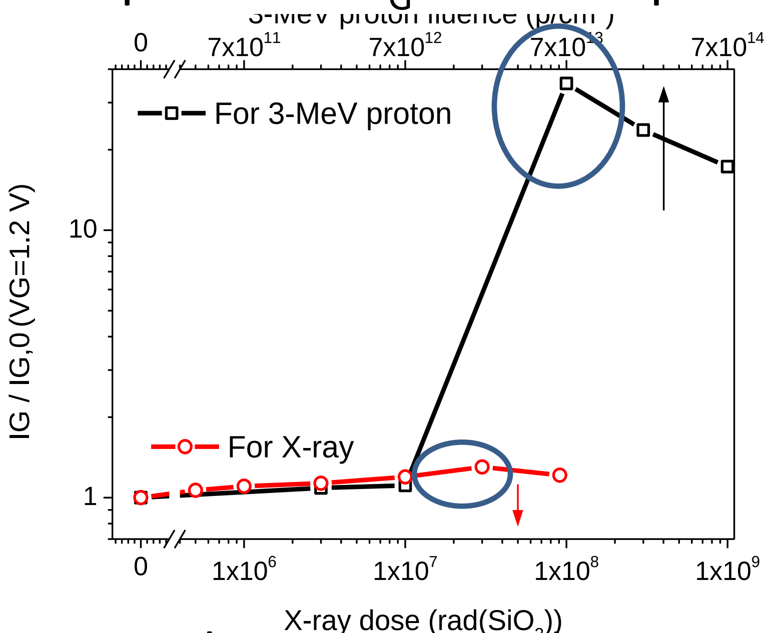
- X-ray irradiation results are introduced here:



- The values of fluence and dose are one-to-one correspondingly.
- After considering the difference in radiation source and dose rate, the degradations of MOS transistors are comparable under the two irradiation environments.

Results and discussion: proton v.s. X-ray

- Comparison of I_G between proton and X-ray:

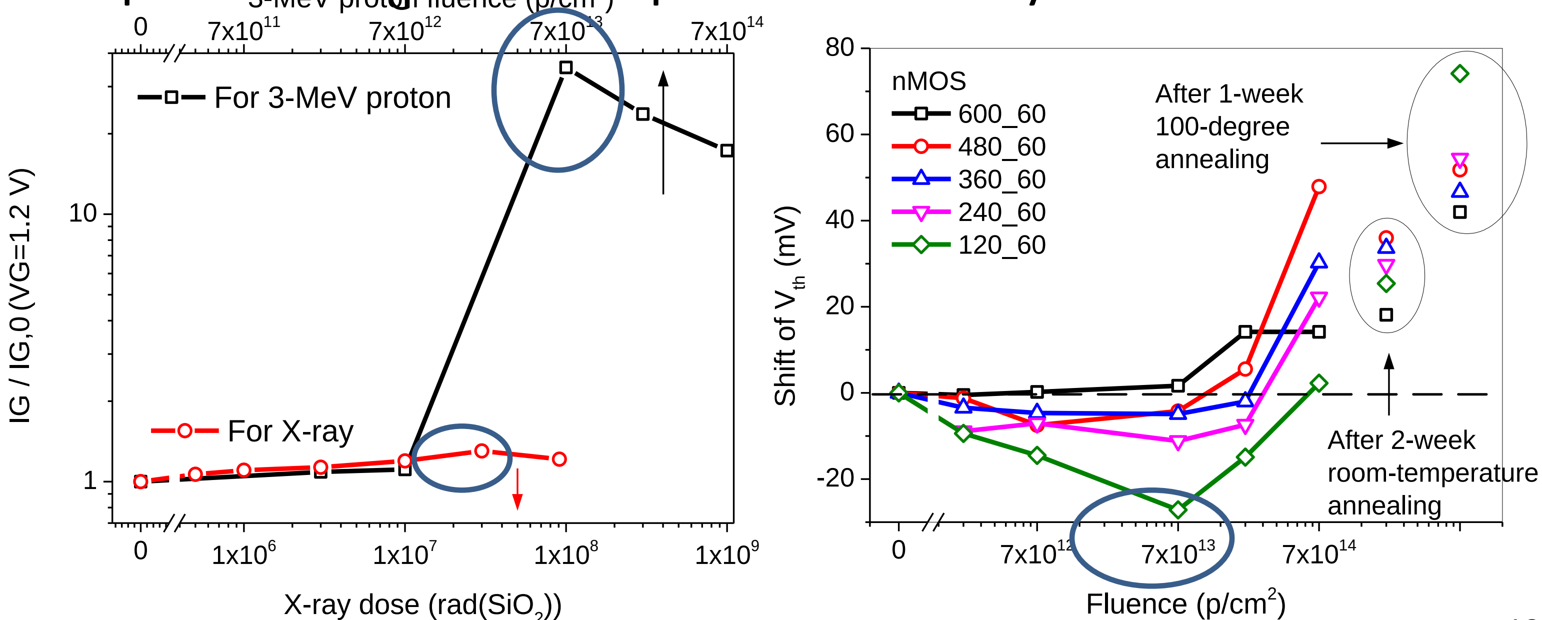


➢ $I_G/I_{G,0}$(with V_G=V_D=1.2 V) under 3-MeV proton and under 10-keV X-ray environments.
➢ I_G is independent of the gate width, indicating it is mainly due to the ESD protection diodes.

- During the proton irradiation tests, I_G first increased with the proton fluence, but then decreased after 7×10^{13} p/cm^2, indicating the influence of TID simultaneously.
- During the X-ray tests, I_G slightly increased with the total dose at first, but then a peak showed up.

Results and discussion: proton v.s. X-ray

- Comparison of I_G between proton and X-ray:



- For nMOS transistors, the rebound point also occurred around 7×10^{13} p/cm^2 ,suggesting the existence of peaks were due to TID.
- TID alone only induced low diodes leakage. When TID and DD contributed together, the radiation damage could be enhanced a lot, but only for devices which are sensitive to DD (e.g., bipolar devices).

Conclusion

- TID and DD effects in 65 nm CMOS transistors were investigated by means of 3 MeV proton.
- Corresponding to the high proton fluence (7×10^{14} p/cm^2), the 65 nm CMOS transistors showed visible TID-induced degradation.
- 10-keV X ray irradiation was performed for comparison, the results suggest that negligible DD could be observed for 65 nm CMOS transistors even for high proton fluence.
- When exposed to proton, DD of the ESD protection diodes was very likely modulated by TID.

Thanks