Measurements Results on a 180nm SOI Monolithic Active Pixel Sensor

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T. Hemperek, T. Kishishita, H. Krueger, N.Wermes (Bonn University)

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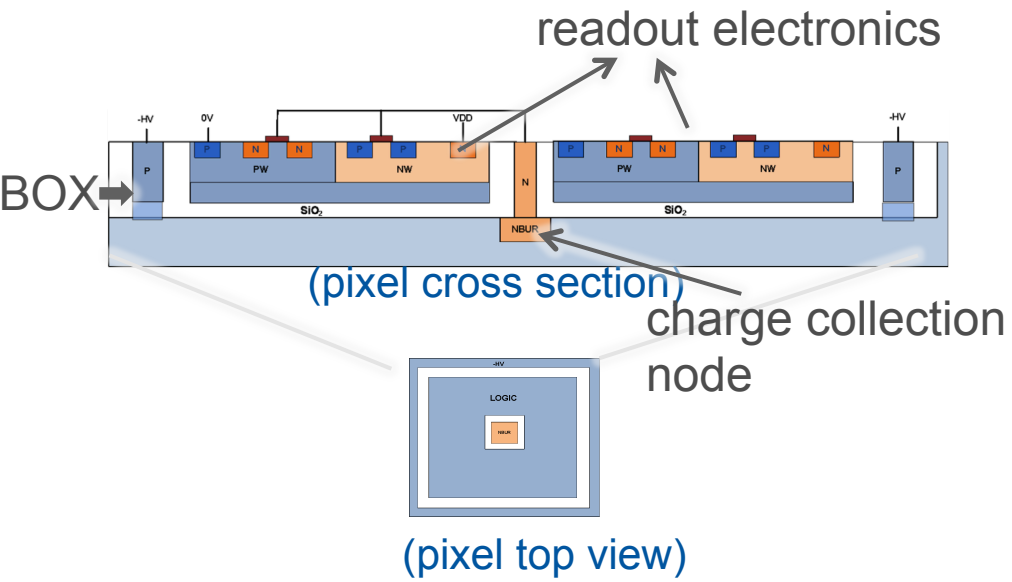
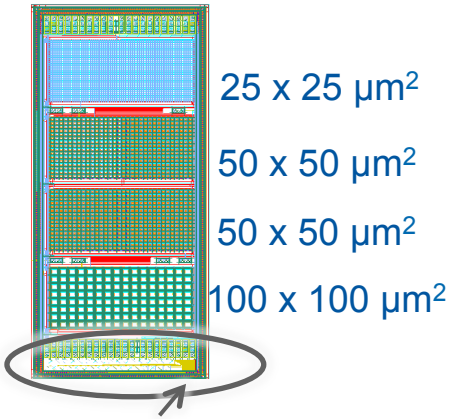
  - Fe55 spectrum
- Summary & outlook

Prototype: XTB01

Idea + Design:
T. Hemperek,
T. Kishishita (Bonn)

(See T.Hemperek talk)





- Chip: 300 µm thick
- Size: 5 x 2 mm^2
- 4 matrixes with different pixel sizes: 100×100 µm^2 , 50×50 µm^2 (x2), 25×25 µm^2
- 3 types of readouts (in testing 3T cell)

- Feature size: 180 nm
- Double well structure to isolate transistors-BOX
- Transistors test structure: normal + enclosed MOSFET
- p-type bulk, 4 metal layers
- Resistivity ~ 100 Ω cm
- HV applied on top (no implants on the backside)

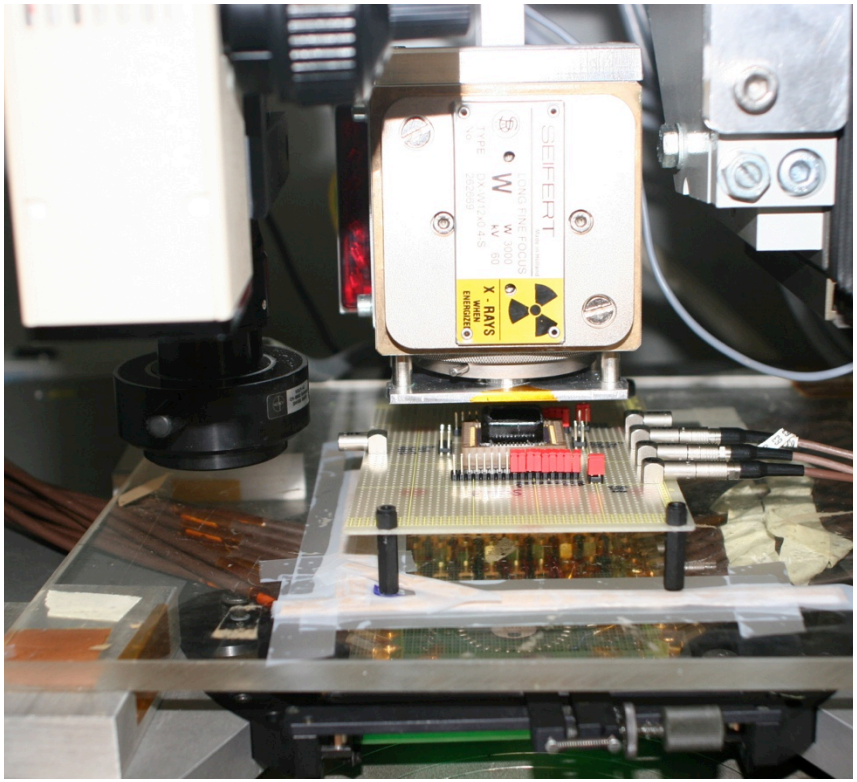
Radiation hardness of SOI transistors

- Transistor's performance degrade due to charge accumulation in SiO_2 and Si-SiO_2 interface.
- The electrical parameters of a transistor shifts due to irradiation
- SOI transistors have an extra layer of oxide bellow its channel (BOX)

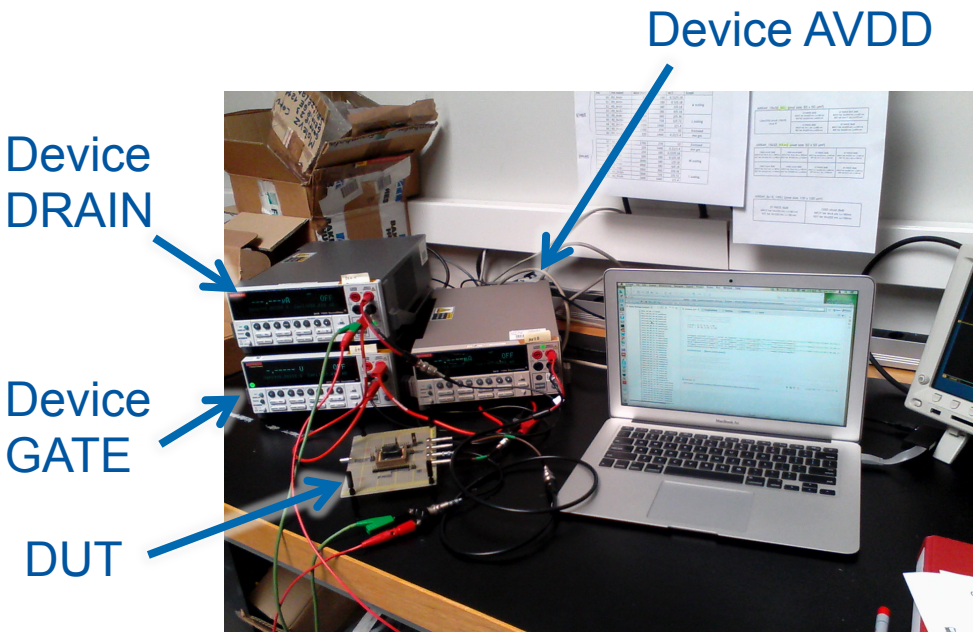
→ This limits the performance of SOI technologies ("back gate effect")

Radiation hardness of SOI transistors - setup

X-rays setup



Transistor's characterization setup



Radiation hardness of SOI transistors - Irradiation procedure

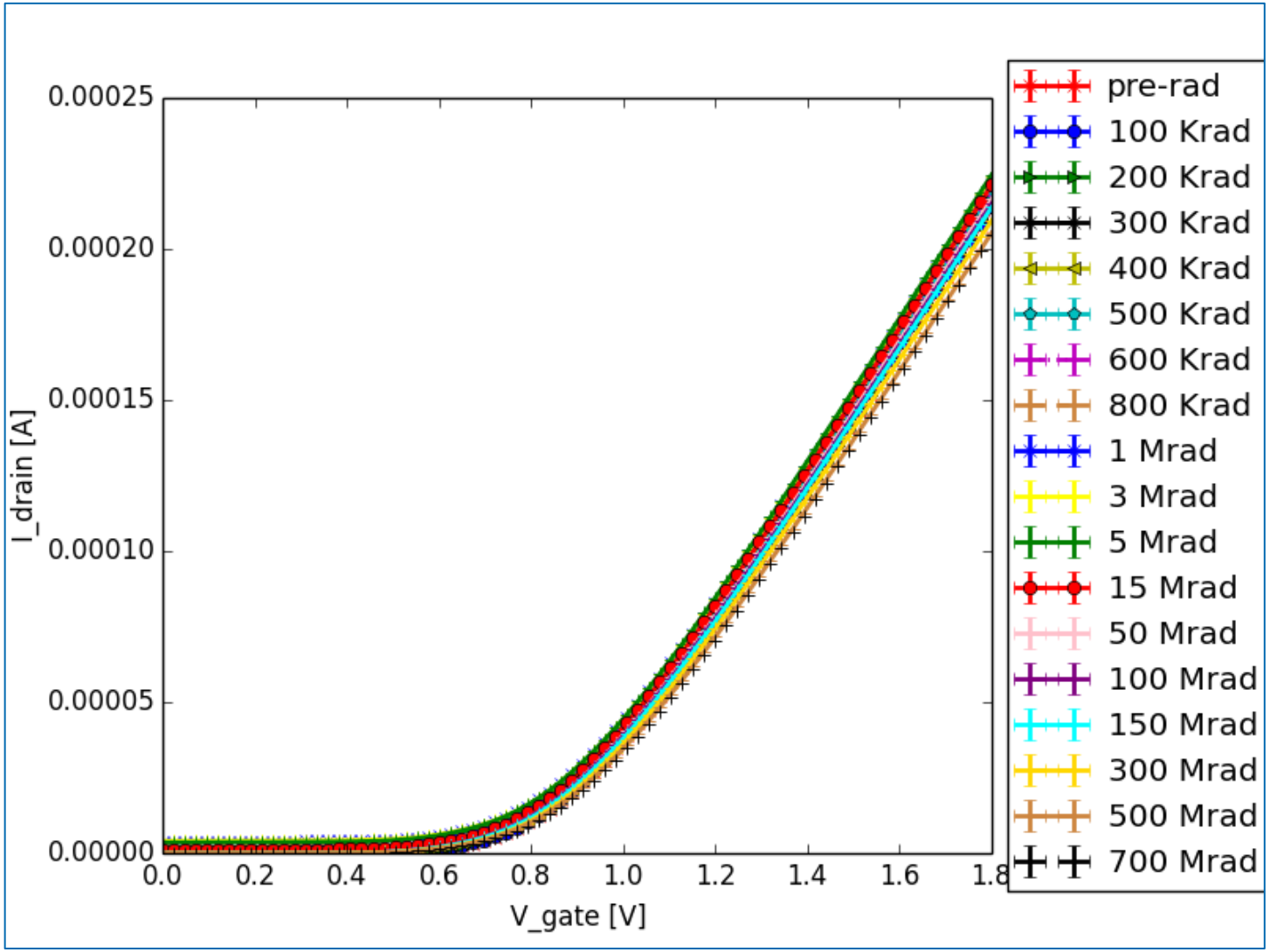
Special thanks to:
M. Barbero (CPPM)
P. Pangaud (CPPM)
F. Faccio (CERN)

- 2 irradiation campaigns performed up to 700Mrad
- Dose rate up to 8MRad/h (2cm – 40 KV – 50mA)
- Bias condition during irradiation

Option A (chip#3)	Option B (chip #6)
NMOS: Vg=1.8V; Vd,Vs =0V (ON)	NMOS: Vg=0V; Vd,Vs =0V (OFF)
PMOS: Vg=1.8V; Vd,Vs =1.8V (OFF)	PMOS: Vg=0V; Vd,Vs =1.8V (ON)

- Procedure → **Standard test method ESA/SCC BS 22900**
  - Dose steps: 100- 600 Krad (100Krad step), 800Krad,1Mrad, 3Mrad, 5Mrad, 15Mrad, 50Mrad, 100Mrad, 150Mrad, 300Mrad, 500Mrad, 700Mrad

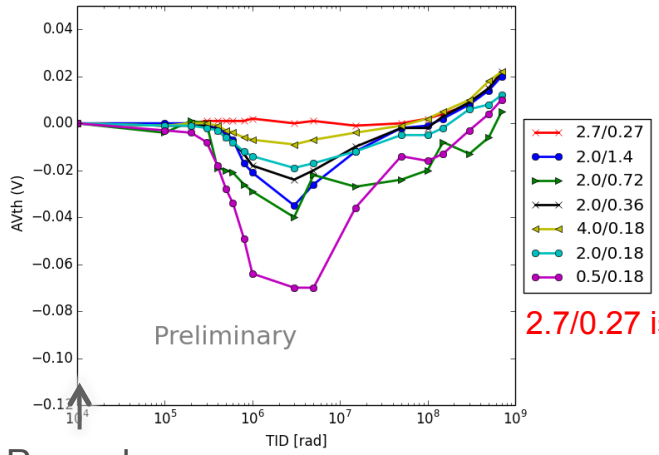
Radiation hardness of SOI transistors - Transistor 0.5/0.18 NMOS - Characteristics



Chip 3

Radiation hardness of SOI transistors – Threshold RESULTS

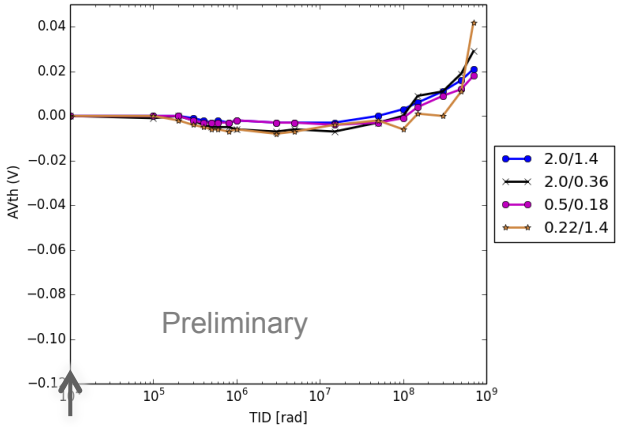
Bias option A (NMOS ON)



2.7/0.27 is EGT

Pre-rad

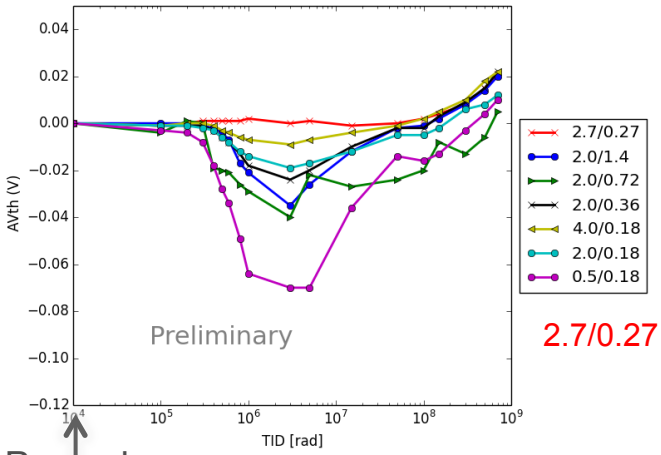
Bias option B (NMOS OFF)



Pre-rad

Radiation hardness of SOI transistors – Threshold RESULTS

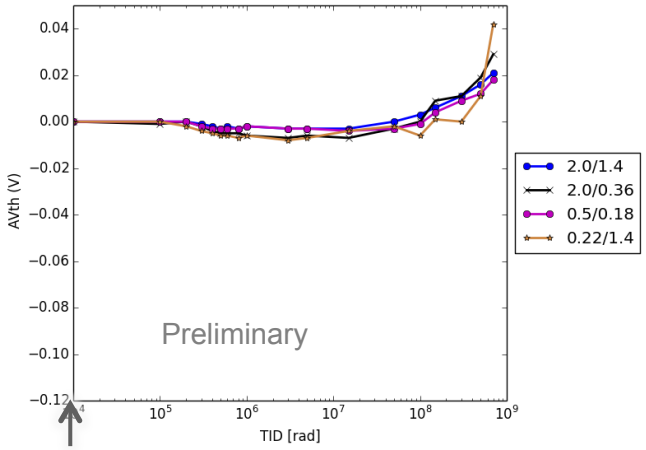
Bias option A (NMOS ON)



2.7/0.27 is EGT

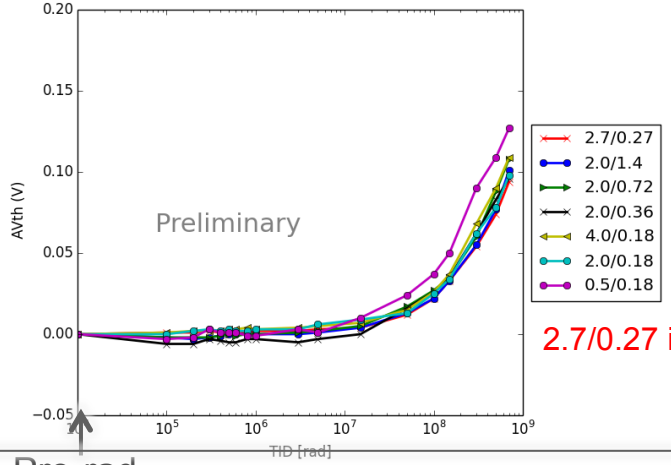
Pre-rad

Bias option B (NMOS OFF)



Pre-rad

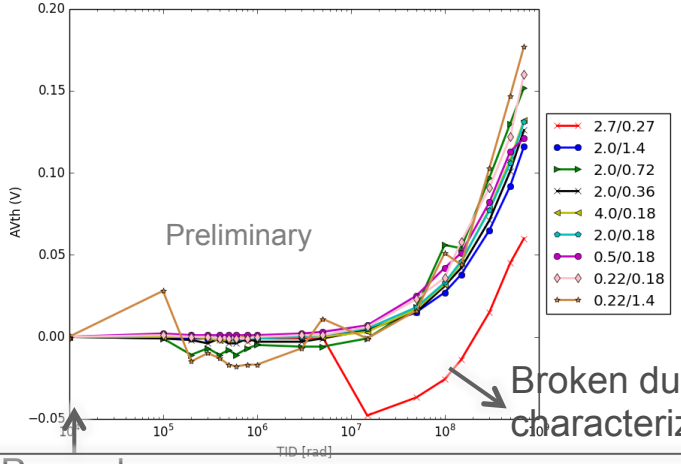
Bias option A (PMOS OFF)



2.7/0.27 is EGT

Pre-rad

Bias option B (PMOS ON)

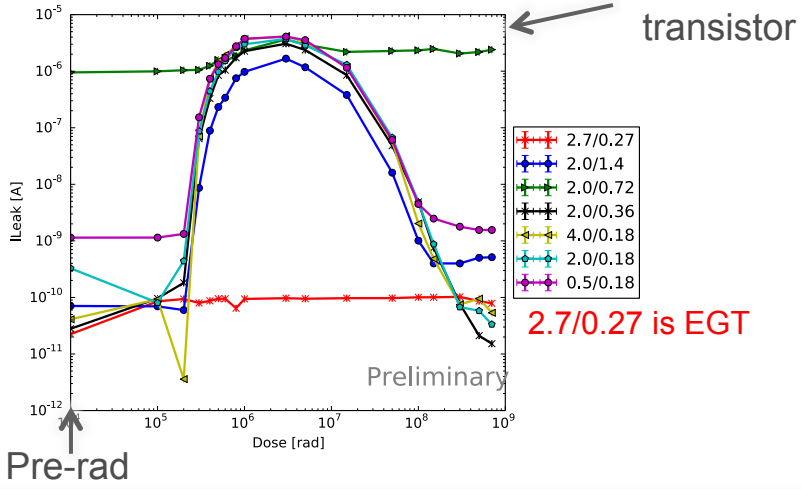


Broken during characterization

Pre-rad

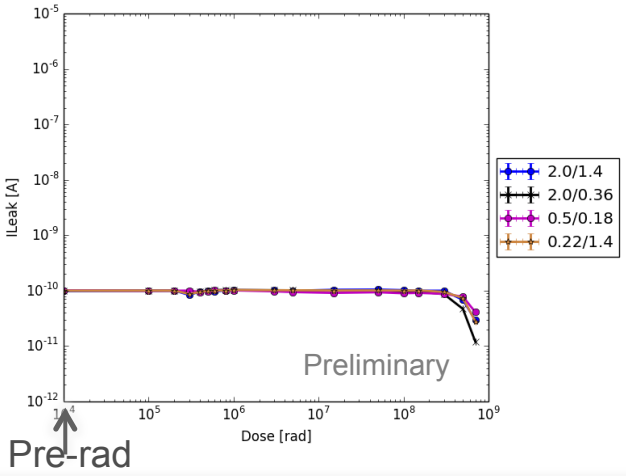
Radiation hardness of SOI transistors – Leakage RESULTS

Bias option A (NMOS ON)



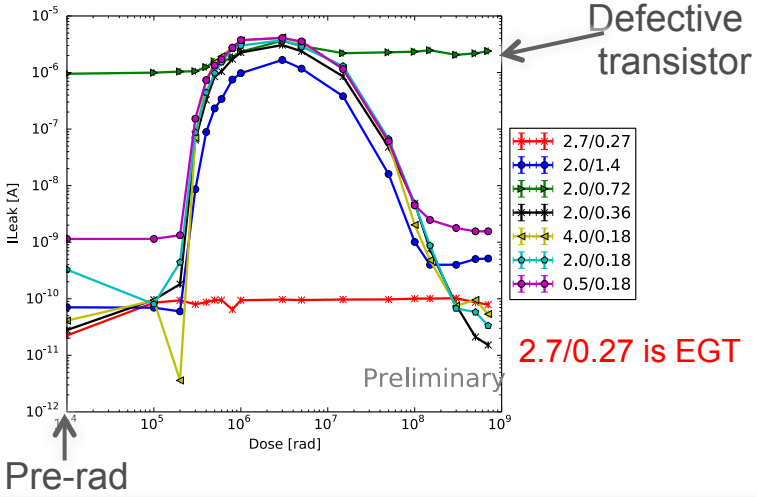
2.7/0.27 is EGT

Bias option B (NMOS OFF)



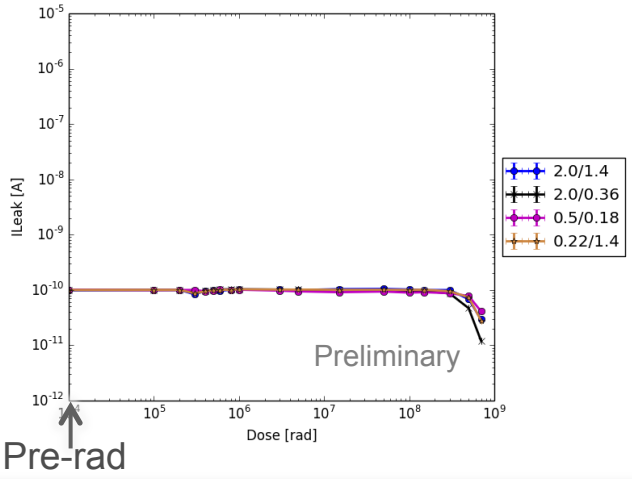
Radiation hardness of SOI transistors – Leakage RESULTS

Bias option A (NMOS ON)

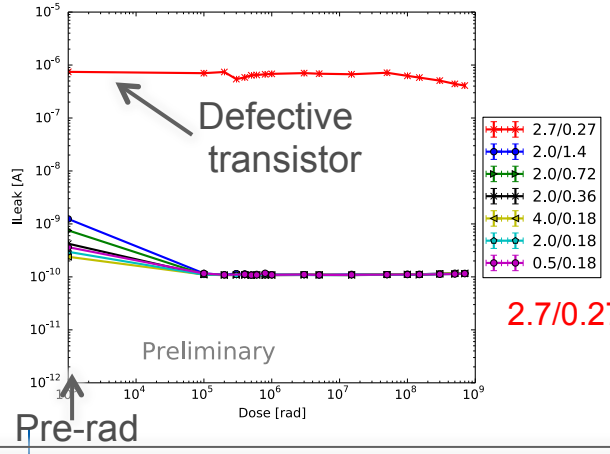


2.7/0.27 is EGT

Bias option B (NMOS OFF)

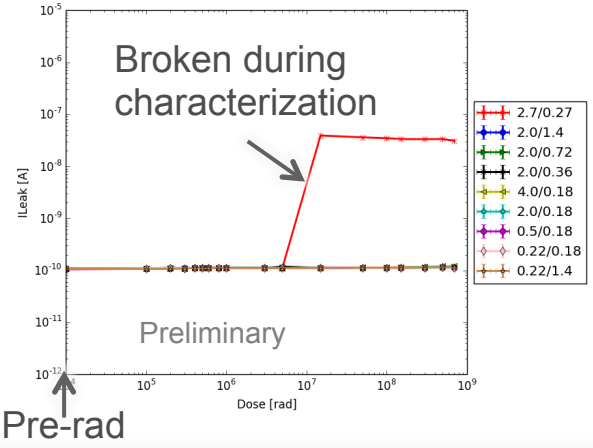


Bias option A (PMOS OFF)



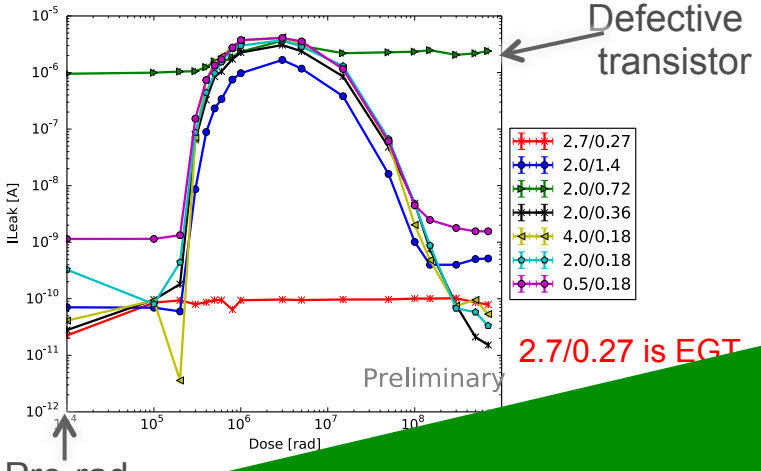
2.7/0.27 is EGT

Bias option B (PMOS ON)



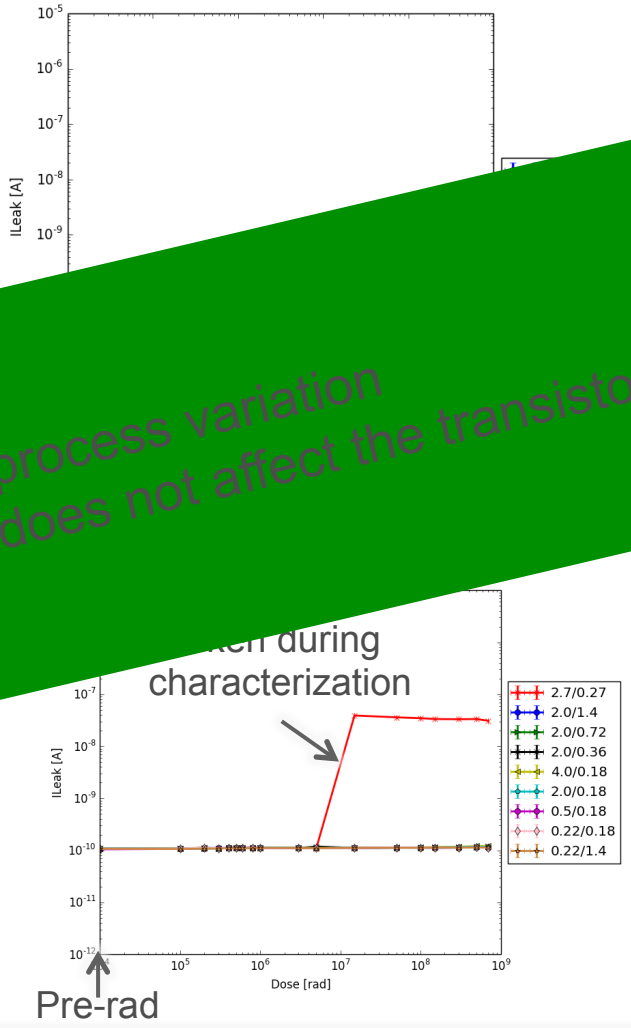
Radiation hardness of SOI transistors – Leakage RESULTS

Bias option A (NMOS ON)



2.7/0.27 is EGT

Bias option B (NMOS OFF)



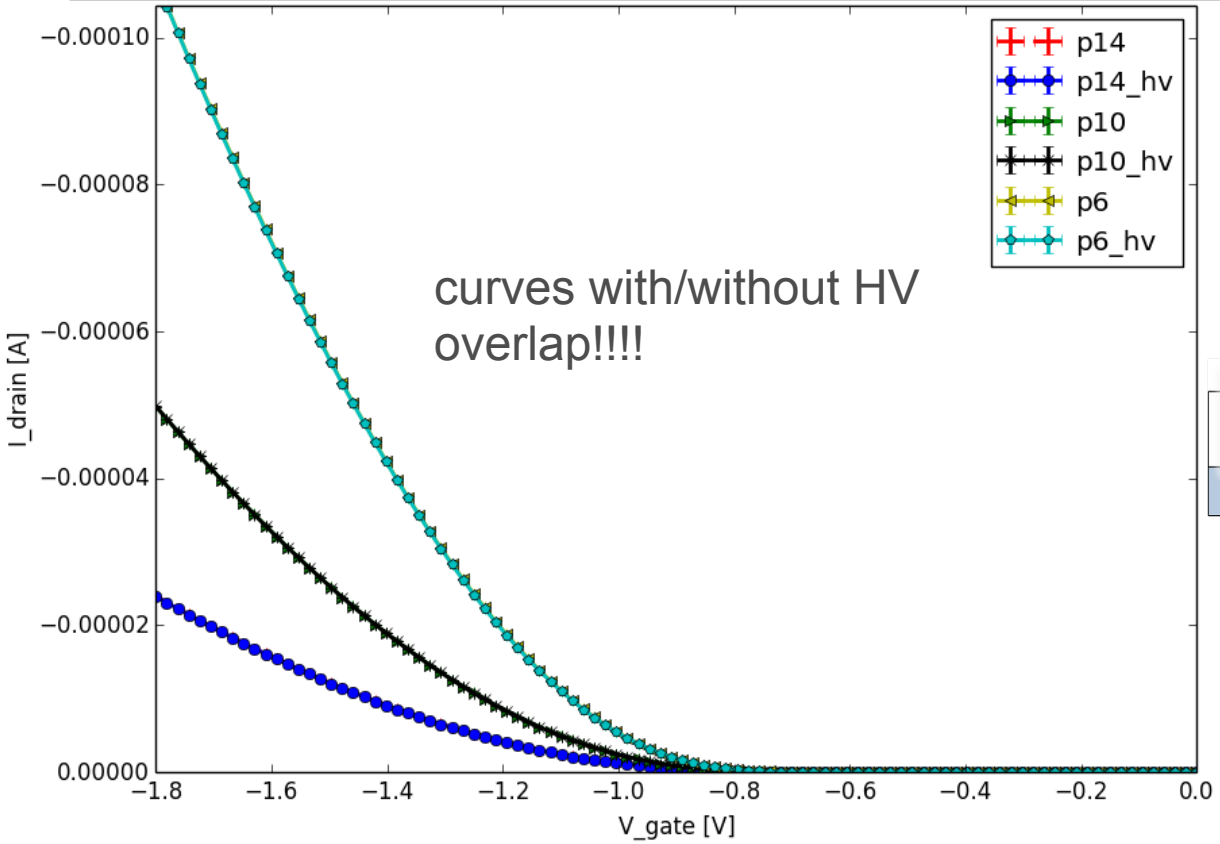
2.7/0.27 is EGT

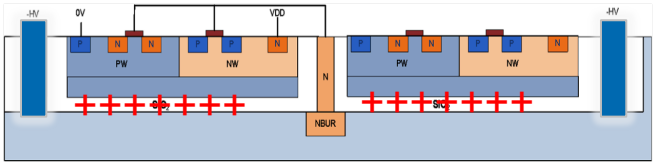
Conclusion:

- The transistor parameter shifts within process variation
- The accumulation of positive charges does not affect the transistor parameters

Radiation hardness of SOI transistors – Characteristics with diode floating / HV

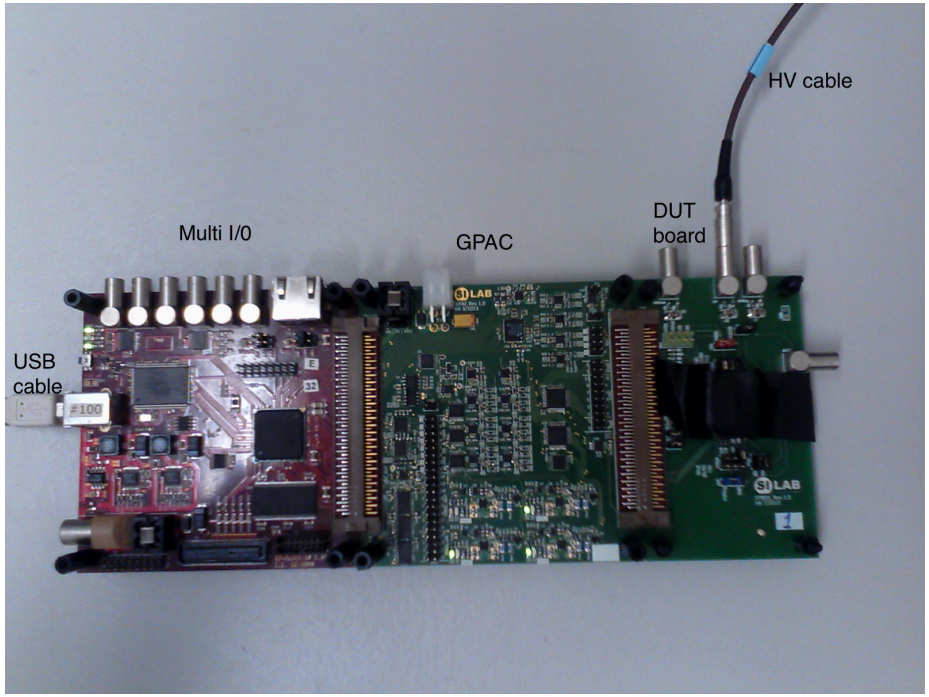
Irradiated chip – with/ without -40V on the sensor diode





- This proves that the electronic part is shielded from the electrical field in the sensor diode

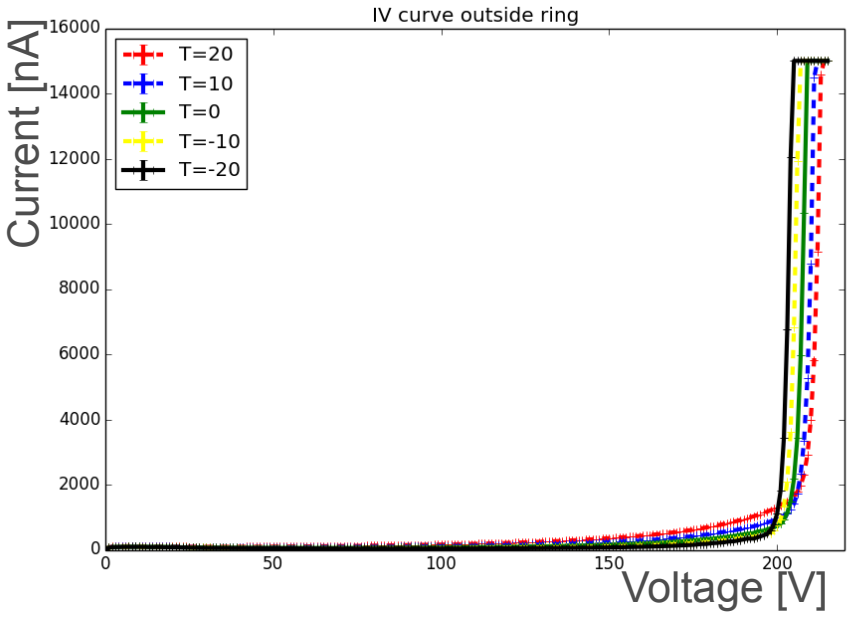
Sensor characterization - setup



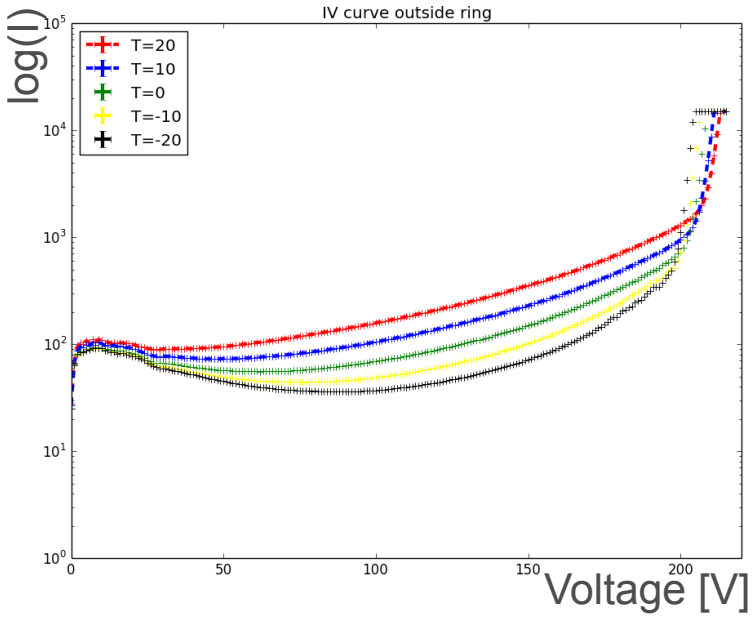
Test system (developed in Bonn):

- Multi I/O board
- General Purpose Adaptor Card(GPAC)
- Device Under Test (DUT) board
- Python software based on Basil framework

IV curves at different T

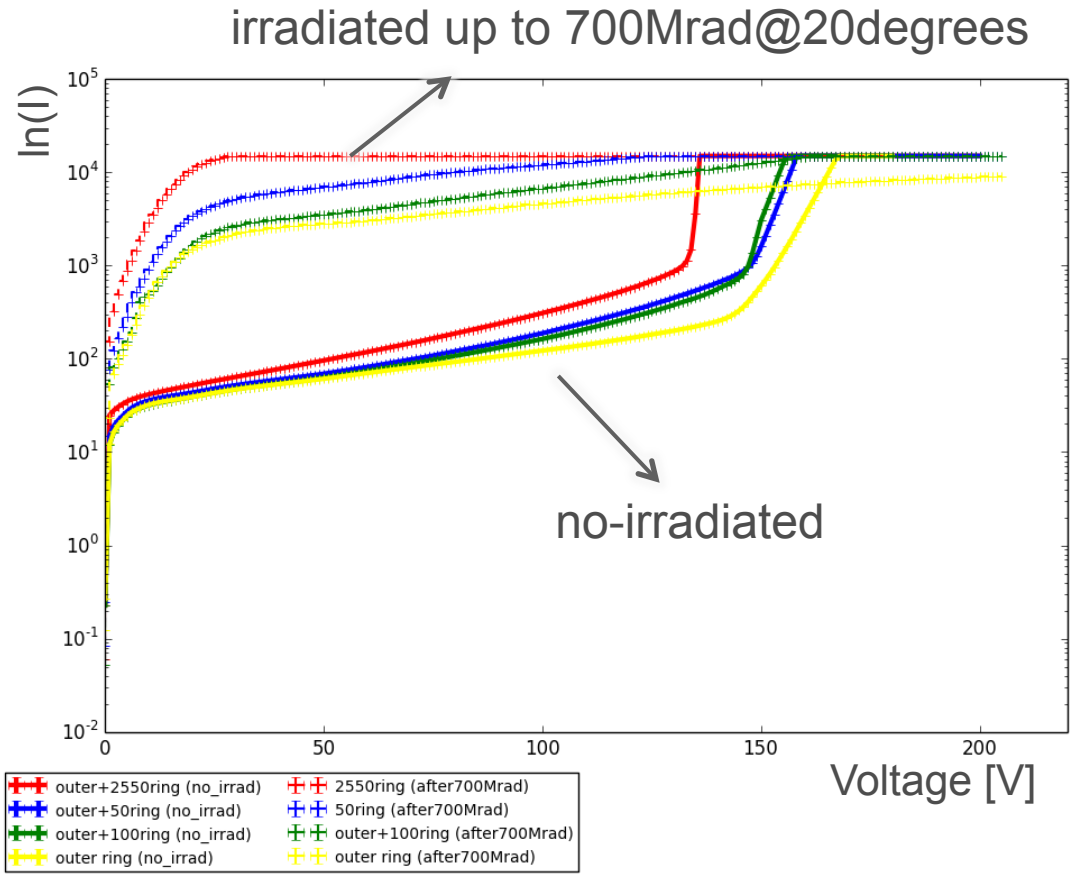


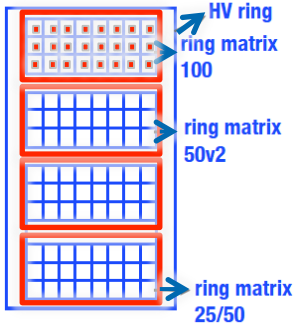
Log scale



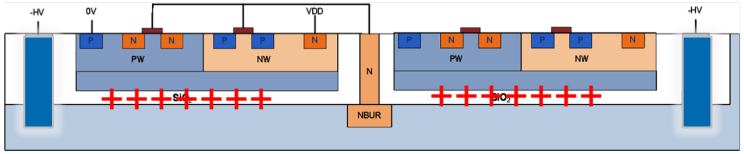
- The prototype stands -200V
- Leakage scales with T
  → Drift / diffusion leakage contribution and surface current under investigation

IV curves in an irradiated/ no-irradiated sample



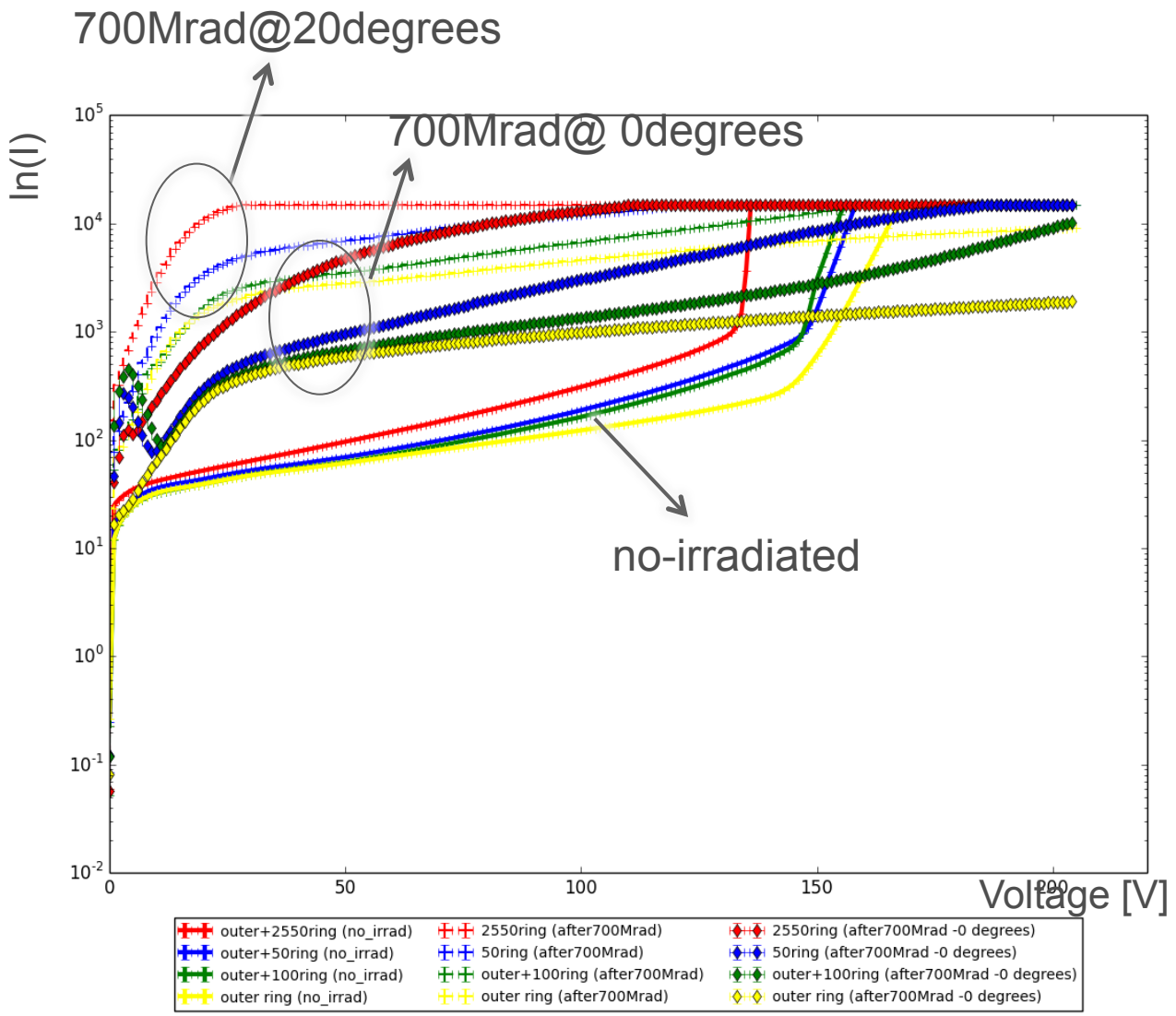


Blue – HV rings (p+)
Red – n+ implants



- The accumulation of positive charges in the BOX due to 700Mrad creates a channel in the $Si0_2$-Si interface → decrease band gap → increases leakage
- Improvement implemented in the next prototype

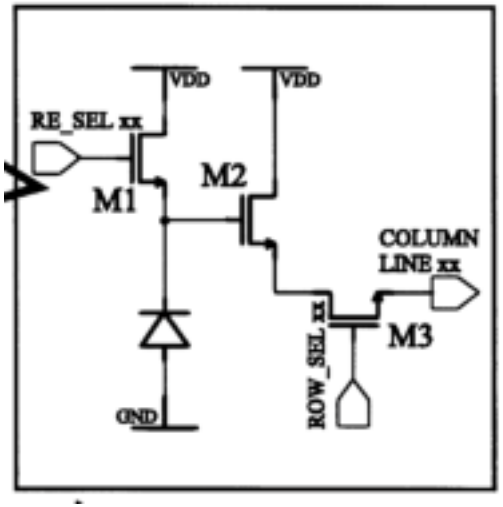
IV curves in an irradiated/ no-irradiated sample



- Leakage current still scales with T

Spectrum Fe55 in a pixel

Pixel readout



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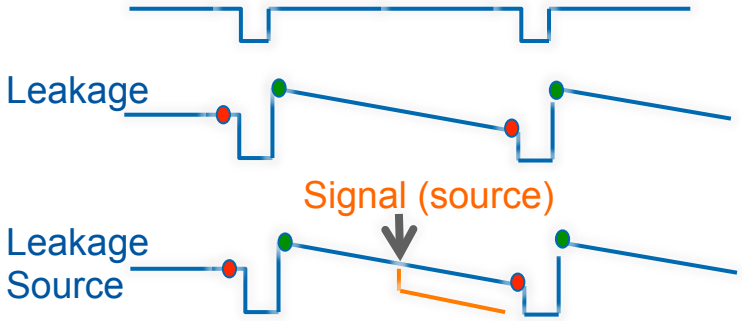
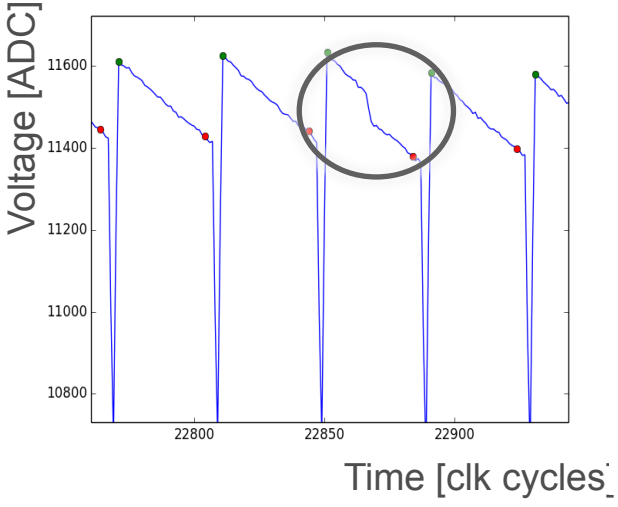
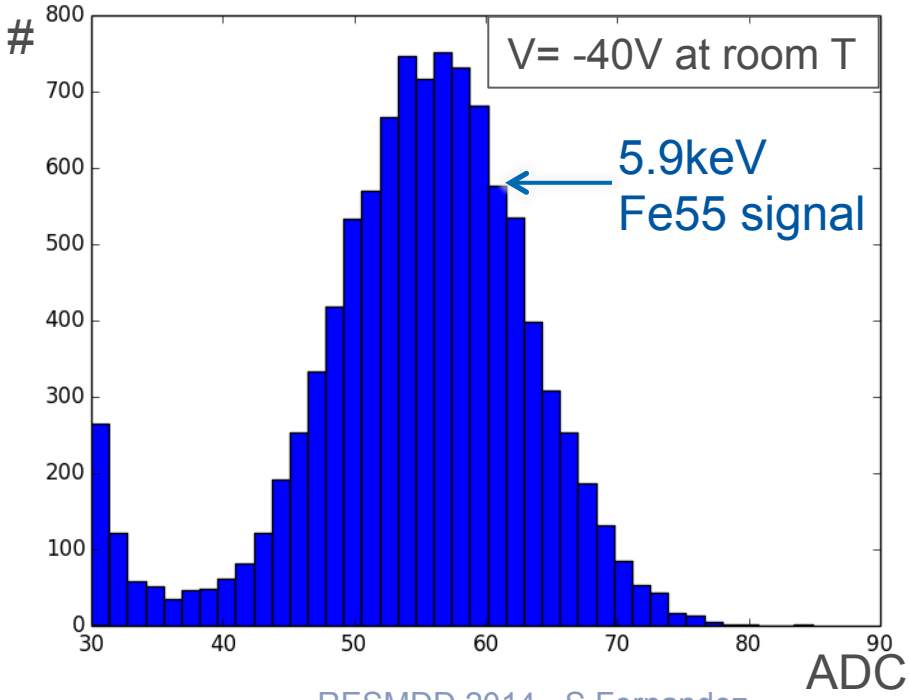
Pixel analog signal







Measurement results - Summary

- **Radiation hardness of 180nm SOI transistors**

  → All results consistent within non SOI technologies (FEI4/IBM 130nm)
  → Parameters shift within process variation up to 700Mrad
  → Transistors are shielded from: the charge accumulation of the BOX and electrical field in the sensor diode.

- **Sensor characterization**

  → Chip stands 200V.
  → Sensor is not shielded from charge accumulation of the BOX (leakage increases a 50 factor)
  → Charge collection proved with Fe55

Outlook

- **Characterization of irradiated samples (Ljubljana, neutrons)**
- **eTCT measurements are foreseen (M.Moll facility, CERN)**
  - → Depletion region
  - → Drift/diffusion signal contribution
- **Test-beam foreseen (SPS November)**

Thanks for your attention

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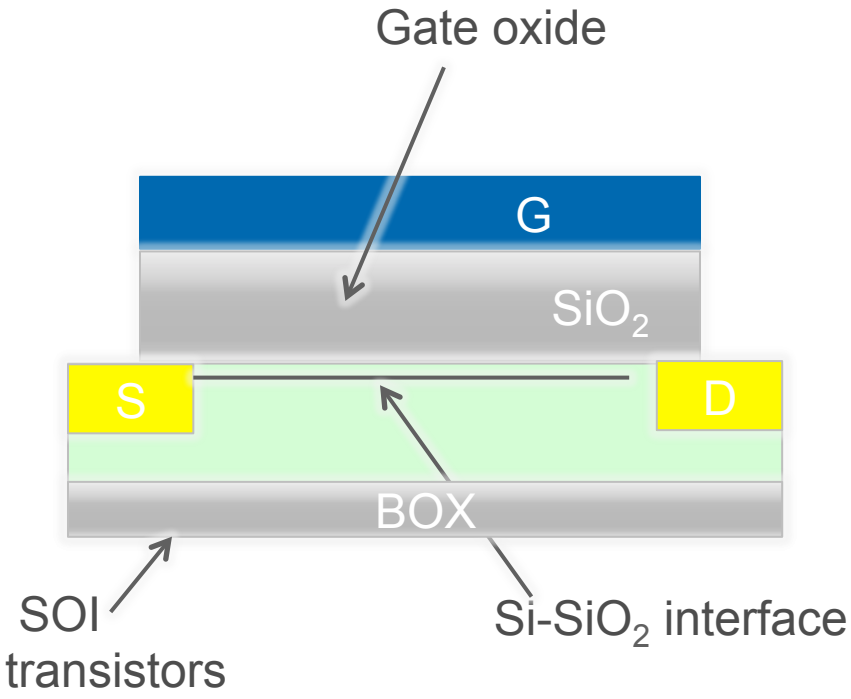
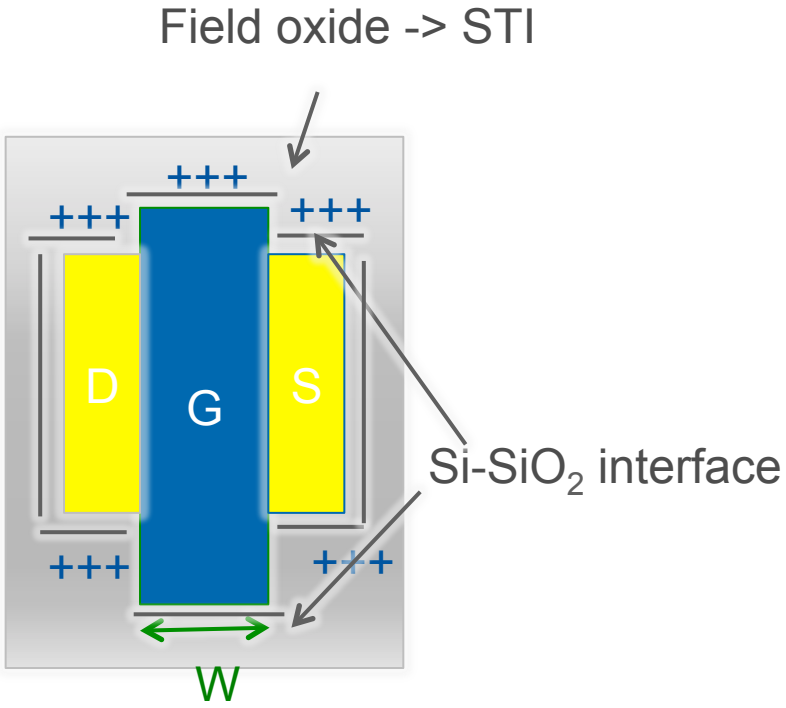
Backup

Radiation damage in MOSFET

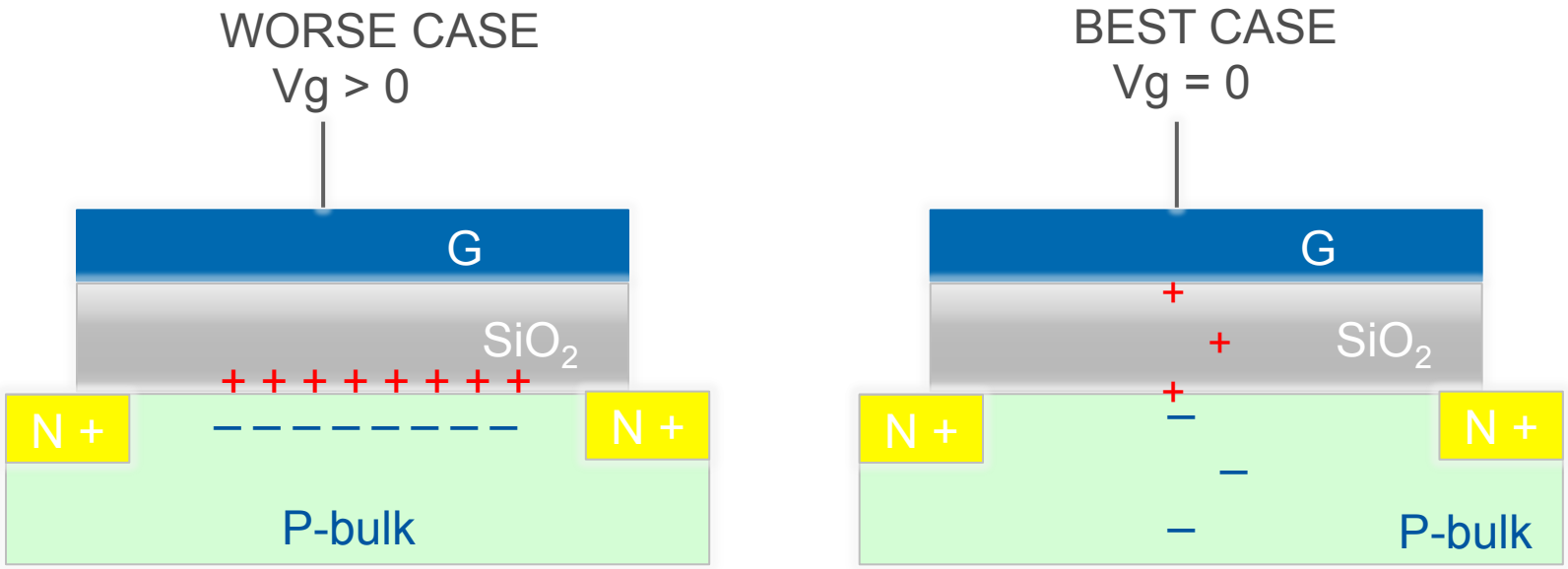
1. Positive charges trapped in the oxide -> parasitic currents
2. Traps in the Si-SiO_2 interface

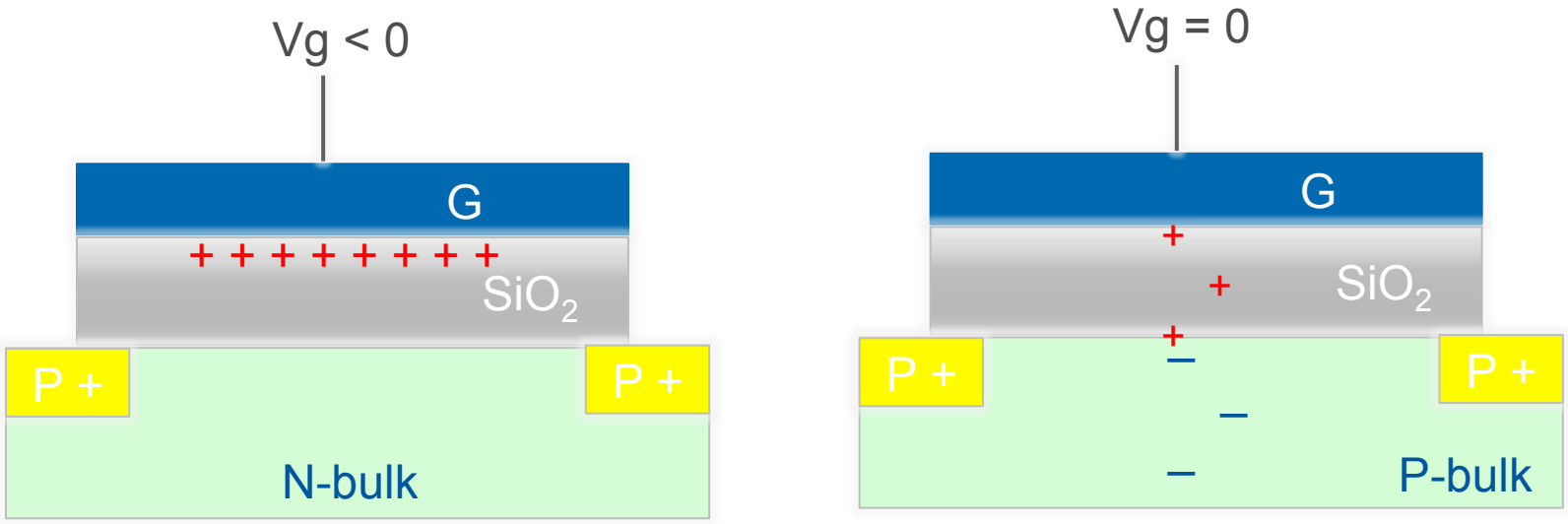




- Bias conditions during irradiation are crucial !!

Bias conditions (NMOS)



Bias conditions (PMOS)

Nowadays it is not clear what is worst bias condition → Oxide thickness dependent (In IBM 130nm PMOS OFF worst)