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HV-CMOS hybridisation and UK tracker R&D plans

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Outline

Will give a brief overview of LC Tracker R&D plans in the UK.

This is not a report on behalf of all UK groups interested in LC. Rather, my personal impressions of recent activities and plans with some inputs from Aidan Robson, Richard Bates, Joel Goldstein and Georg Viehhauser.

Also asked to report specifically on Liverpool HV-CMOS hybridisation plans, which I'll do as part of the above.

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UK LC activities

UK particle physics groups are keen to (re)build a strong involvement with preparations for detectors for a linear collider.

In process to submit an SoI to STFC to obtain moderate funding to start activities in a few targeted areas. One of these areas is the tracking. The focus is on ILC, but there is an obvious overlap with CLIC.

Note that a positive reception of this SoI, even if it brings little funding, allows institutes to spend a bit more of existing effort on LC related work.

Tracking

UK has contributed significantly to Silicon trackers for the LHC (ATLAS and CMS strips, LHC-b VeLo and their upgrades)

- Sensor R&D
- Development electronics
- Module design
- Full detector engineering

Based on current R&D interests in the UK, institutes propose to contribute to the design and engineering of a linear collider tracking detector and pursue CMOS technology solutions for the sensors. Also keen to contribute work on layout optimisation.

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Sensors

UK strengths

- Long experience in MAPS pixel sensors (RAL, Oxford, Bristol)
- More recently substantial investment in HV/HR-CMOS, focussed on hybrid sensors (Glasgow, Liverpool)
- Strong infrastructure for sensor characterisation, irradiation, ..

CMOS technologies

MAPS sensors for pixel tracker.

Strong UK interest in MAPS pixel tracker led by RAL. Primarily targeting ILC. Potential for very high granularity large area detector at reduced cost (compared to planar sensors). Interest to use HR substrates to improve radiation tolerance (and timing performance at the same time)

Hybrid HV/HR-CMOS sensors

Hybrid implementation allows for flexible pixel/strip layout

HV-CMOS should give good timing performance

Significant funding in UK for generic R&D on HV-CMOS (Glasgow, Liverpool). Also expect to have significant HV-CMOS component in AIDA2020 with a strong UK participation.

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UK HV/HR CMOS planned activities

- Device characterisation: in lab, with source, x-rays, test-beam,..
- .. hand-in-hand with device simulation to understand and optimise devices
- Device design and submissions:
  - Contribute to design devices for CLICPix
  - Develop devices with dedicated geometry for tracking layers, position encoding,..
- Work on hybridisation:
  - Produce and test capacitively coupled HV-CMOS-to-ROIC assemblies
  - Identify suitable (flip-chip) equipment to develop an R&D to optimise bonding process, choice of dielectric, ..

Design and engineering

Strong infrastructure and expertise for large tracker projects

- Module/stave design (ATLAS SCT and strip upgrade, LHC-b VeLo)
- Engineering of larger structures: SCT Barrels and disks, ATLAS upgrade staves
- Assembly projects: ATLAS SCT module production and assembly of barrel and one endcap, LHCb VeLo module production

Very interested in contributing to the tracking detector for a linear collider detector. Highly challenging in terms of mass, stability, air cooling,

Hope to put some effort of physicists, design engineer and technicians on this.

Summary

UK groups are trying to (re)build a strong LC R&D.
Primary focus on ILC but strong overlap with CLIC programme.

Positive reception of SoI by STFC would allow us to put a more effort than so far.

Keen to open the discussion with others groups to see how the UK groups could best contribute to existing efforts.

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