AGH UNIVERSITY OF SCIENCE AND TECHNOLOGY

ASIC development at AGH-UST

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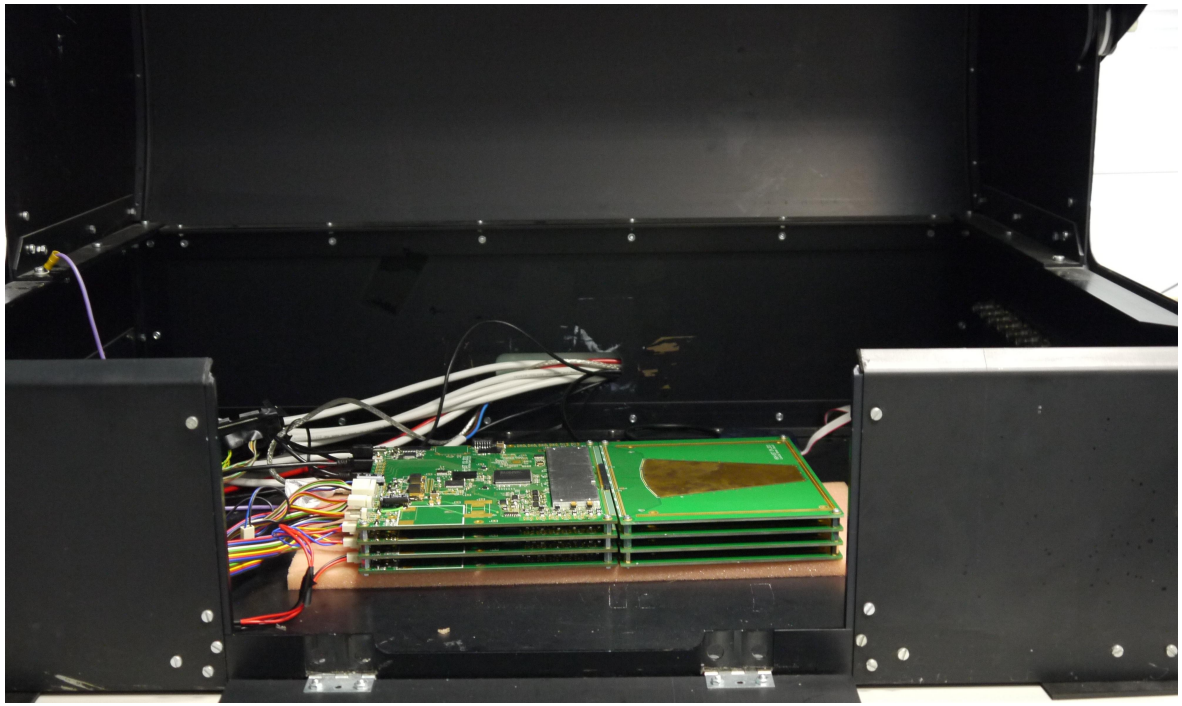
CLICdp Collaboration Meeting 10-11 June 2014 CERN

Outline

- Works on muli-plane FCAL detectors (with old readout ASICs)
- Works on front-end/readout ASICs in CMOS 130nm
  - Front-end R&D (preamp&shaper) in IBM nm
  - ADC, PLL R&D in IBM 130 nm
  - Multichannel readout R&D in IBM 130 nm
  - IBM , TSMC issues
- Pixel R&D in SOI
- Summary

In the spirit of the collaboration meeting aspect, presentations are expected to report on new work, work in progress and work plans relevant for CLIC, rather than conference-style overview presentations.

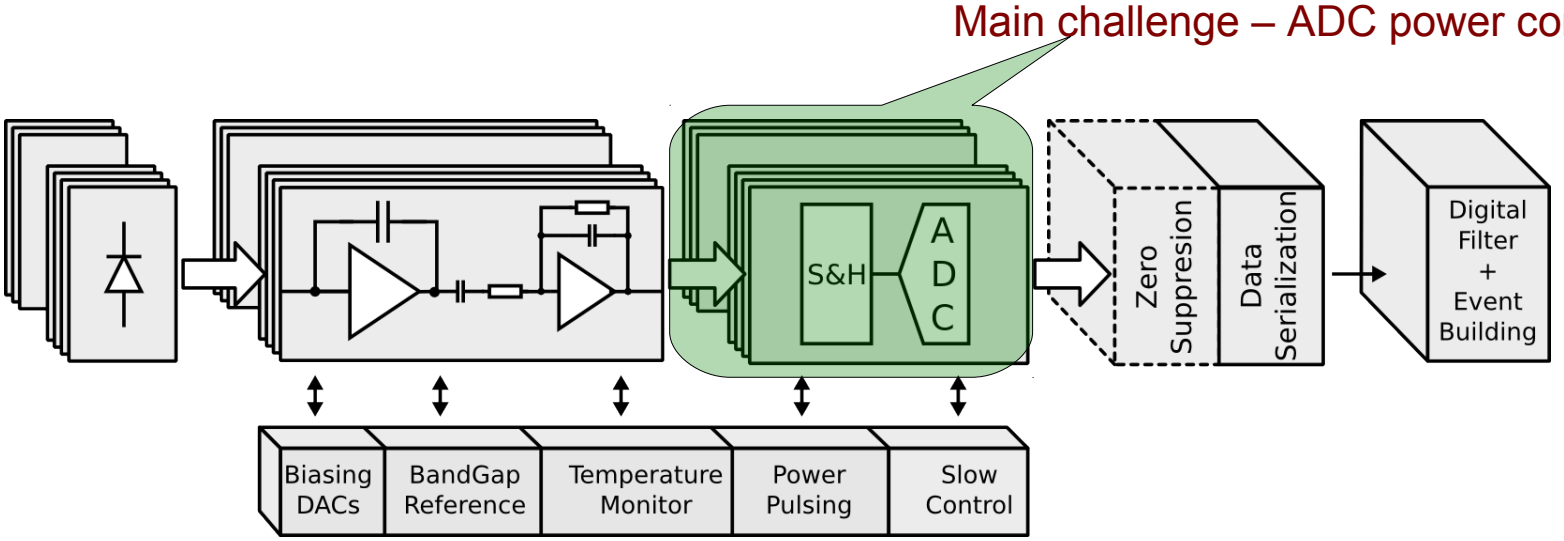
Works on multi-plane FCAL detectors
Multiboard readout integration



Goals:
- test with cosmic rays
- testbeam at CERN at the end of 2014

Status
- presented on FCAL meeting 2 weeks ago...
- 4 boards have the same low noise (working alone)
- in multi-board configuration still some disturbances are present (work in progress...)

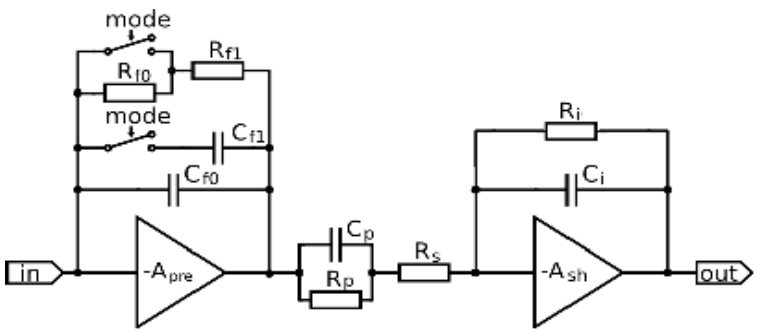
Works on multichannel readout ASICs in CMOS 130 nm



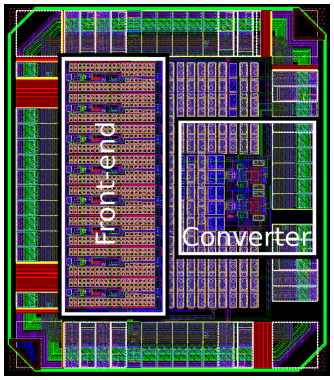
We have been working on multichannel readout architecture comprising a dedicated front-end and a fast low-power ADC in each channel, a low power PLL for high speed clock generation, and various other blocks...

Works on front-end
LumiCal front-end in CMOS 130 nm

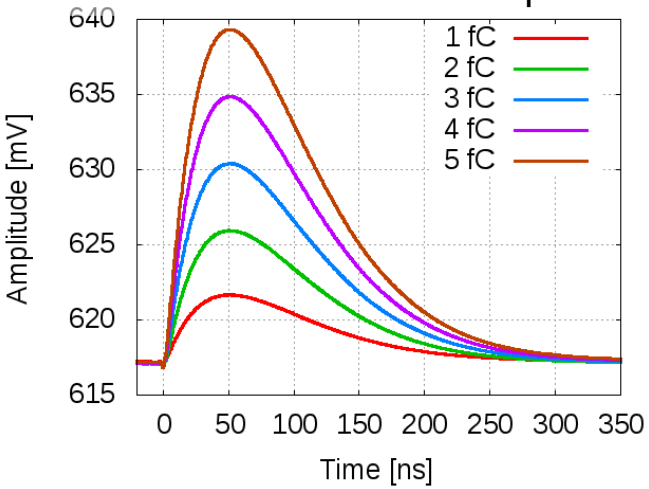
Channel schematic diagram



Layout



Measured front-end response



Design specs:

- 8 channels
- Cdet ≈ 5 ÷ 50pF
- 1st order shaper (Tpeak ≈ 50 ns)
- Variable gain:
  - calibration mode - MIP sensitivity
  - physics mode - input charge up to ~5 pC
- Power pulsing implemented
- Power consumption ~1.5 mW/channel

Very Preliminary Measurements:

- Fully functional
- Tpeak ≈ 51 ns
- Calibration mode @10pF:
  - gain 4.1 mV/fC
  - linear range ~60 fC
  - ENC 930 e-
- Physics mode @10pF
  - gain 105 mV/pC
  - Linear range ~2.7 pC (saturates >5pC)

Works on ADC
Prototypes of SAR ADC vs State-of-the-Art

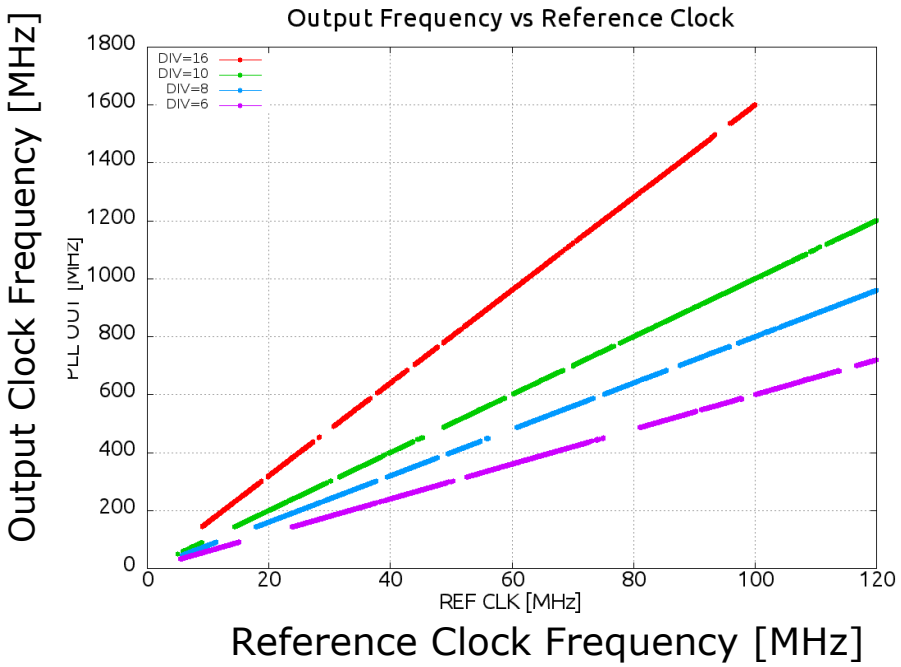
Main features	LHCb	LumiCal
Resolution	6	10
Sampling frequency [Ms/s]	>80	>40
Power cons. [mW] @40Ms/s	0.35	1
Size [mm^2]	0.016 40 x 400	0.087 146x600
DNL/INL [LSB]	<0.4	~1.0
SINAD@40MS/s[dB]	37.5	>56
ENOB[bits]	5.8	9.3
FOM [fJ/conv]	~150	~50

Performance of **our ADCs**
is similar to
State-of-the-Art designs

Works on PLL
PLL architecture, design and results

Main features:

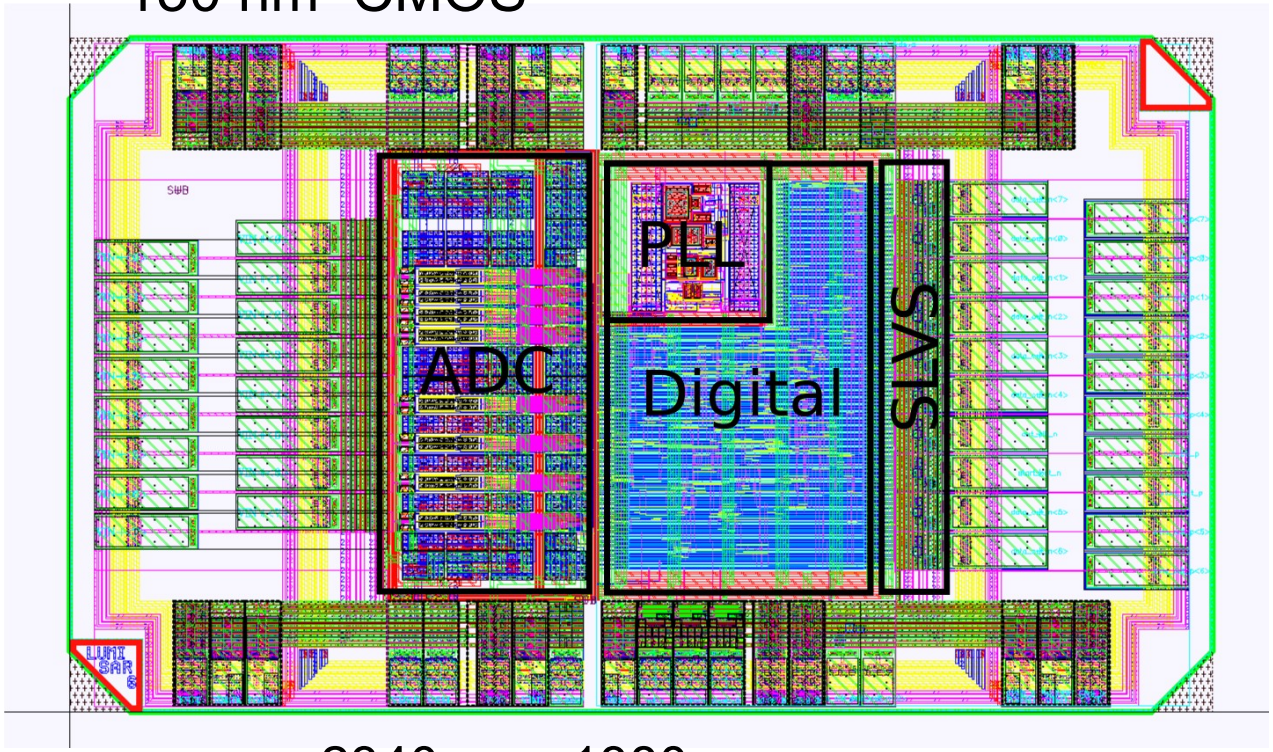
- General purpose PLL block
- Very wide output frequency range: **20MHz – 1.6GHz** (SLVS limit.)
- Power consumption **~0.6mW @ 1GHz**
- Different loop division factors: **6**, **8**, 10, 16
- Size 300um x 300um



M. Firlej, T. Fiutowski, M. Idzik, J. Moroń, K. Świentek, "Development of variable frequency, power Phase-Locked Loop (PLL) in 130nm CMOS technology , TWEPP2013 23-27 September 2013, Perugia Italy

Multichannel ADC ASIC
Layout diagram

130 nm CMOS

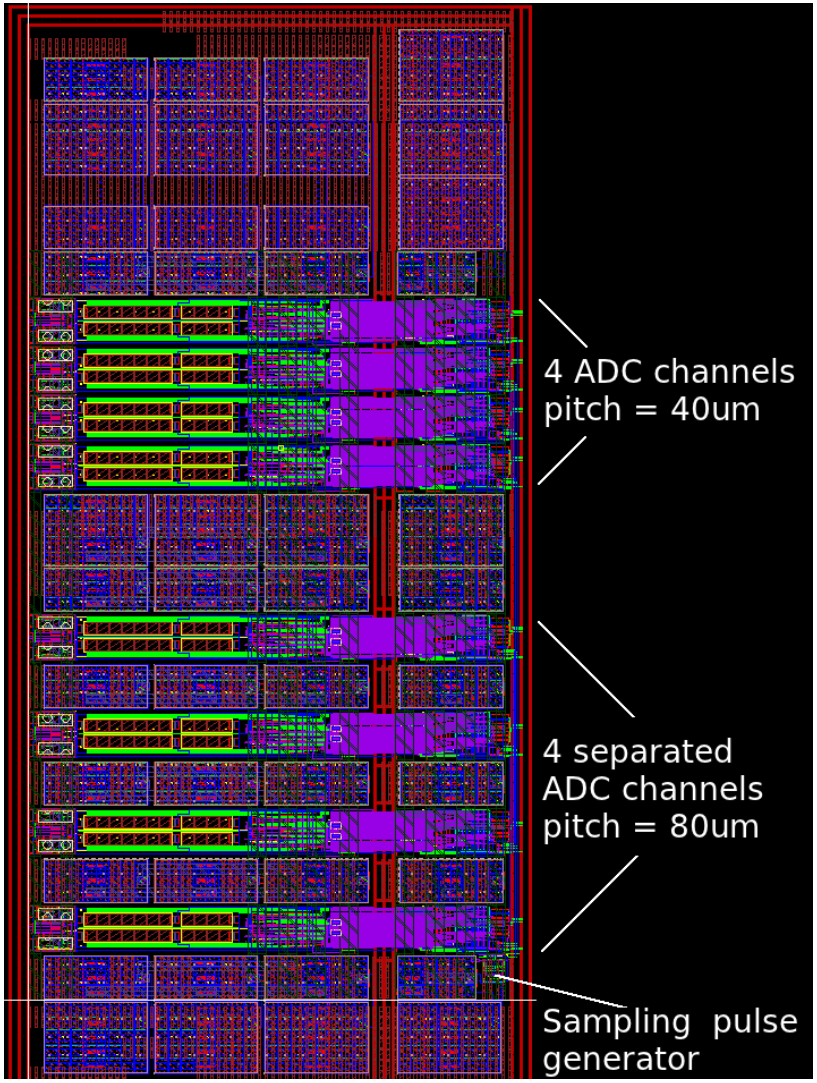


2340um x 1380um

ADC prototype contains:

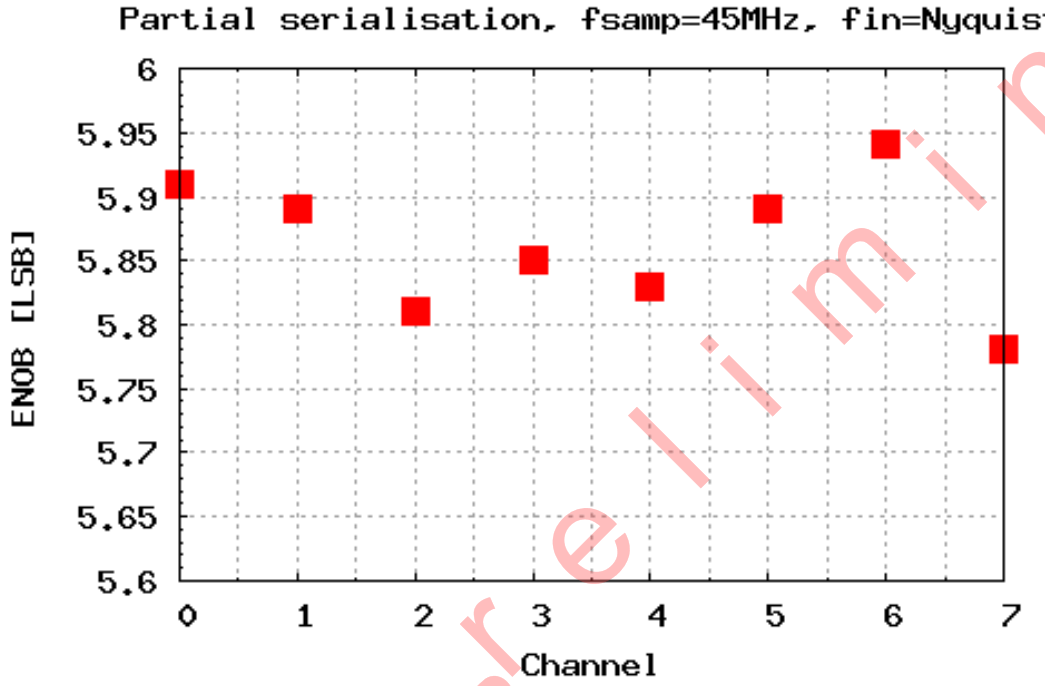
- 8 channels of 6-bit SAR ADC
- Readout circuitry (multiplexer & serialiser)
- PLL for generation of high frequency readout clock
- SLVS I/O circuitry
- Staggered pads
- Command decoder

Layout of 8 channels of SAR ADC



- ADC channels designed in 2 different pitch values:
  - 40 um (4 channels)
  - 80 um (4 channels)
- Decoupling capacitances in the gaps between channels

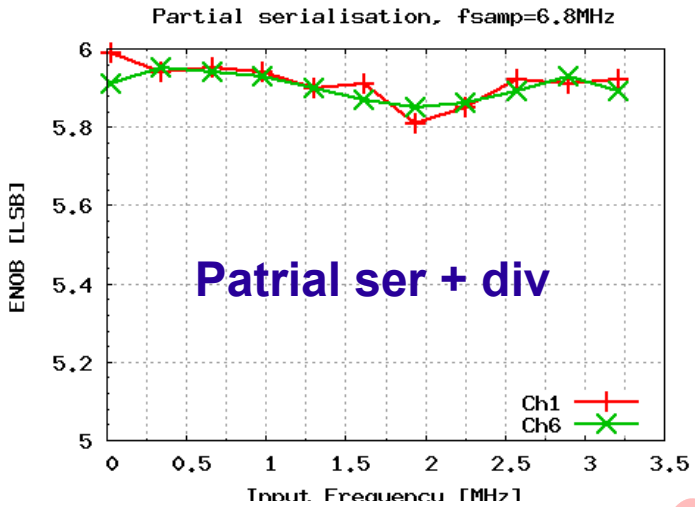
Measurement results
ENOB uniformity between channels

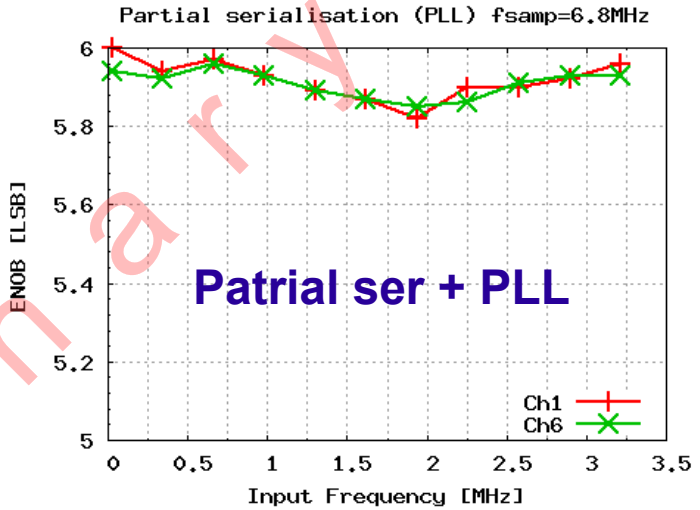


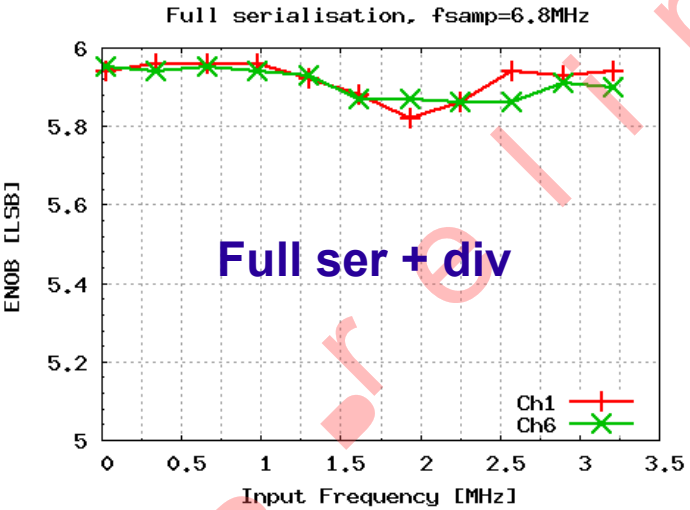
- Measured for all channels in partial serialisation mode
- fsamp = 45MHz
- fin, Nyquist (~22MHz)

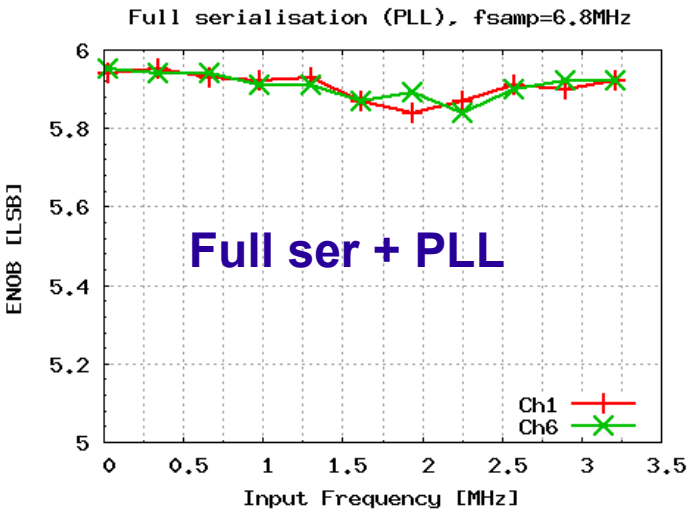
Very good ENOB uniformity over channels

Measurement results
Different readout modes, fs=6.8 MHz



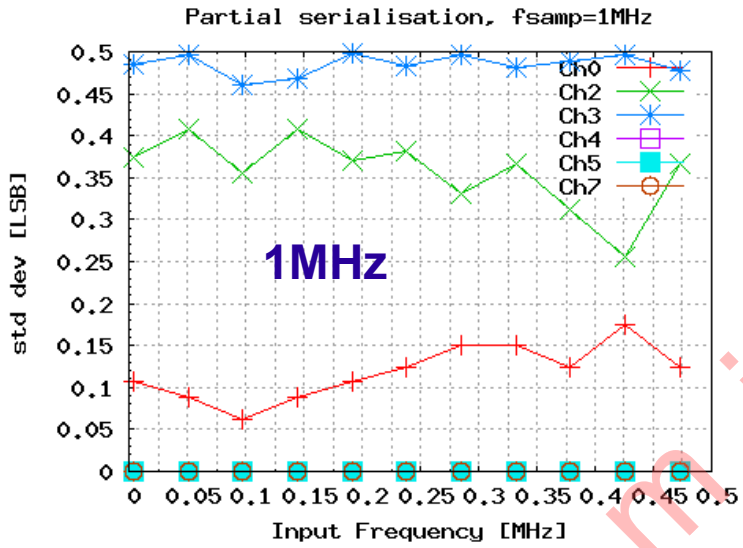


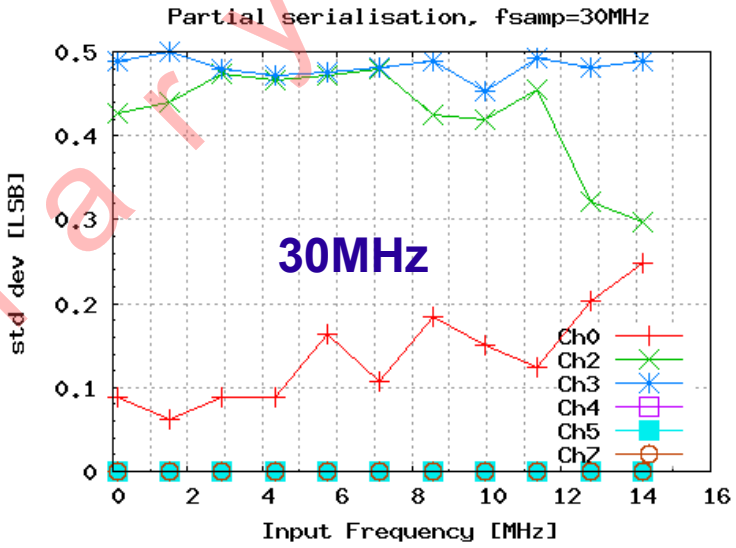




Very good and consistent results obtained in all modes!

Crosstalk effects, fsmp < 40 MHz



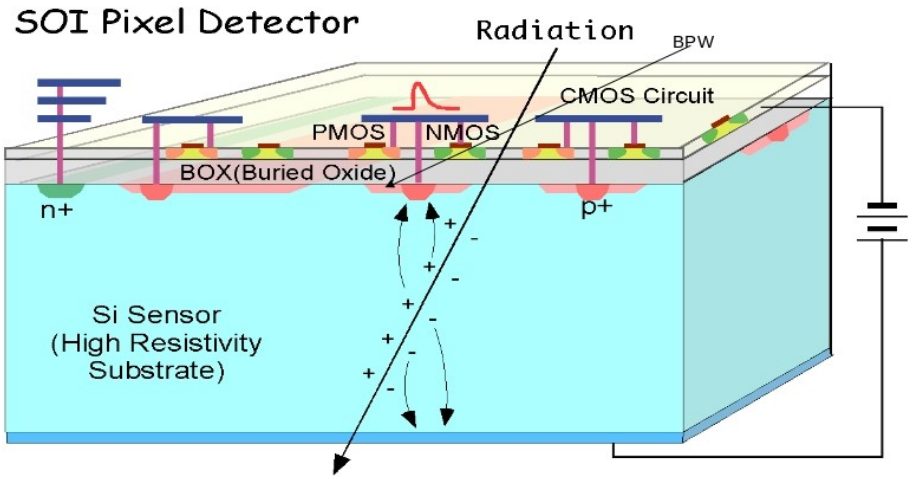


- Signal in channels 1(40um pitch) & 6(80um pitch)
- Standard deviation calculated in channels without signal
- Different behaviour of ch 0-3 (40um pitch) and 4-7 (80um)
  - 4-7 are completely quiet, no “crosstalk” effect observed
  - 0-3 have small “crosstalk” slightly dependent on frequency

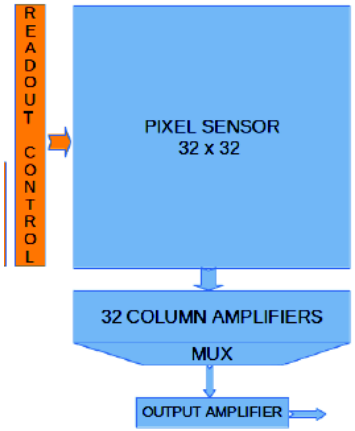
Latest IBM and TSMC news

- We have just received new IBM 130 nm prototypes
  - 8 channel LHCb style front-end (Tpeak ~ 25ns, very short tail)
  - Updated 6-bit and 10-bit ADCs, PLL
  - 8 channel digitizer with 6(10)-bit ADCs, PLL, SLVS etc...
  - There is a lot of testing to be done !!!
- We have just submitted first structures in TSMC 130 nm
  - SLVS I/O interface
  - PLL
  - Should be fabricated in ~2 months
- Technology choice will be done on the basis of radiation measurements of TSMC 130 nm, in ~3 months...

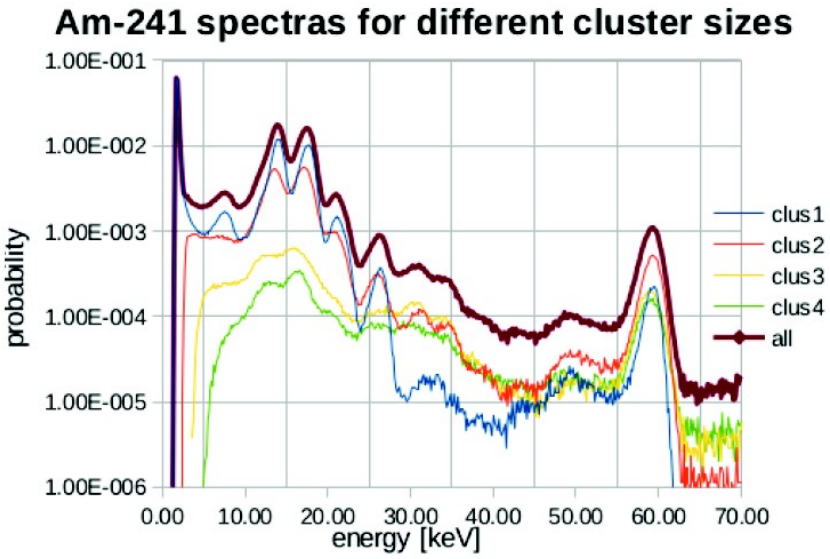
Works on SOI pixels detectors
R&D is done together with IFJPAN (P. Kapusta)



First prototype with
32x32 pixels fabricated
In Lapis 200nm SOI
process. tested



We have designed the 2nd prototype
Using Double SOI process
We are waiting for the chips...



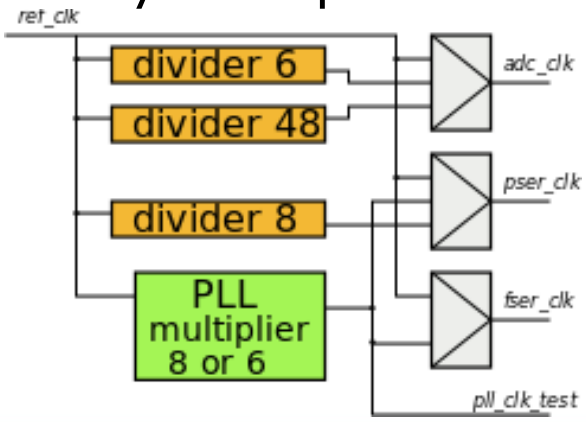
Summary

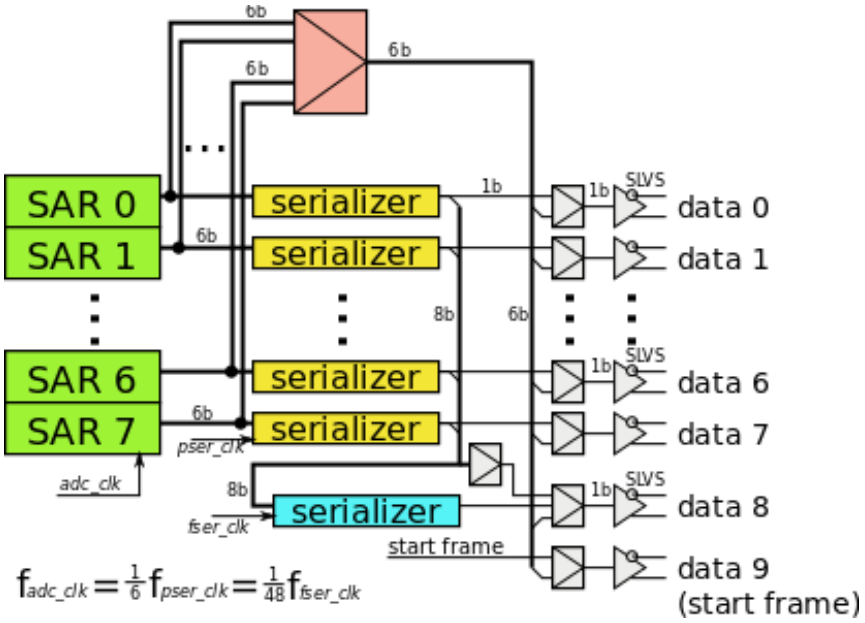
- We are doing our best to get working the multi-plane detector with the old AMS0.35um based readout board...
- Works on front-end and more complex readout ASICs are ongoing at AGH-UST
  - We have quite nice results with front-end, ADC, PLL blocks designed in IBM CMOS 130 nm
  - We are starting to integrate the blocks into complex readout chips
  - Because of not clear future of CMOS 130 nm, recently we have started first designs in TSMC 130 nm
  - **There is also small SOI pixel R&D ongoing**

Thank you for attention

8 channel ADC ASIC
Readout modes - block diagram

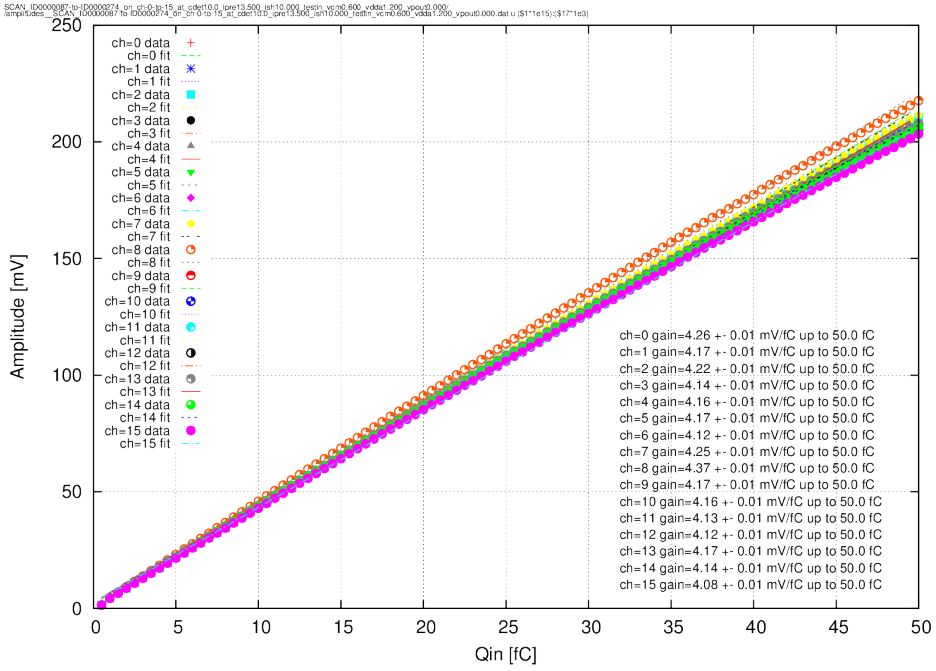
- Three modes
  - test
  - partial serialisation
  - full serialisation
- Two clock generation schemes (serialisation)
  - by division
  - by multiplication





Works on front-end in progress…
LumiCal front-end in CMOS 130 nm

Gain



Noise