CTF3 BPM ACQUISITION SYSTEM

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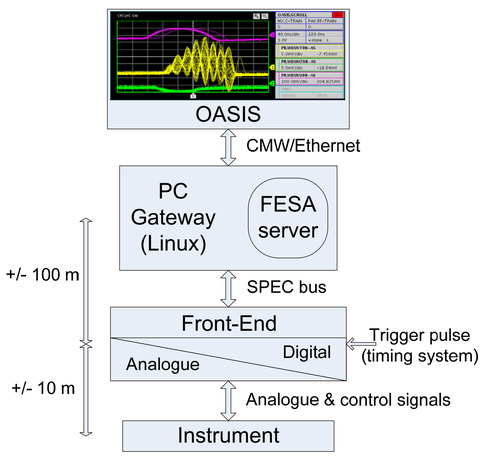
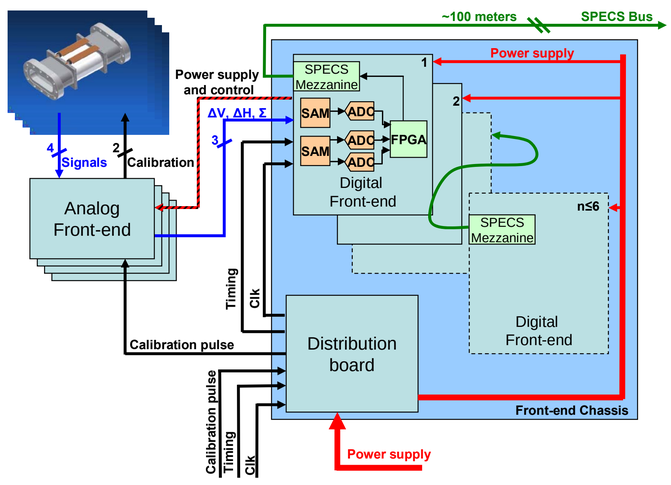
Abstract

The CLIC Test Facility 3 (CTF3) is an R&D machine being built in order to validate concepts that will be used in the Compact LInear Collider (CLIC). CTF3 being an instrumentation intensive machine, considerable amount of money is put into the acquisition hardware and high quality cables used to bring the instrument signals to the digitalisation crates with as little degradation as possible. The main idea in this new approach is to reduce the distance between the signal source and the Analogue to Digital Converter (ADC) and therefore reduce the cost of the cabling. To achieve that, we have developed a radiation hard front-end that we install directly into the accelerator tunnel. This front-end deals with the digitalisation of the signals after an analogue buffering. Afterwards, the data is sent to a computer through the Serial Protocol for Experimental Control System (SPECS) field bus. Finally the digitalised signals are made available to the operation crew thanks to a device server implementing in FESA the OASIS interfaces. After a presentation of this low cost solution to Beam Position Monitor (BPM) acquisition, the paper gives the results of the first integration tests performed in the CTF3 machine.



ARCHITECTURE

The system is made of four parts as depicted on the left. At the bottom, we have the instrument that produces the signals we want to digitalise, e.g. a BPM. The analogue signals are connected to the front-end that is installed very close to the instrument (typically 10 meters) in the radioactive zone. On trigger reception, the front-end buffers the data in analogue form using an analogue memory and converts it with a slower but radiation hard ADC. Once digitalised, the data is read from the front-end memory by a gateway using the Serial Protocol for Experimental Control System (SPECS) field bus. Since the gateway is not radiation hard, we install it in a technical building outside the machine tunnel. The front-end is connected to the gateway using plain category 6 Ethernet cables running on distance of typically 100 meters. The acquired waveforms are exported into the control system by a device server written with the CERN Front-End Software Architecture (FESA) framework. The server implements the properties specified by Open Analogue Signal Information System (OASIS)[1].



The Front-End consists of two parts: the analogue front-end connected to the beam position monitor for signal amplification and calibration and the digital front-end (DFE) to digitalise and send the data to the gateway. Up to six DFEs are grouped together under the beam pipe inside a chassis with a distribution board. The DFE receives the differential signals conditioned by the analogue front-end. On trigger, the analogue memories sample the signals at 512 MS/s with a dynamic range of 12 bits. Once the memories are filled up, they are read out at 800 kHz by a bipolar 14-bit ADC. This acquisition cycle must be executed between two beam pulses. The digitalised data is stored in the internal RAM of the FPGA. A SPECS mezzanine is plugged on each DFE for the transmission between the front-end and the gateway.

With the four electrodes' signals from the BPM, the analogue board produces three signals: a sum (Σ) and two differences (ΔH & ΔV). Depending on the BPM's type, these differences can be either the horizontal and vertical deviations or the two diagonal deviations. A final calculation is done by software in the gateway to have normalized horizontal and vertical deviation signals.
The reason why we have chosen the solution of the fast analogue memory and a slower ADC is to resist the radiations and be able to install the system close to the beam (cable cost minimisation). All the components have been chosen to resist at least 35 kRad. The analogue memory is a SAM (Swift Analogue Memory) developed by Commissariat à l'Energie Atomique (CEA). The ADC, a LTC1419 from Linear Technology, matches the memories characteristics, 14-bit resolution and differential inputs, and is fast enough to read the SAM content between two beam pulses.
For the data transmission, the mezzanine is connected to the FPGA through a parallel bus. As on the DFE, the FPGA on the SPECS mezzanine is an ACTEL ProASICPlus. It is a flash FPGA which has also been tested and resists up to 35 kRad.
An additional feature of the digital front-end is the analogue board control. Gain, attenuation and calibration are configured through the digital board with the SPECS bus. A control signal to select which BPM to calibrate is sent by each DFE to the distribution board. A small logic bloc on the latter is implemented to send the calibration pulse to the right BPM. The distribution board is also used to receive and amplify signals such as the main sampling clock from the RF system and the beam synchronised trigger. At last, it serves as a power supply distribution for the digital front-end boards.

CONCLUSIONS

The first tests have validated the first DFE prototype as well as the whole system. The second DFE prototype is being tested before launching the final series.

An installation for 50 BPMs with the original solution (ADCs in VME crates and long HQ cables to bring the analogue signals) would cost about 240 k€. With the DFE solution, the total cost is around 80 k€ including the PC gateways, SPECS boards, the DFEs and the cables (power supply, calibration and, SPECS buses). That means the new solution is three times cheaper! In fact, in addition to the significant cost reduction, we have also improved the acquisition chain. With the digitalisation closer to the source, we have a better signal/noise ratio and the analogue memory/14-bit ADC combination has a higher effective number of bits.

The DFEs will also be used to acquire instruments other than the BPMs, which the system was initially designed for. Furthermore, with a constant cabling cost reduction in mind, we are also investigating the possibility to include the calibration system and the power supply inside the front-end chassis. The final goal is to have an autonomous chassis directly connected to the mains.

REFERENCES

[1] S. Deghaye *et al.*, "OASIS: a new system to acquire and display the analog signals for LHC", ICALEPCS'03, Gyeongiu, Korea, October 2003.
[2] D. Charlet *et al.*, "SPECS: A Serial Protocol for the Experiment Control System of LHCb", Orsay, France, October 2005.
[3] S. Deghaye *et al.*, "Hardware Abstraction Layer in OASIS", Geneva, Switzerland, October 2005.
[4] A. Guerrero *et al.*, "CERN Front-end Software Architecture for accelerator controls", ICALEPCS'03, Korea, October 2003.