FPGA Use within the Detector Volume

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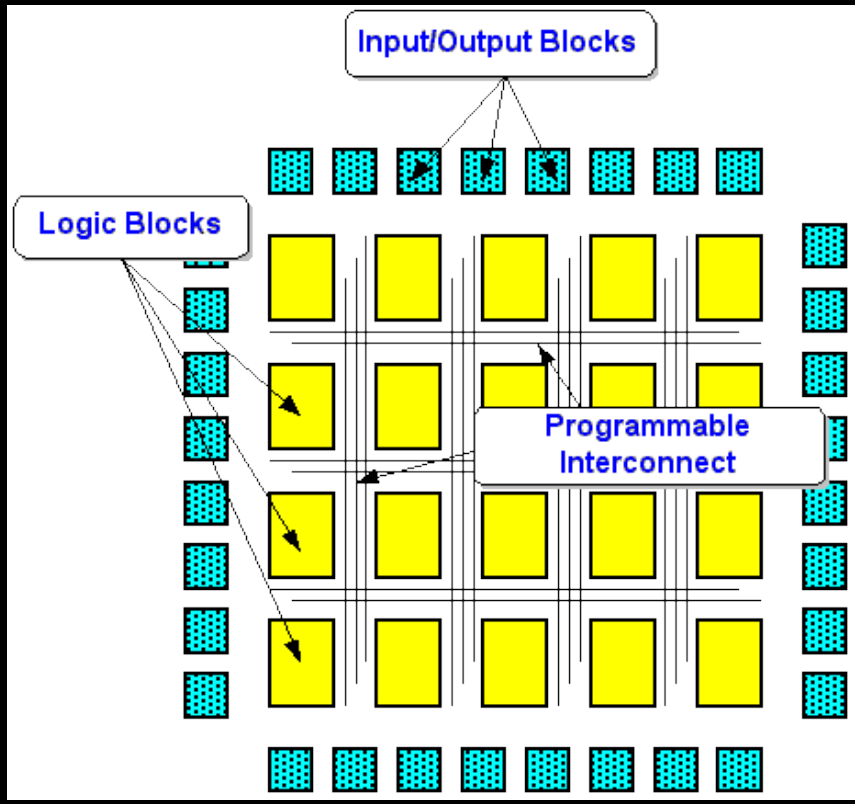
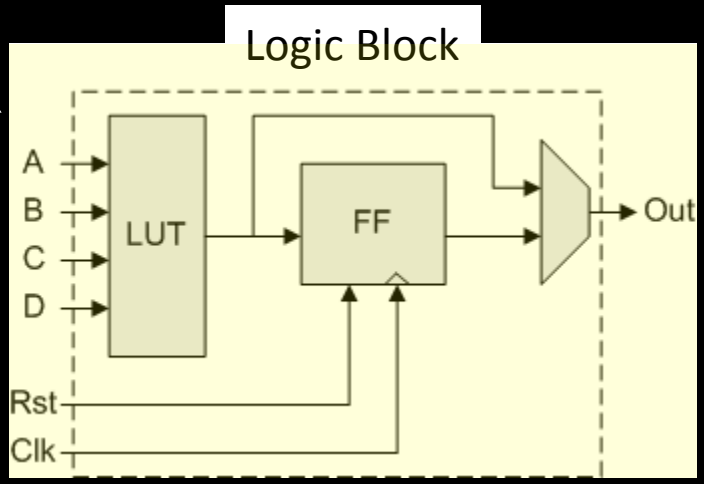
Disclaimer: difficult to cover all cases, this talk is a partial view.

What are FPGAs ?

- A Field Programmable Gate Array (FPGA) is a integrated circuit which contains lots of logic blocks.
- Logic blocks can be connected together in a programmable way.
- inputs and outputs are also programmable, in direction, strength and standard (CMOS, LVPECL, LVDS, etc).



Each logic block can be programmed to perform a boolean operation (in the LUT) and store a single bit in a Flip-Flop.



The data needed to set all programmable options of an FPGA is often called "**Configuration data**".

The circuit realized with the Logic blocks and interconnects in an FPGA is called "**User Logic**".

Why do we care about that ?

In HEP detectors and accelerators, commercial-grade FPGAs have become extremely useful to build digital hardware tailored to specific requirements, including non-standard data processing and interfaces.

Being commercial circuits, they are not (necessarily) tolerant to ionizing radiations

→ this point is the focus of the talk.

Many subsystems use or will use FPGAs in radiation areas (but not in extreme radiation areas like central trackers)

Non-exahustive list (more details on back-up slides):

ATLAS:	TileCal, muons
CMS:	HCAL, muons, GEM, CP-PPS
LHCb:	RICH, calorimeters, muons
ALICE:	TDC

Example: CMS HCAL

- in the original FEE there were 2 types of FPGAs and 5 types of ASICs.
- in the Phase-1 upgrade FEE there will be ~5 types of FPGAs and 4 types of ASICs

FPGAs in HEP: trends

- initially FPGAs were simple boolean logic; later other blocks have been integrated: CPU, PLL, high-speed communication, etc.

- in the HEP Front-End Electronics installed around 2005, FPGAs were mostly used for control and readout logic with external high speed links.

- in recent FEE systems, FPGAs (will/could) take advantage of newer functions: high-speed links for increased data readout, PLLs for clock management related to synchronization with the accelerator clock, etc.

- Powering newer FPGAs becomes more complicated: need to provide higher currents at lower voltages.

FPGA types by technology

Technology of the memory element	Main Vendors
SRAM (Static RAM)	Altera, Atmel, Lattice, Xilinx
Anti-fuse: one-time-programmable	MicroSemi, Aeroflex, Quicklogic
Flash memory cells	MicroSemi

Radiation effects on CMOS digital circuits (not limited to FPGAs)

1. **TID = Total Ionization Dose**. Measured in Grey = Gy (or in rad: 1 Gy = 100 rad)

2. **SEE = Single-Event Effects :**

- SEL = Single-Event Latchup
- SEU = Single-Event Upset
- SET = Single-Event Transient
- SEFI = Single-Event Functional Interrupt
- SEGR = Single-Event Gate Rupture
- SEB = Single-Event Burnout

Main radiation effects on commercial FPGAs

Memory cells	TID (degradation, then failure)	SEU on configuration	SET on configuration	SEL
SRAM	**Virtex-6:** ~3.8 kGy [1]. **Arria GX**: degrades from 1.7 kGy, still alive at 70 kGy [13]	Yes	Yes	No, on recent Xilinx families [12, 13].
Anti-fuse	**Aeroflex Eclipse**: 3 kGy [18]	No	Yes	No [12]
Flash	**ProASIC3**: fails at ~300 Gy. **Igloo2:** one sample failed at ~1 kGy. **SmartFusion2**: one sample survived 380 Gy; reprogramming fails at ~20 Gy [10]	No	Yes	No on ProASIC3x [8]. Suspect non-destructive SELs on SmartFusion2 [10]

Mitigating the radiation effects is possible but can be complicate…

Example: the configuration of SRAM-based FPGAs can be upset by a particle.

Initial solution: we can reprogram the FPGA periodically:
Problem: sometimes the configuration will be upset much before reprogramming it, other times it will be reprogrammed when there is no need → not very efficient

Better solution: certain FPGAs allow to monitor the status of their own configuration, then an external controller can detect when the configuration is upset and trigger the reprogramming → ACTIVE RECONFIGURATION
Problem: we need a controller that will not be upset by radiation.
Problem #2: during the reprogramming phase, the FPGA will loose all data and capability (dead-time, data loss).

Even better: certain FPGAs allow to monitor and reprogram only a part of the FPGA itself, this reduced the data-loss → ACTIVE PARTIAL RECONFIGURATION
This is done in ALICE TPC.

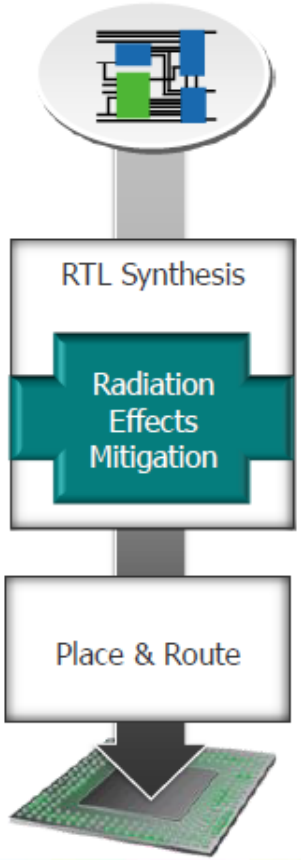
More research is ongoing to reduce even more the data-loss.

SEU mitigation in the User Logic

- The FPGA designer can do it “by hand” or with his/her semi-automatic tools
- There are also commercial synthesisers doing it (see next slides)

Synthesis-Based Radiation Effect Mitigation

- FSM: Automatic encoding for mitigation
  - SEU Detection & Recovery, SEU Fault Tolerant
- TMR: "Smart" Automatic Redundancy Insertion
  - Multi-mode, multi-vendor: more control, more options
  - Mitigates SEUs and SETs
- Flow with Place-and-Route (P&R)
  - P&R options switched off to retain redundancy
  - Script that helps floor-planning for multi-event reduction
- Equivalence Checking Support
  - Confidence that no functional error is introduced



Why use Safe FSM?

- Synthesis does **not** implement "*when others / default*" clause
- Fully defined FSM cannot detect illegal transition
- Less area intensive than TMR
- Only control logic needs to be protected
  - — Data stream already protected with data recovery

"SEU Detect" FSM Encoding

Automatically Detects and Recovers from SEU on State Register

Problem

- SEU on FSM state register

Solution

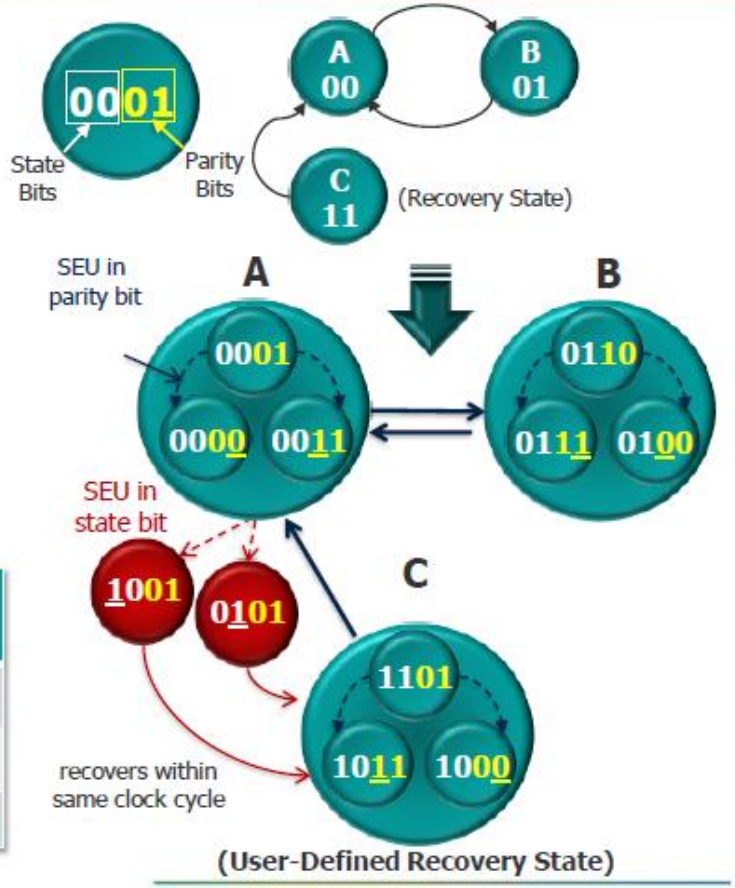
- FSM encoded for recovery/error-handling state
- Adds 2 parity bits for error detection
- Detects all invalid transitions[1]
- Does not mitigate SET or configuration upset
  - Works better for hardened configuration at lower frequencies

Benefit

- Automated, no tool or mitigation expertise required
- Works for efficient encoding styles (binary, gray)[2]
- Prevents "false alarm": SEU on parity bits ignored

STATE	BEFORE	With parity bits	SEUs detected	SEUs having no impact on operation
A	00	0001	1001, 0101	0011, 0000
B	01	0110	1110, 0010	0100, 0111
C	11	1101	1001, 0101	1000, 1011

1 – To valid or invalid states
2 – Previous Safe FSM implementations do not detect SEUs for binary or gray encoding



"SEU Correct" FSM Encoding

Automatically Corrects SEU on State Flip-Flops

Problem

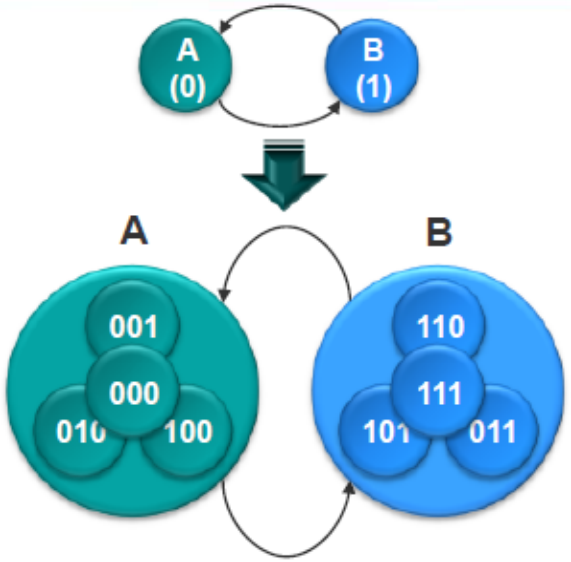
- SEU on FSM state register

Solution

- FSM encoding automatically corrects state register
- Hamming -3 encoding
  - Adds *k* parity bits[1] to state vector
- Does not mitigate SET or configuration upset
  - Works better for hardened configuration at lower frequencies

Benefit

- Automated, no tool/mitigation expertise required
- SEU does not interrupt normal FSM operation
  - Applicable for all encoding schemes



STATE	BEFORE	With Parity Bits	These States Map to Same Destination State
A	0	000	001 010 100
B	1	111	110 101 011

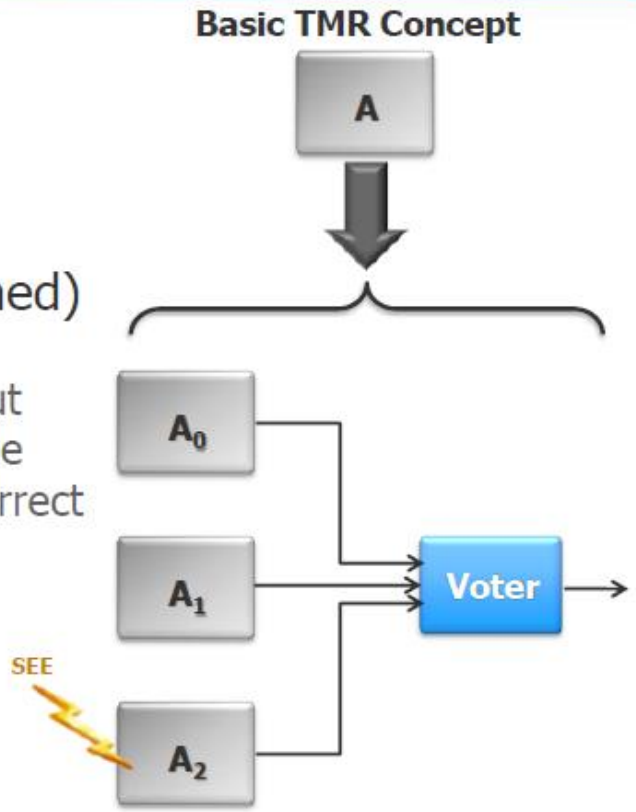
Area Impact

# of state bits	Parity bits added
1	2
2-4	3
5-11	4

1 – *k* must satisfy equation $2^k \geq k+n+1$ (*n* = # of state bits)

Mitigation Using Redundancy

- Redundancy can be used at
  - Multiple board level
  - Multiple FPGA level
  - Single FPGA level (Silicon or HDL)
- Triple Modular Redundancy (defined)
  - Unit Triplication
  - Adding a majority voter at the output
  - If a single event effect (SEE) hits one unit, the voter output will remain correct



Localized TMR

What

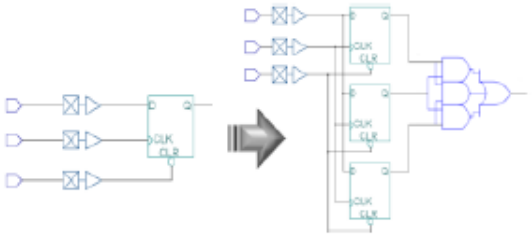
— Sequential elements are tripled, followed by a voter

– e.g., flip-flops, memories, RAM blocks, FIFOs, SRLs

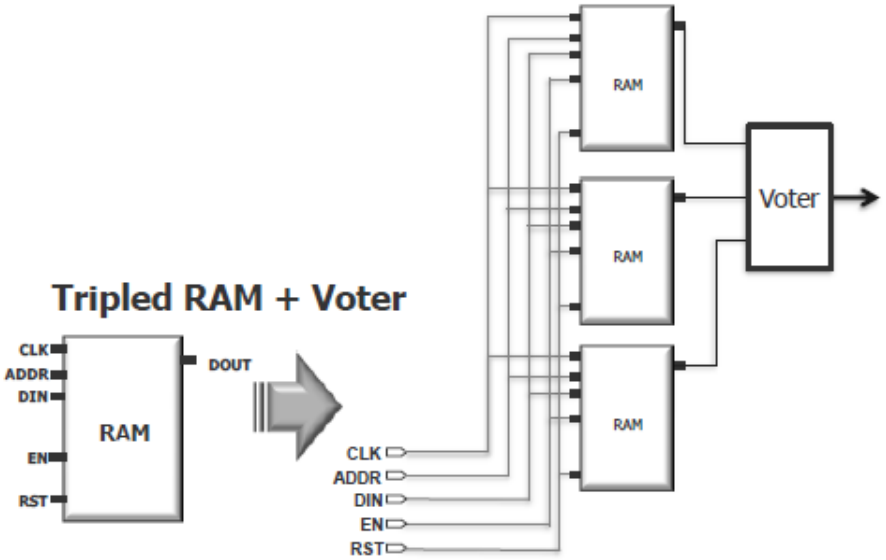
Benefit

— SEU mitigation

Tripled Registers + Voter



Tripled RAM + Voter



Distributed TMR

What

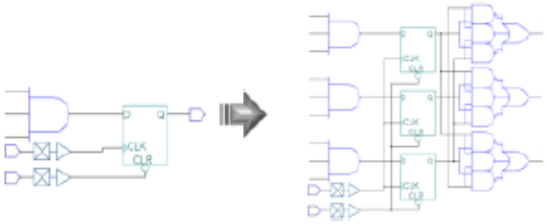
— Sequential, combinatorial logic, and voters are tripled

— I/O triplication (optional)

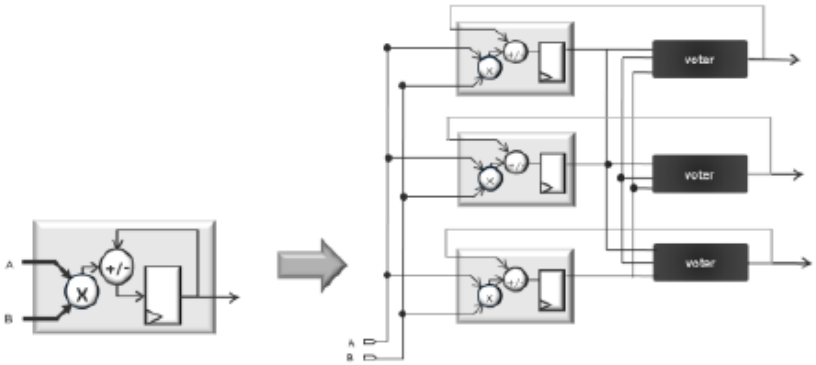
Benefit

— SEU, SET & configuration upset mitigation for logic and data routes

Tripled combinational logic, registers, voters



Tripled DSP blocks & voters



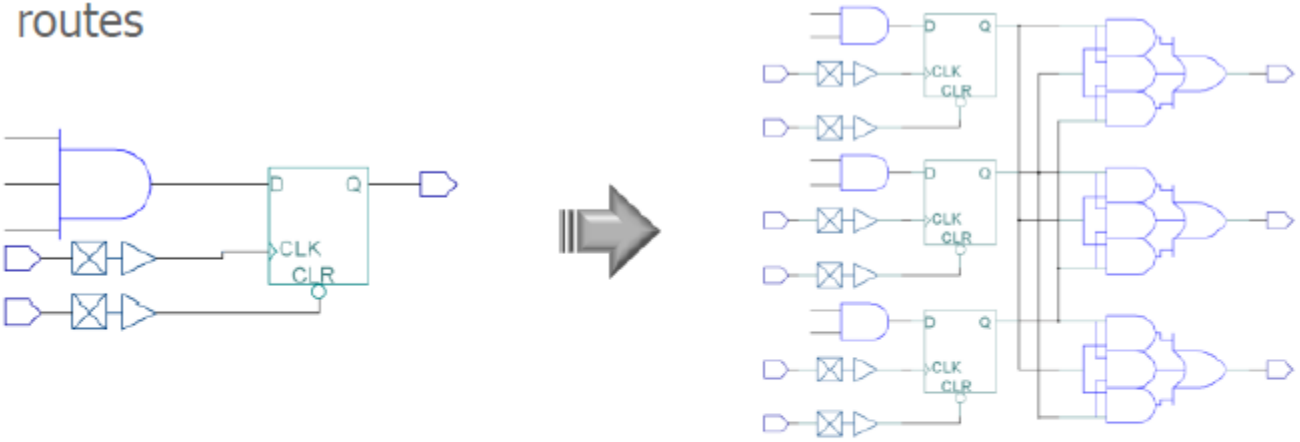
Global TMR

What

- Sequential elements, combinatorial paths, voters, global buffers are tripled
- I/O triplication (optional)

Benefit

- SEU, SET & configuration upset mitigation for logic, data & global routes



Situation at CERN

- so far collaboration across different projects is rare and based on the initiative of individual developpers
- some synergies (igloo2 in CMS HCAL and in the machine group BE-BI)
- might be useful to coordinate radiation tests or at least advertise. An initial attempt is : https://twiki.cern.ch/twiki/bin/viewauth/FPGARadTol/)
- we had a “Workshop on FPGAs for High-Energy Physics” held at CERN on March 2014.

Conclusions

We could benefit from:

- common test programs
- common procurement strategies
- common design strategies


The End

Back-up slides

FEE systems of CMS

Sub-system	Approx radiation	FPGAs in 2008-2012	FPGAs after 2012 (radiation ~6x higher)
Tracker [2]	200 kGy. 10^{14} n/cm^2	No FPGAs (ASICs only)	No FPGAs (ASICs only)
ECAL [3,4]	25 kGy.	No FPGAs (ASICs only)	No FPGAs (ASICs only)
HCAL [5]	3 Gy. 10^{11} n/cm^2	Actel anti-fuse FPGA, for control only	igloo2 (flash) for control, data processing, TDC and transmission from 2016
Muon detectors	0.4 Gy. $5x10^{10}$n/cm^2	SRAM FPGAs [6, 7].	igloo2 (flash) for control, data processing, TDC and transmission from 2014 [15]
CT-PPS	200 Gy, $2x10^{12}$ n/cm^2 per 100/fb integrated lumin.	Did not exist	igloo2 (flash) for control, data processing, TDC and transmission from 2018 ?

FEE systems of ATLAS

Sub-system	Approx radiation	FPGAs in 2008-2023	FPGAs after 2023 (radiation ~6x higher)
Tracker	Xx kGy. 10^{14} n/cm^2	No FPGAs (ASICs only)	
Liquid Argon Calorimeter [16]			On chamber (3.4 kGy): probably no FPGAs. On sTGC (90 Gy): investigate with xilinx for processing and 10 Gbps readout links.
Tile calorimeter [17]	15 Gy. 10^{11} n/cm^2	640 Mb/s, severe errors in data transmission, loss of configurations	Demo project with xilinx for processing and 10 Gbps readout links
Muon detectors	xx Gy. 5x10^{10}n/cm^2		

FEE systems of LHCb

Sub-system [9, 10]	Approx radiation in 2008-2018	FPGAs in 2008-2018	FPGAs after 2018 (radiation ~6x higher)
Inner Tracker	60 kGy. 10^{14} n/cm^2	No FPGAs in the hot zone (ASICs only)	Under study (probably not required)
RICH	240 Gy, 10^{12} n/cm^2	Actel AX (antifuse) + Actel ProAsicPlus (flash) for controls	Xilinx Kintex7
Outer Tracker	70 Gy. 10^{12} n/cm^2	No FPGAs in the hot zone (ASICs only)	
SciFi Tracker			Under study (Microsemi Igloo2)
Calorimeters	50 Gy. 10^{12} n/cm^2	Actel AX (antifuse) for 80 MHz processing, Actel ProAsicPlus (flash) for 40MHz processing and control [9]	Under study (Microsemi Igloo2)
Muons [11]	80 Gy. 10^{12} n/cm^2	Actel ProAsicPlus, for calibration system	Under study (Flash device)

FEE systems of ALICE

Sub-system	Approx radiation	FPGAs in 2008-2012	FPGAs after 2012 (radiation higher)
TPC [20]	16 Gy. 10^{11} n/cm^2 [21]	Virtex-II Pro (SRAM) for datapath, with its configuration verified and refreshed by an Actel ProASIC+ (flash)	Microsemi SmartFusion2 (flash). Links up to 5 Gbps. Problems observed. FPGA PLL loss of lock → use TTCrx instead [10]. ProASIC3 (flash) for radmon.
DDL (Detector Data Link, common to all subsystems)		Actel ProASIC+ (flash). 200 MB/s links	
All others	~0 at the FPGA location		

SEU prevention in FPGAs

SEU on Flip-flops → TMR, fault-tolerant FSM.
There are two commercial synthesisers that can do automatic TMR of flip-flops, in order to prevent SEU:

1) Synplify: http://www.actel.com/documents/SynplifyRH_AN.pdf
It is in use in Cern by a few groups, so far so good (circuits not yet deployed).

2) Precision RT: http://www.mentor.com/products/fpga/synthesis/precision-rad-tolerant/ (ITAR limited)

SEU on memory → encoding

SET prevention in FPGAs

Prevention of SETs:
- TMR that includes combinatorial logic
- filtering with guard-gate

Precision Rad-Tolerant can do TMR of combinatorial logic. Apparently this feature is not supported for Actel FPGA (as of today).

Commercially available tools are evolving rapidily wrt SEU and SET → keep watching.

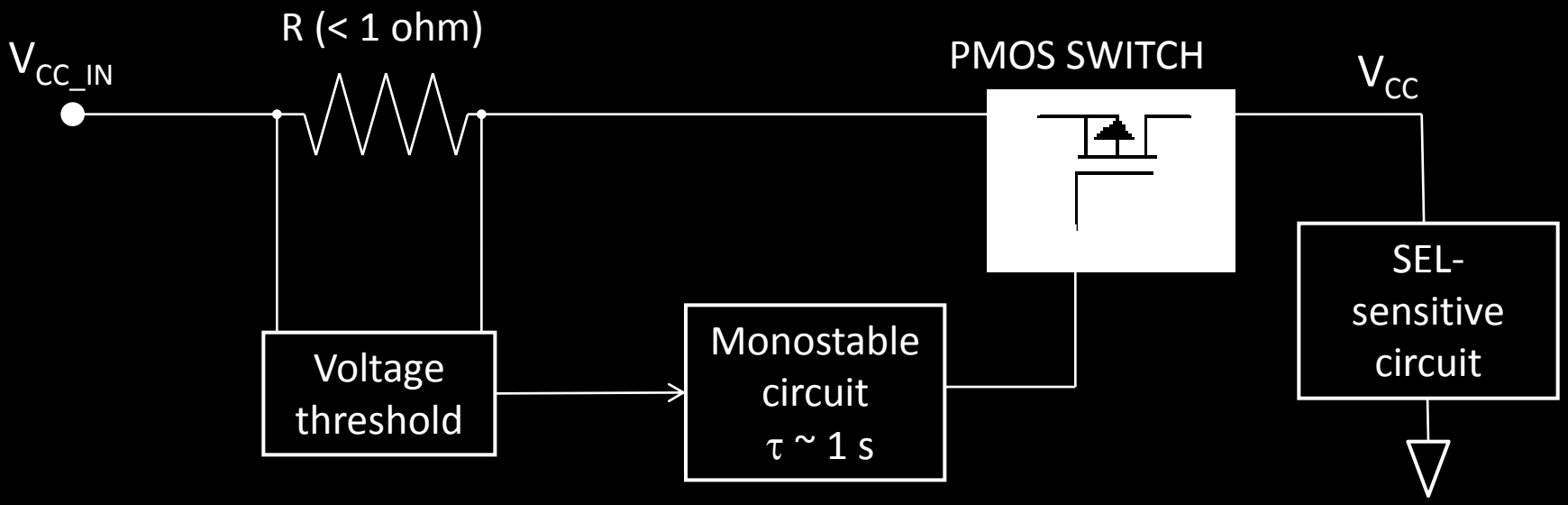
In the Microelectronics Section of CERN, some designers have been using a custom script that generates automatically TMR on registers and combinatorial logic.
The script supports only Verilog 1995 designs.
The script is available to people registered on the CERN FPGARadTol web page.

SEL prevention

A SEL is a latch-up caused by a particle crossing the circuit.
It can happen on the internal nodes (while normal latchups occur mostly on the I/Os due to ESD).
Most modern FPGAs are immune from SEL.
But other commercial components can be affected by SEL.

→ external SEL protection circuit.

SEL-protection circuits: a generic scheme



When a SEL-sensitive circuit develop a SEL, it draws more current. An external circuit can detected this situation and cycle the power.
Problem: also the protection circuit can be affected by radiation. But being a simpler circuit, it is possible to design it so that it is very unlikely that it develops a problem.

30

SEFI

SEFI = Single Event Functional Interrupt

The definition can vary according to the authors, but it normally indicates an SEE which affects the entire device, for instance:

- power-on reset
- global reset,
- global tristate
- problems in the circuit that program the rest of the FPGA

For an FPGA, it is difficult or impossible to mitigate SEFI within the FPGA design. SEFI could be mitigated at the system level.

31

FPGA types by market

- **Military and aerospace markets**: FPGAs designed explicitly for radiation hardness. HEP projects normally cannot (afford to) buy them. Not covered here.

- **Commercial markets**: all other applications. Accessible to HEP projects → covered in this talk.

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