# Calorimeter Electronics Upgrades

*F. Lanni, BNL*
*on behalf of the Electronics Preparatory Group*

**Outline**

- Motivations
- Evolution of the readout architecture toward HL-LHC and requirements
- On-going developments across experiments
- Conclusions: possible common developments

*2nd ECFA High Luminosity LHC Experiment Workshop*
*Aix-les-Bains, France*
*21-23 October 2014*

# Motivations

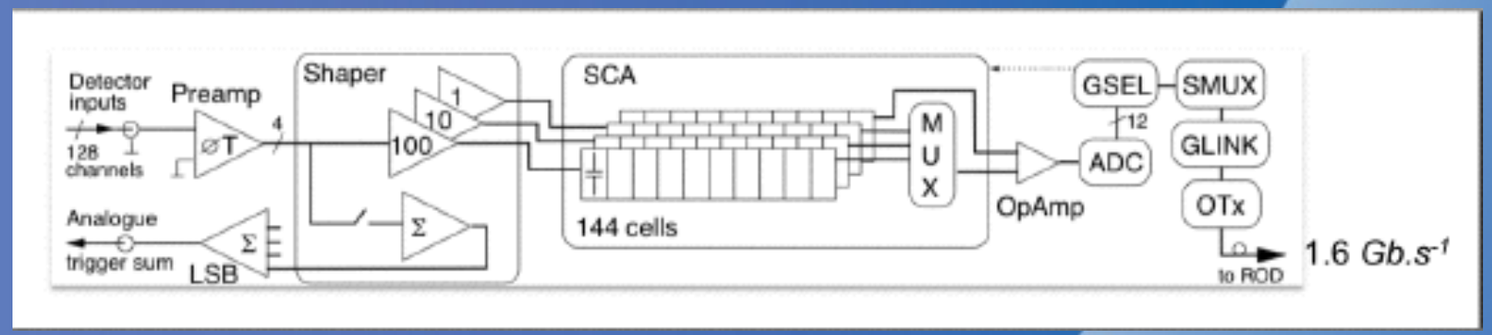
- Radiation tolerance limits:
  - *Integrated luminosity of 3000 $fb^{-1}$ at the end of HL-LHC exceeds design specifications*
- Longevity (systems and components):
  - *A total of ~30 years of operation since initial construction and installation instead of anticipated 10 years*
- Requirements from Trigger systems @ HL-LHC
  - *Readout architecture not compatible with requirements of the trigger systems @ HL-LHC*
    - *Example: CMS and ATLAS with Level-1(0) triggers >> 100kHz and >>2.5us latency*
  - *More complex trigger algorithms to be deployed at Level-1 requiring to access more and higher precision information from the detectors.*

# Calorimeter readout evolution toward HL-LHC

***Readout architecture w/o pipelines nor Level-1 trigger logic: data digitised and streamed off detector @ 40MHz.***

## ATLAS Liquid Argon Calorimeter Front-end:

*3 gain settings, analog pipelines*
*Gain selection (GSEL) and A/D conversion after Level-1.*
*Each Front-End Board (FEB): 1 readout link @ 1.6 Gbps*

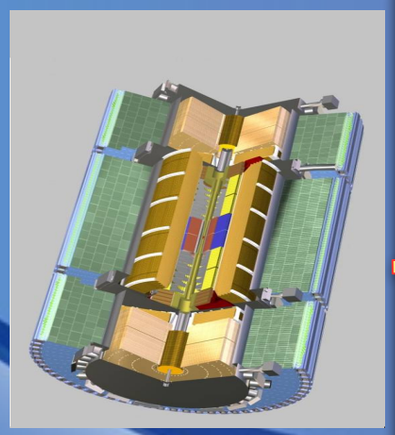


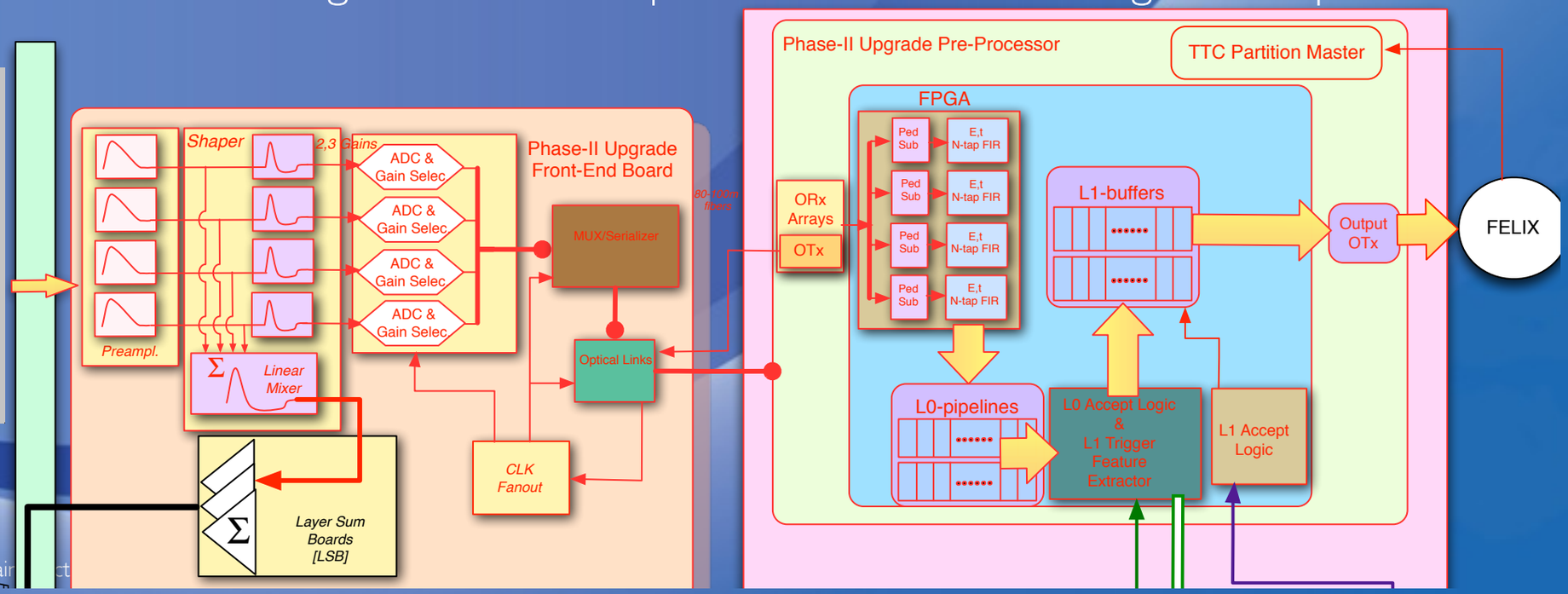

***For HL-LHC:***

A/D conversion @ 40MHz (with or without GSEL)

~10-20 @ 10Gbps links/FEB

Back-end Pre-processor boards with large FPGAs and input bandwidth in the range 1-2 Tbps





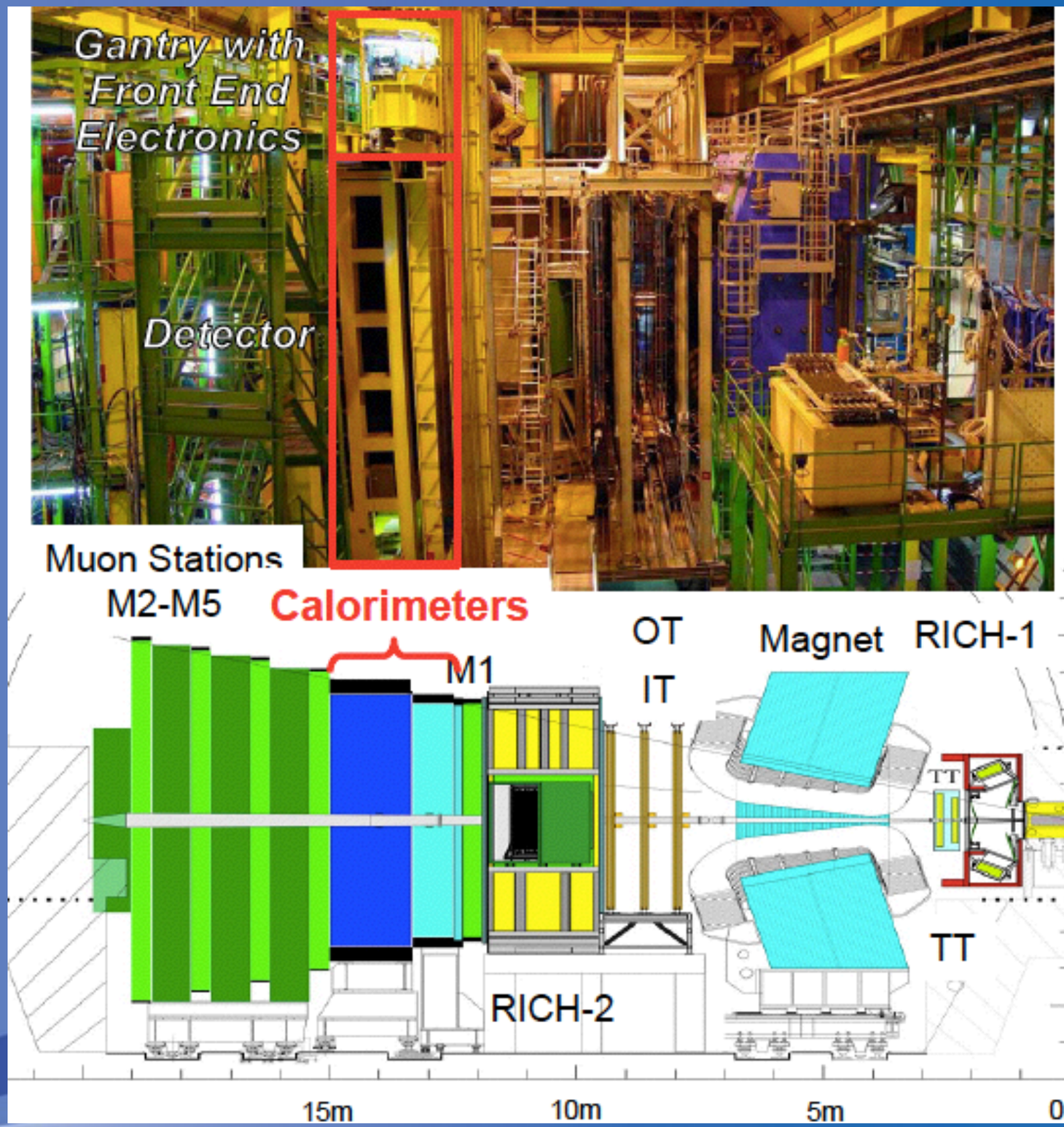
# Requirements

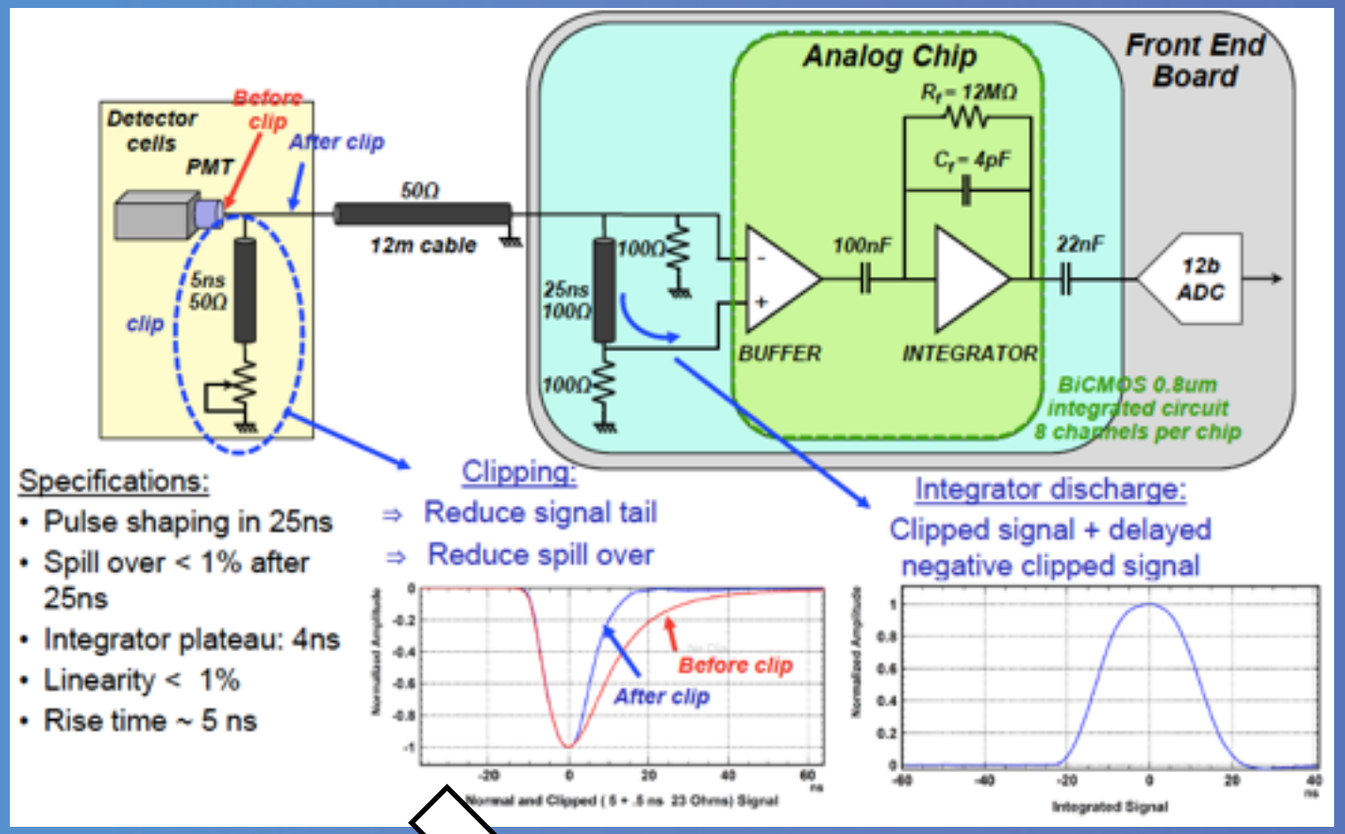
- Analog front-end design optimised for high pile-up (detector technology specific)
  - *ASICs CMOS (130nm, 65nm) and SiGe BiCMOS technologies*
- Low power, high dynamic range (16-bits), high resolution (~11-12 bits ENOB) digitisers/channel @ 40/80 MHz
- Very high bandwidth optical links (5-10Gbps)
- Back-end electronics to process massive data based on large FPGAs (~100 fast transceivers each) and high density optical I/O bandwidth

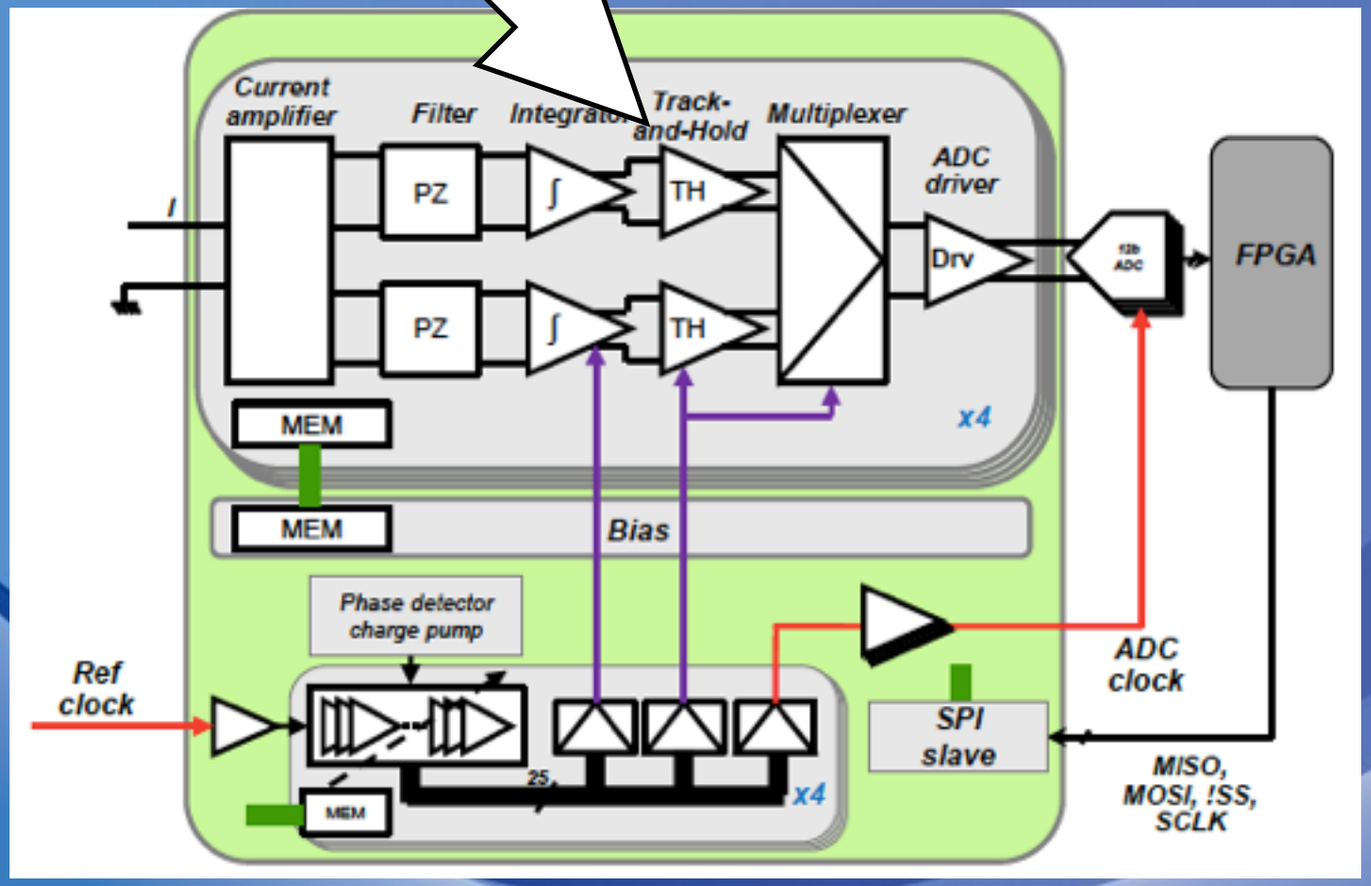
# LHCb Calorimeter upgrades

Calorimeter electronics upgrades motivated by improved L0 trigger system:

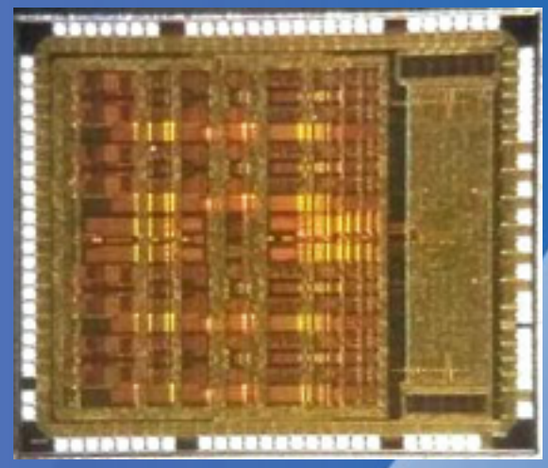
- Trigger in software
- Readout @ 40 MHz
- Scheduled for LS2 shutdown (2018)






- Reduced PMT bias current to extend lifetime. Delay line noise
- Front-end ASIC implementation with increased gain/reduced input series noise
- Development in AMS SiGe 0.35um



- Prototype (v.3 received last July) designed to test key features of the circuit
  - Electronically cooled input impedance through current mode feedback
  - Low noise performance
  - Dynamic range
  - Track and Hold synchronisation with ADC through precise (1ns) synthesised delay lines (DLL)

# CMS Calorimeter Upgrades

2013 2014 2015 **LS1**

- Multi-anode PMTs in Hadronic Forward (HF) calorimeter
- HF Back-end (μ-TCA modules)

2016 2017

- Back-end HCAL
- HF Front-end

2018 2019 **LS2**

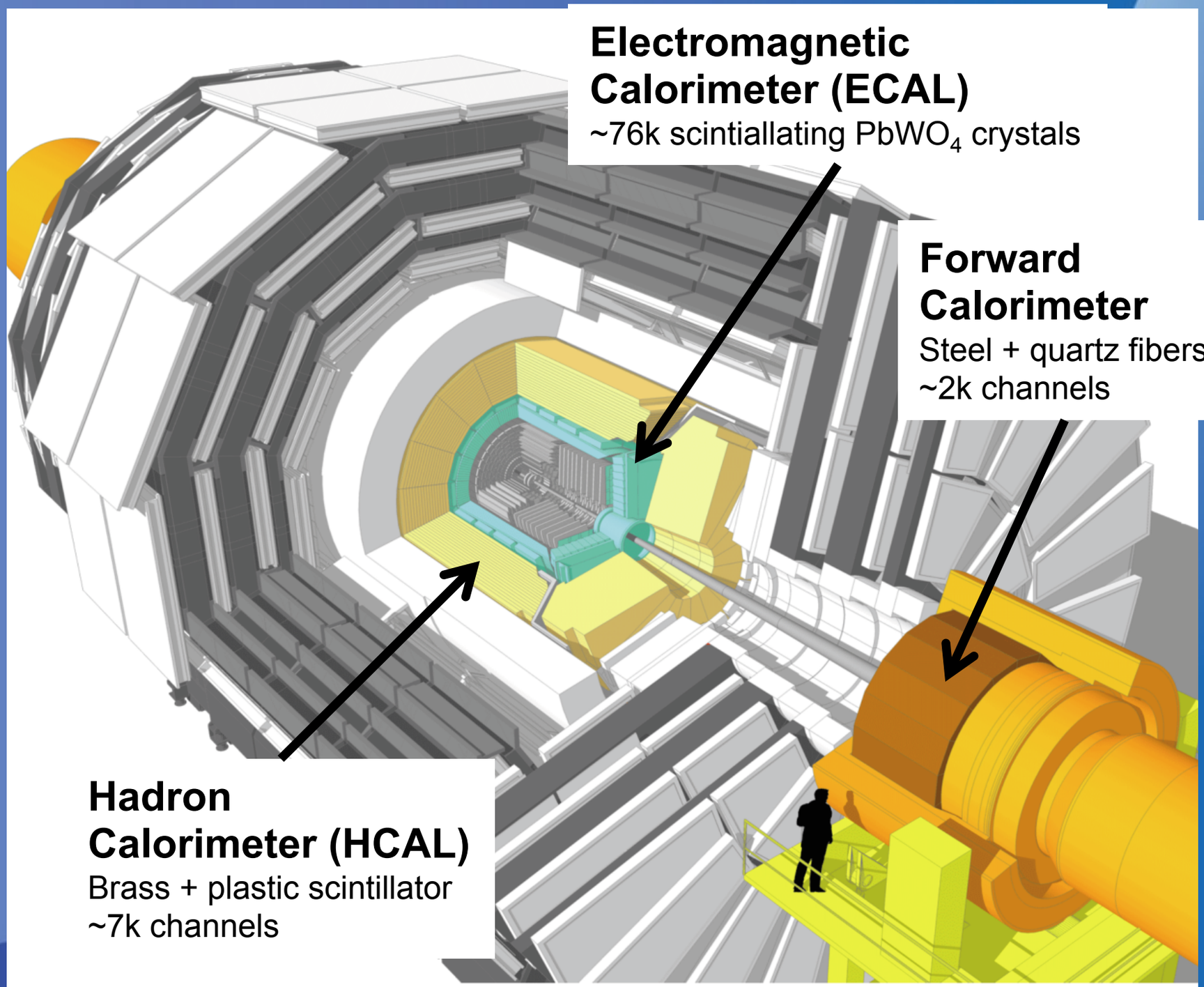
HCAL photo-detector (SiPM) and front-end

2020 2021 2022

2023 2024 2025 **LS3**

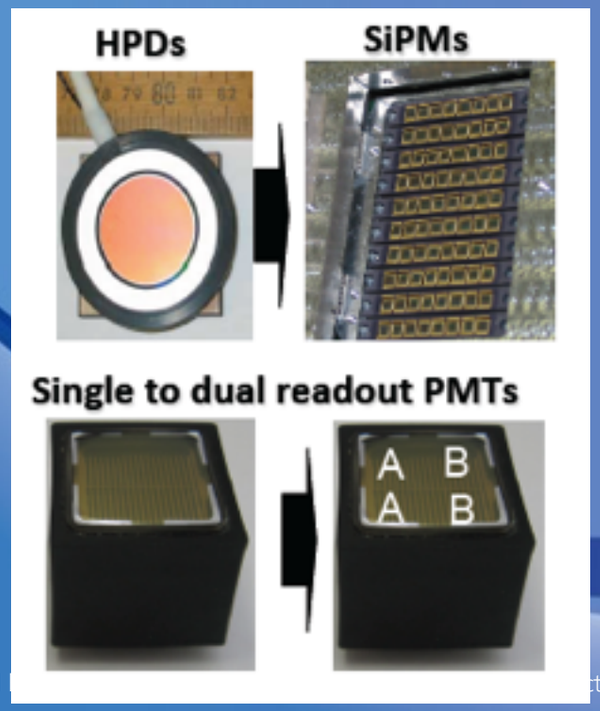
ECAL: readout upgrade/ new Endcap calorimeter

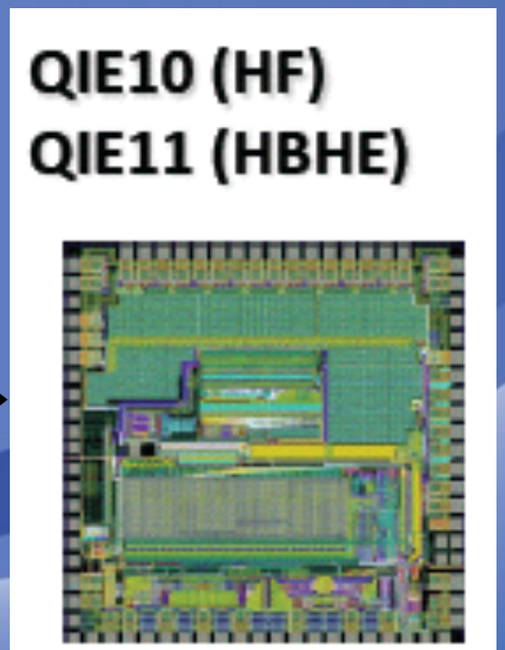
2035 ...

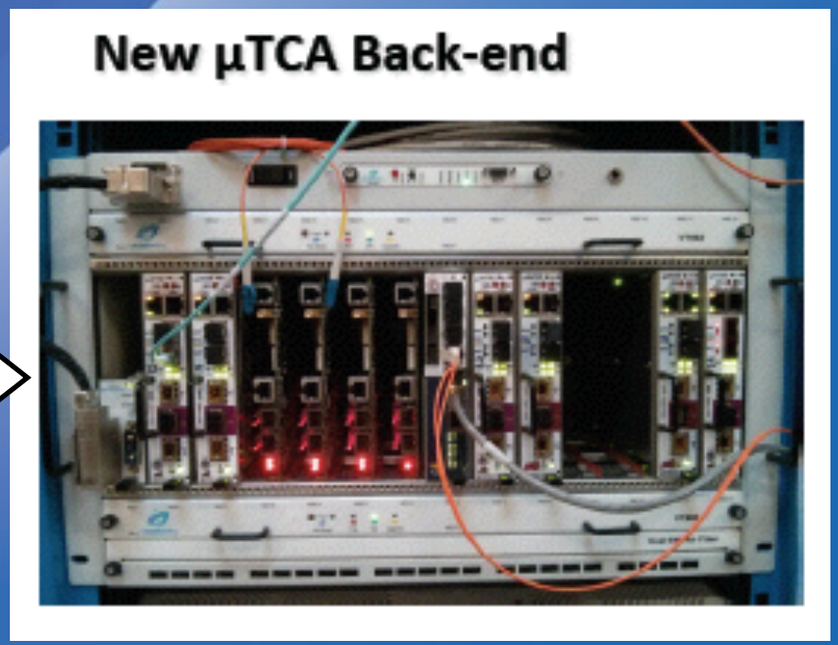


# HCAL/HF Readout Electronics

- New photodetectors to reduce spurious signals and improve reliability
  - Front-end and Back-end electronics upgrade staged between LS1 and LS2
- Improved background rejection using precision timing with new FE ASICs
- Higher granularity allows depth segmentation to access longitudinal shower development: improved calibration and shower reconstruction, and improved isolation in trigger and offline analysis
- Front-End Electronics:
  - **Charge Integrator and Encoder (QIE) ASIC in AMS 0.35um SiGe BiCMOS process**
  - Rad tolerant FPGA (ProASIC3) to synchronize and format data from several QIEs
  - CERN GBTx (4.8 Gbps data link) and VTTx to transmit data optically to the back-end
- Back-End Electronics uTCA format



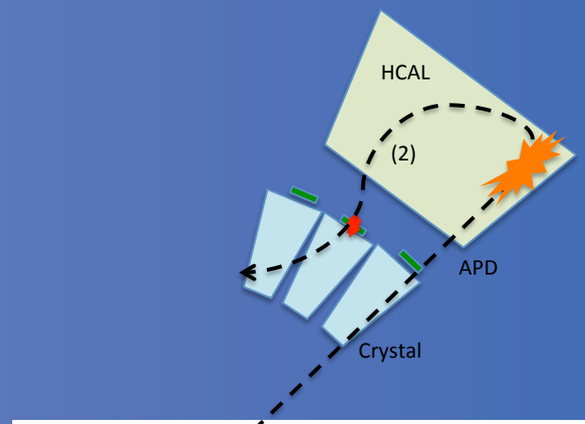
# ECAL (Barrel)

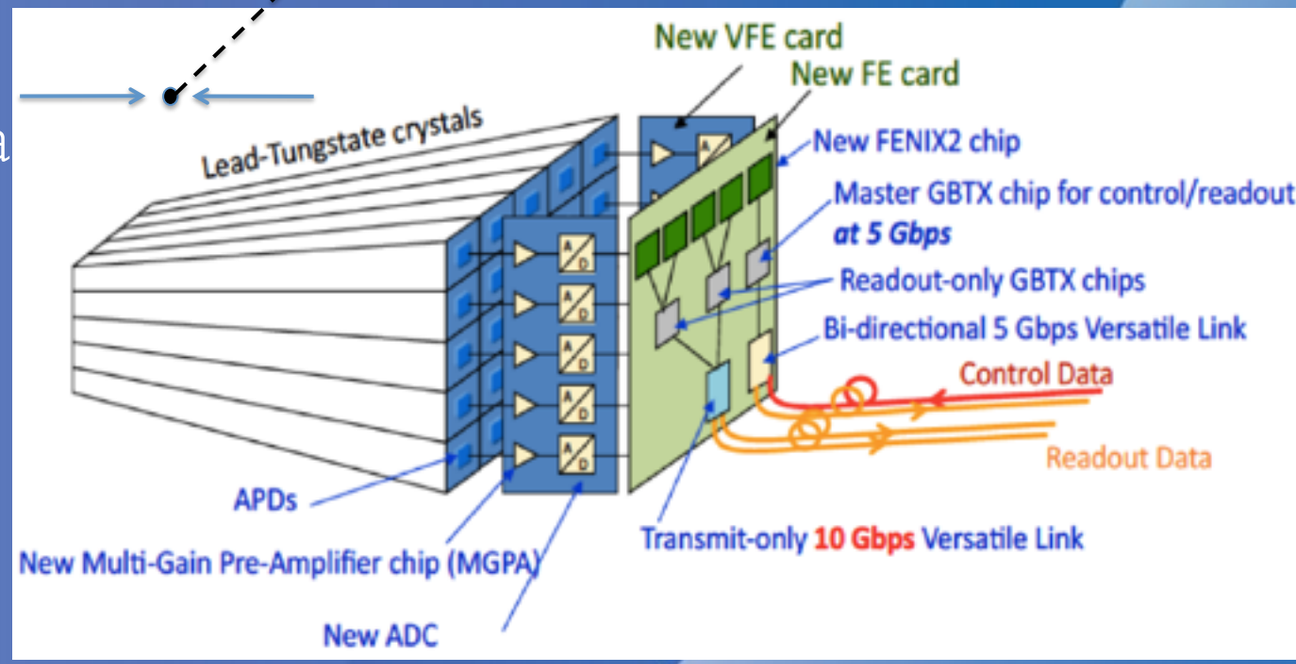
Upgrade during LS3 needed to be compatible with the Trigger requirements:

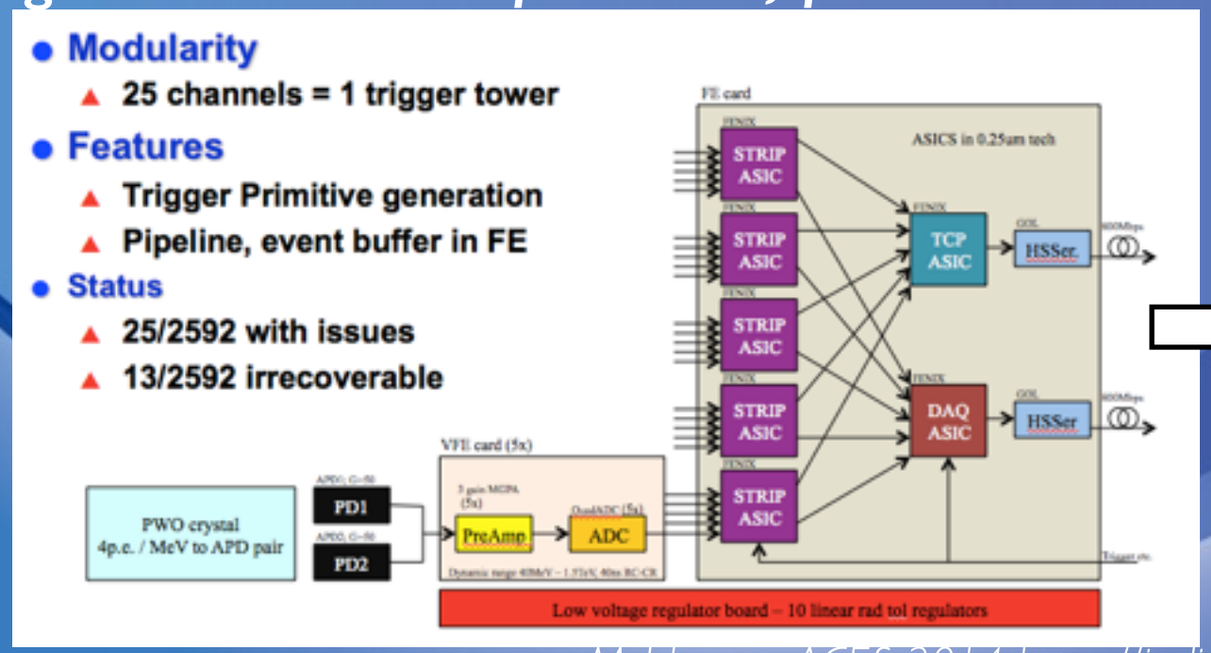
- Rates up to 1MHz (vs. today's150kHz)
- Latency up to 25us (today's max. ~5us)

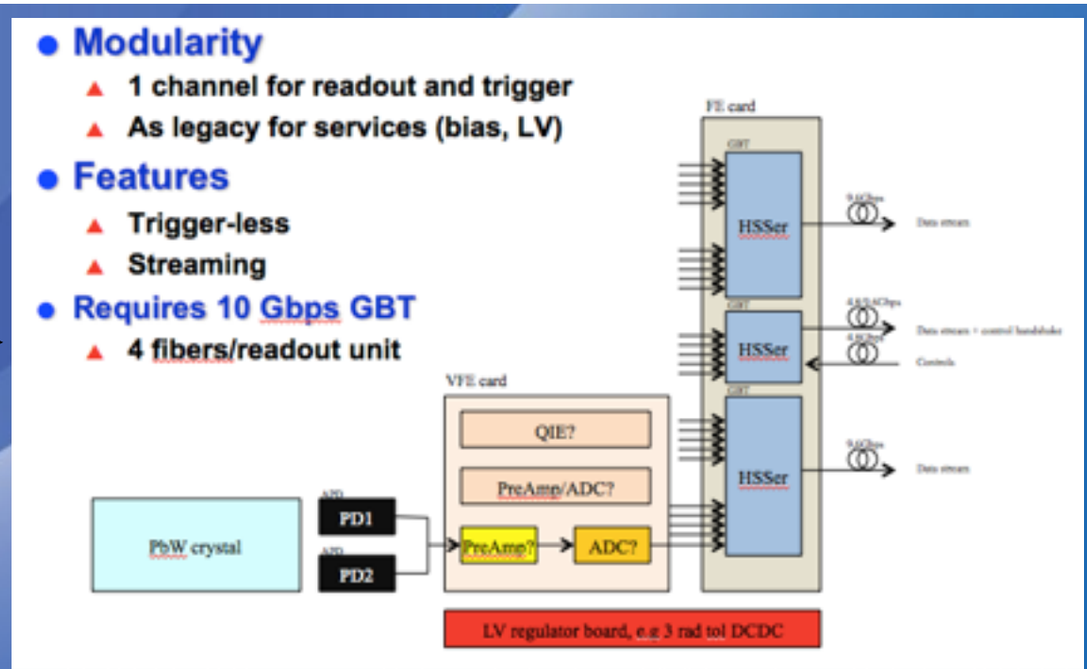
Motivated also by improved reliability and by a more robust mitigation of spikes (hadrons interacting with APDs in ECAL barrel) for the pileup expected @ HL-LHC.

***Increased modularity of the front-end, data streamed off-detector, no trigger primitive generation in the front-end, fast links***



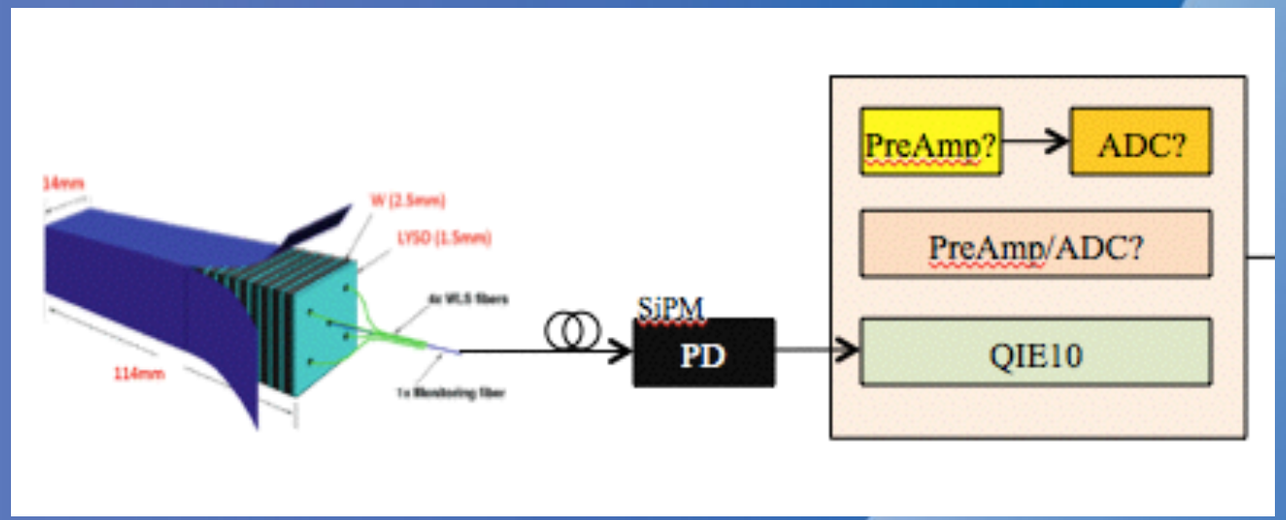

M. Hansen, ACES 2014 https://indico.cern.ch/event/287628/session/5/contribution/44/material/slides/0.pptx

# Endcap Calorimeters

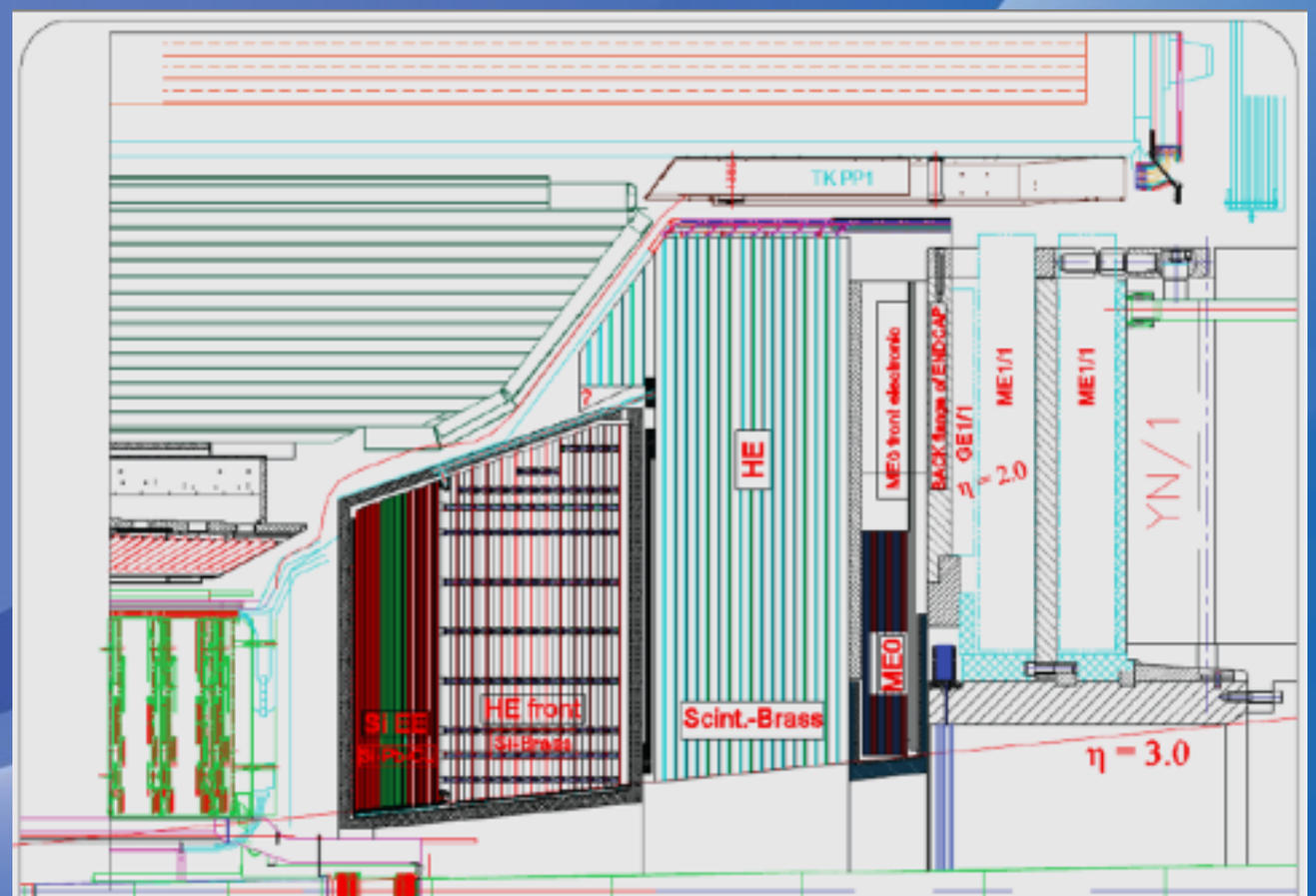
Endcap ECAL and HCAL will be suffering radiation damage and will need to be replaced in LS3

Two options considered:

1. **Shashlik** (new ECAL and fully rebuilt HCAL):
   - ***Readout very similar to ECAL barrel and HCAL Phase-I***

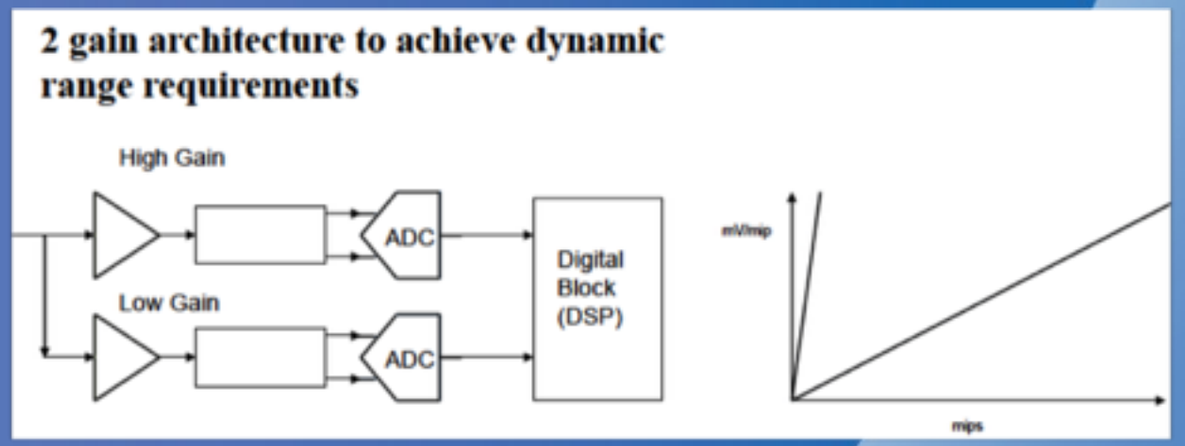


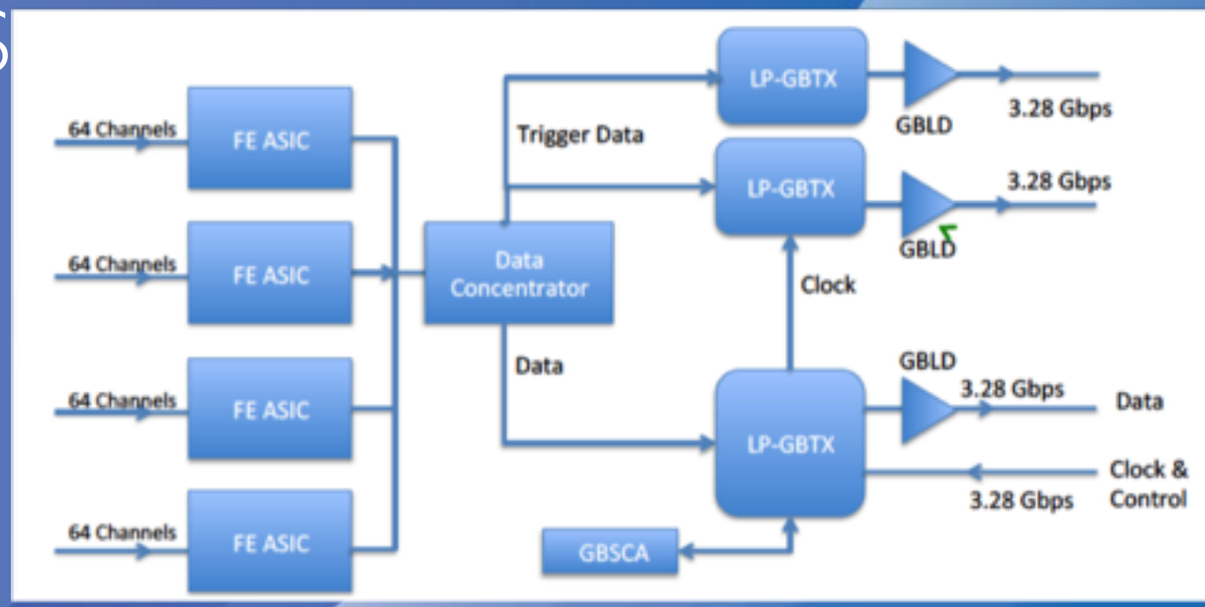

2. High Granularity Calorimeter (HGC)
   - **EM calorimeter**
     - 30 layers Si+Pb/Cu
     - 420m$^2$ pad detectors
   - **Front Hadronic Calorimeter**
     - 12 layers of Si+brass
     - 250m$^2$ pad detectors
   - **Rebuilt-half HE**



# HGC Electronics challenges

- 5M channels
- Detector Capacitance: 50-100pF
- Peaking Time: 15-20ns
- Digitization:
  - Sampling Frequency 40/80 MSPS
  - Dynamic Range: 12-bits
  - Resolution: 8-10 bits
- Trigger Data @ 40MHz
- Full readout @ L1 max rate
- Power: 15mW max
- Radiation Levels: up to $10^{16}$ n/cm$^2$ and several MGy



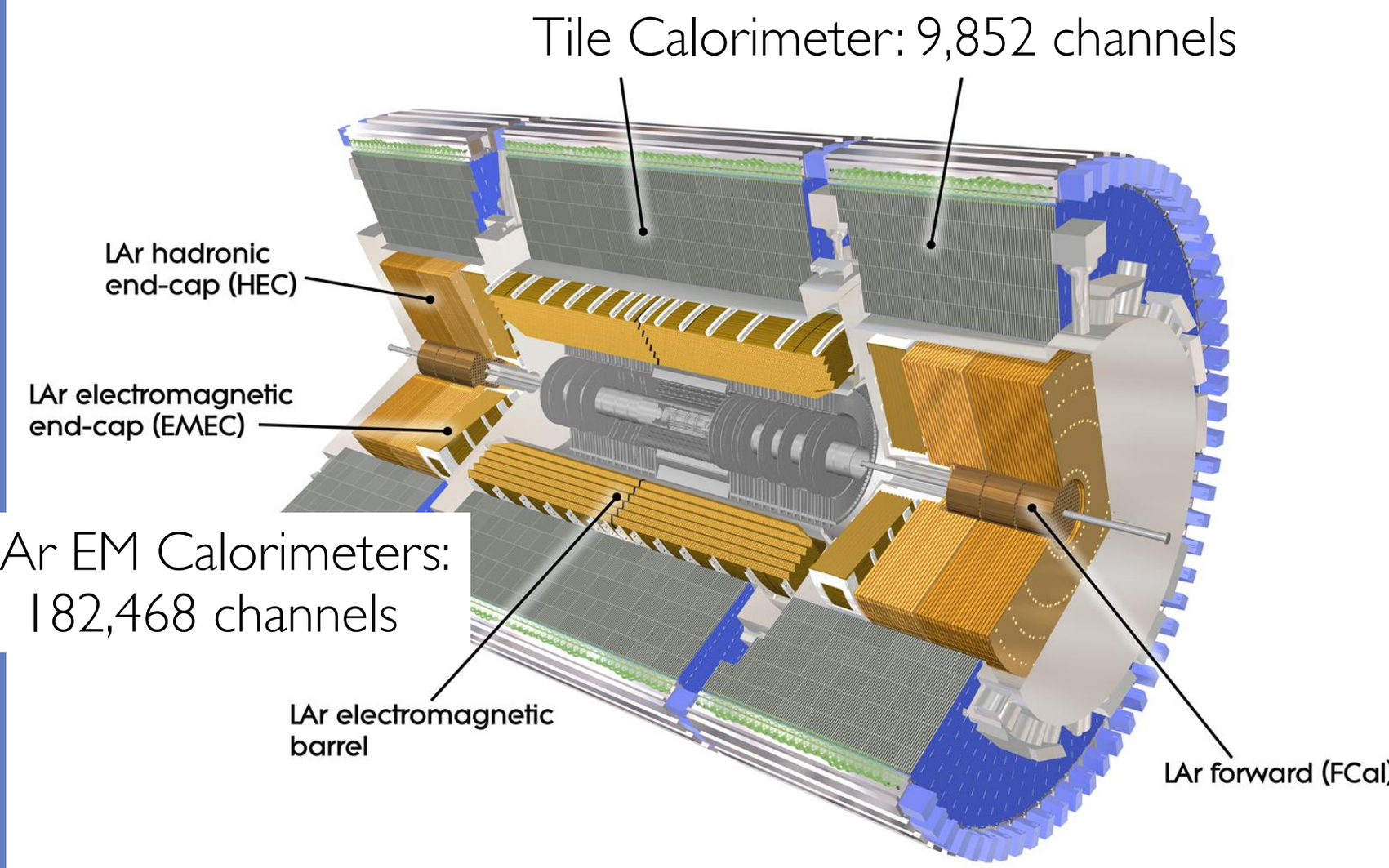

~90000 electrical links & 15000 5 *Gb.s*$^{-1}$ optical links

# ATLAS Calorimeter Upgrades

2013
2014
2015
2016
2017
2018
2019
2020
2021
2022
2023
2024
2025
…
2035

## LS1

- Consolidation (e.g. LV power supplies)
- Phase-I LAr demonstrator




## LS2

LAr calorimeter trigger readout upgrades

## LS3

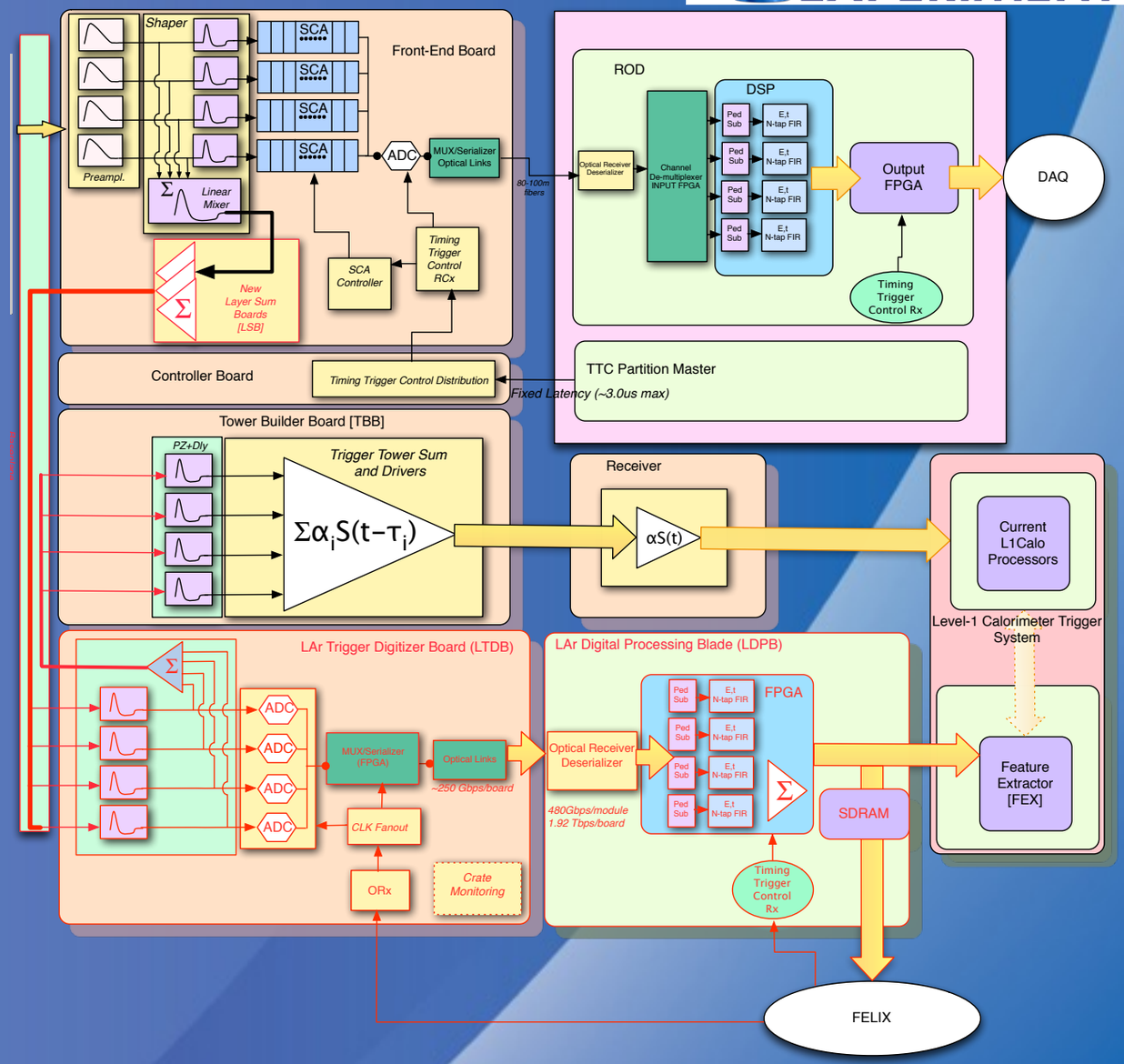
- Upgrade of FE and BE of all (LAr and Tile) calorimeters
- [FCal upgrade]

*Motivations: Radiation damage, ageing, improved reliability, new trigger requirements*

# Phase-I LAr upgrades

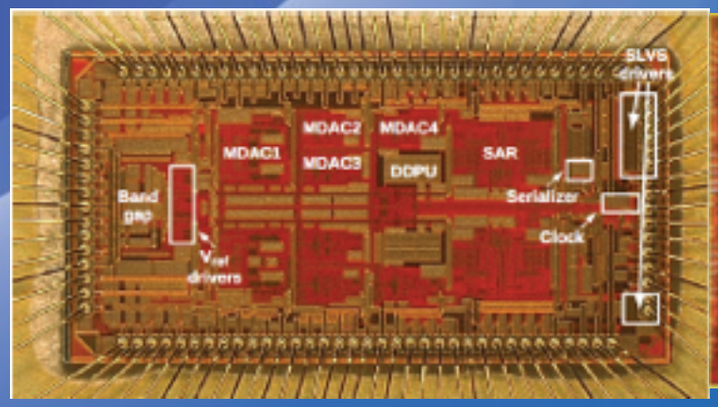
**x10 increased granularity EM calorimeter trigger readout for better pileup rejection**

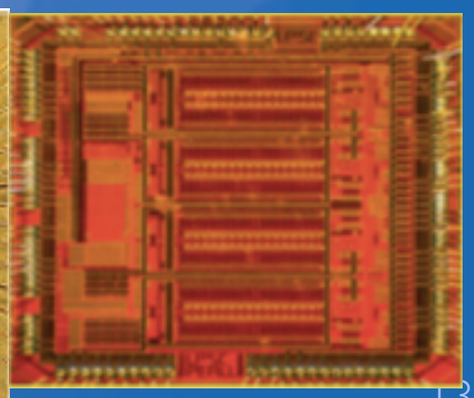
- From Trigger Towers ($\Delta\eta\times\Delta\varphi$=0.1x0.1) to **Super-Cells** ($\Delta\eta\times\Delta\varphi$=0.025x0.1) in the first two layers of the EM calorimeter by upgrading components of the Front-End electronics on-detectors and installing new boards: **LAr Trigger Digitizer Boards (LTDB)**: ~30k channels




**40 MHz 12-bit ADC required:**

- ***Target: 12-bit @ 40MHz, serial output, power ~100mW/channel***
- COTS evaluation
- 2 ASIC independent developments on CMOS 130nm:
  - Mixed architecture: pipeline (8-bits) + 4 SAR (4-bits)
  - Full SAR architecture
- Recent review to select baseline with mixed architecture

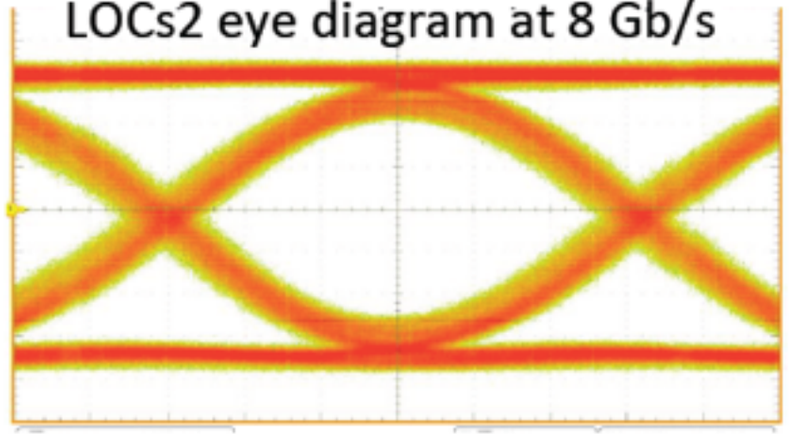


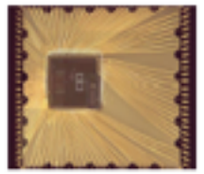
# Phase-I LAr upgrades

**Serializer, laser driver optical transmitter:**

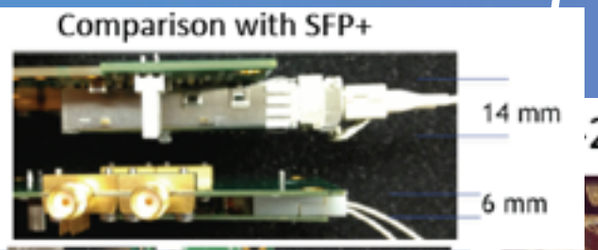
- GBTx + VTTx
- *Links on Chip (LoC) [serializer] + laser driver in SoS 250nm and customised MTx based optical module*



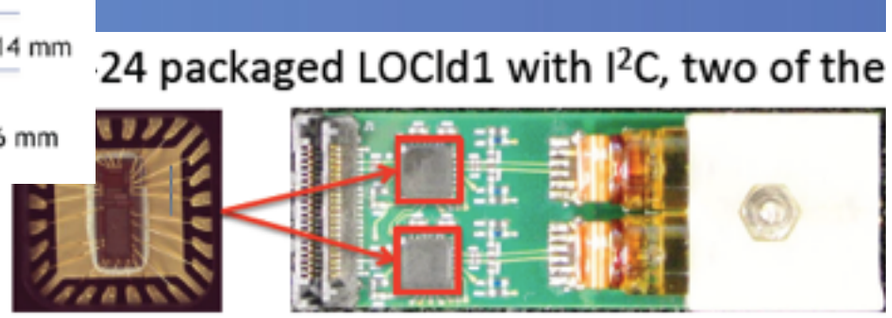

LOCs2 prototype QFN-100 package



- LOCs2 is a 2-channel, 8 Gb/s per channel, serializer
- Its LCPLL tunes from 3.3 to 4.25 GHz with RJ ~ 1 ps.
- Power consumption 1.25 W for the chip with both channels run at 8 Gb/s.

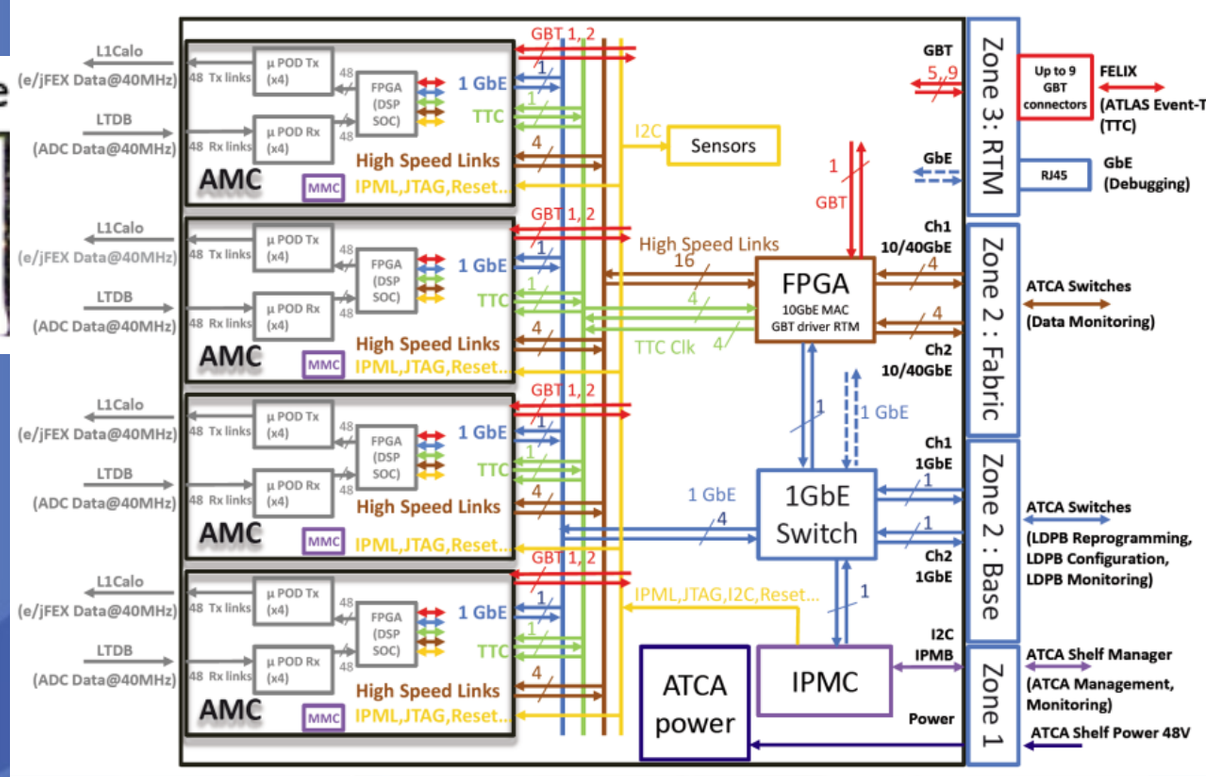



24 packaged LOCld1 with I²C, two of the



## LAr Digital Processing Blades (LDPB)

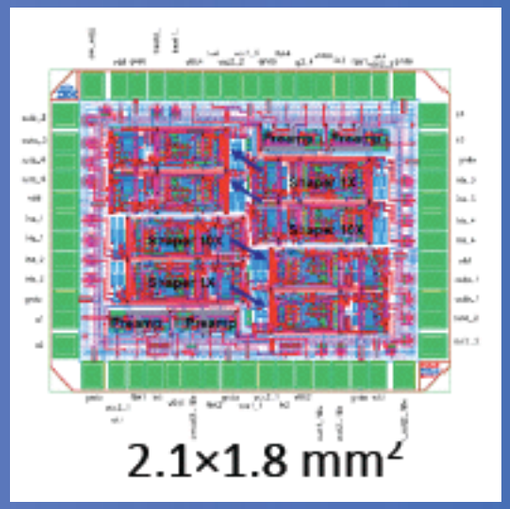
- ATCA format
- 4 Main processing FPGAs (Altera Arria10) on (4) AMC mezzanines
- 4x8 MicroPods for I/O from detector to LVL1 trigger Feature Extractors (48 Rx + 48 Tx)

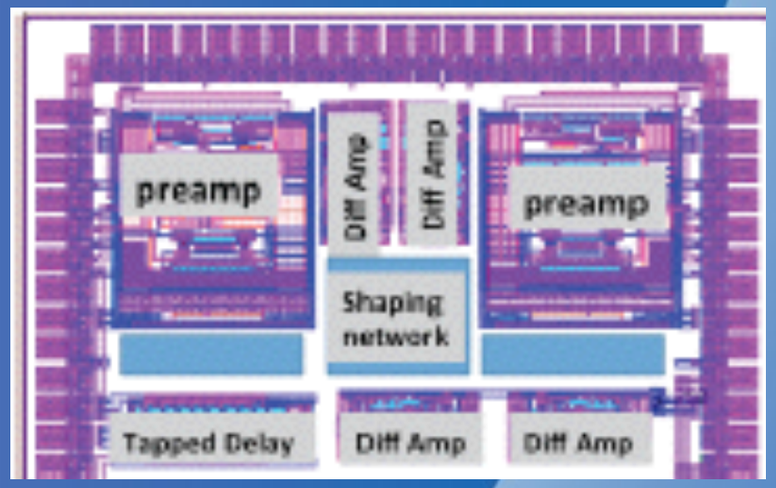



# Phase-II LAr upgrades

**Analog front-end (preamplifier and shaper) in SiGe BiCMOS processes:**

- LAPAS: IBM 8WL (2008)
- IHPPSD: IHP SG25H3P (2011)




**Continuing developments in SiGe (AMS)**

**Explore 65nm CMOS technology from TSMC**

- For analog readout: on-going feasibility study to prove consistency with noise and dynamic range requirements
- Building-up on experience on ADC design for Phase-I to migrate toward 65nm development aiming at a further reduction in power (<10mW/channel)
- Similarly for the serialiser and the drivers to the optics

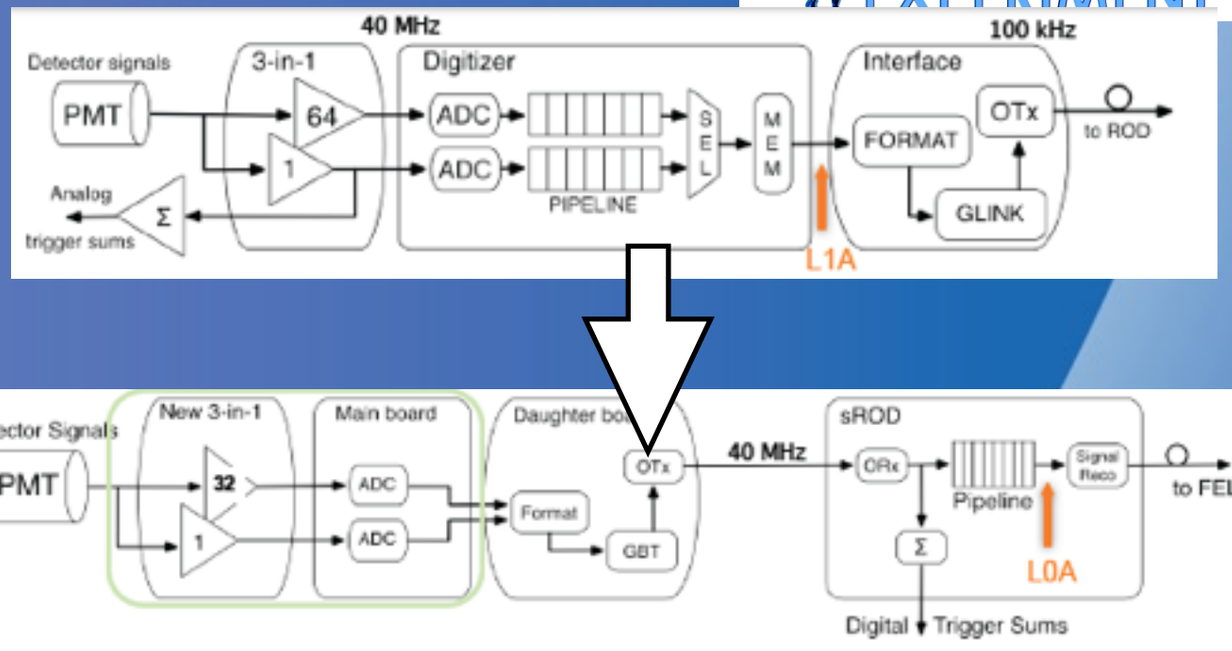
**Considering and exploiting the possibility of full integration in a single ASIC: System on Chip (SoC):**

- Simplification of the Front-end boards and of all the services on-detector (power distribution and cooling)

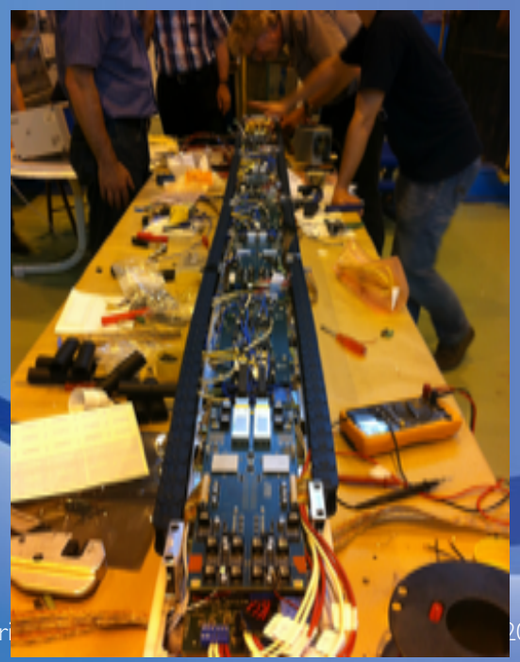
# Tile Calorimeter

- Transmission of full data @ 40 Mbps to the back-end sRODs
  - ***Full redundancy (x2) and no gain selection in the front-end***
  - Pipelines and de-randomizer buffers in the back-end modules (sRODs)
  - sROD also providing digital information for the LVL0/1 trigger system
- *Simplification of the front-end and improved reliability (less interconnections)*

*Finer modularity: 1 electronics drawer splitted in 4 independent mechanical mini-drawers*




| | |
|---|---|
| Total data rate | ~80 Tb/s |
| Number of links | 4096 (+4096) |
| Data rate per link | 10 Gb/s |
| Links per Duper-Drawer | 4x4 (+4x4) |
| Data rate per SD | 160 (+160) Gb/s |



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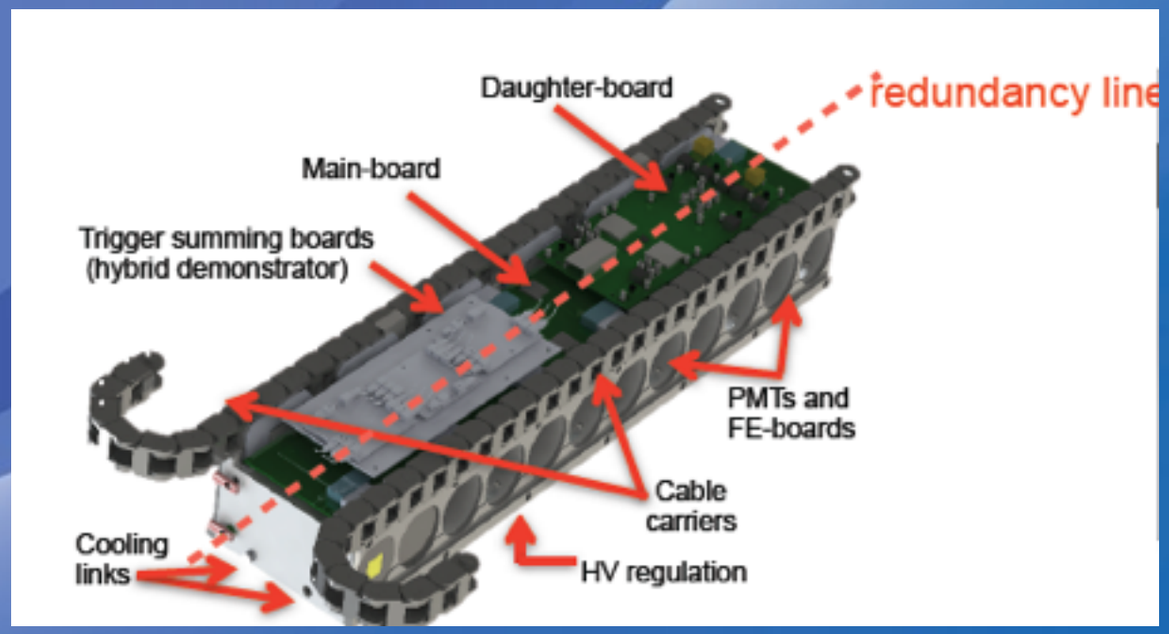
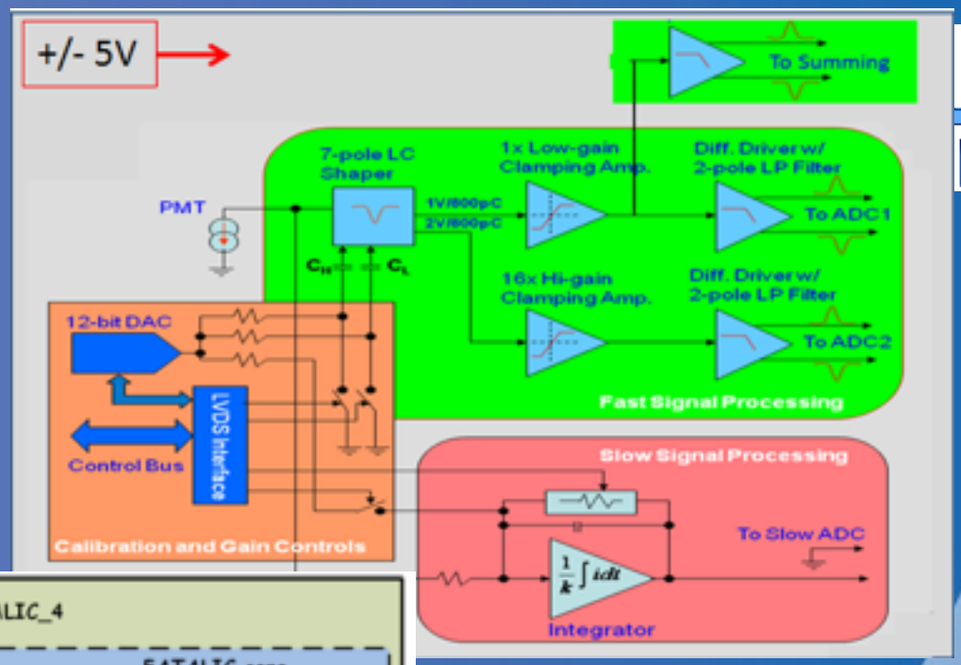
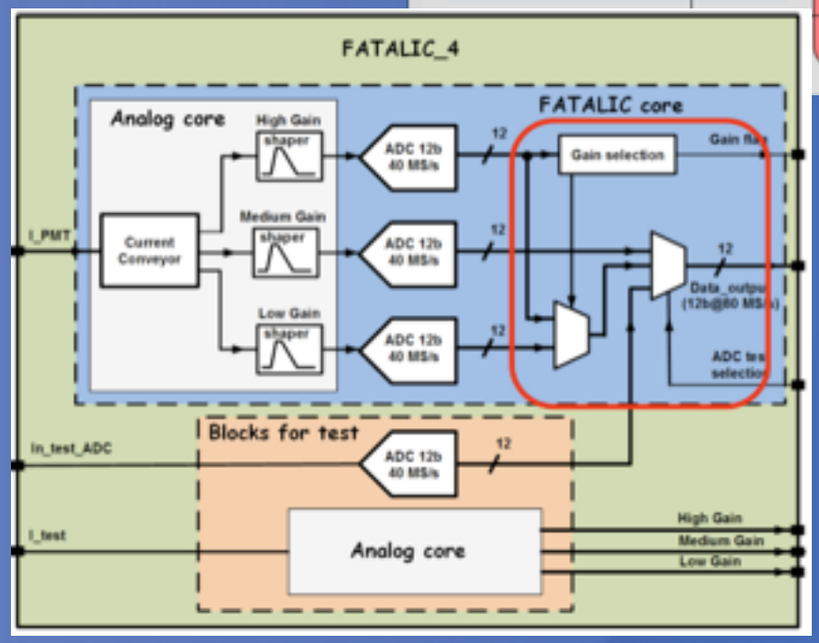
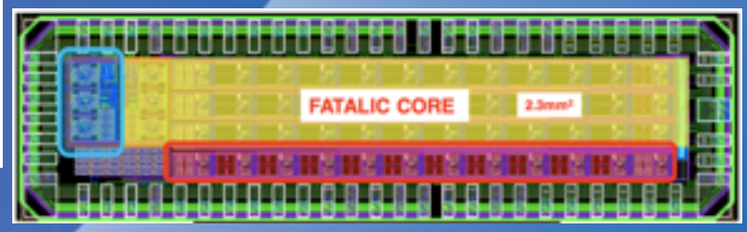


# Tile Calorimeter




### 3 Options for Front-End

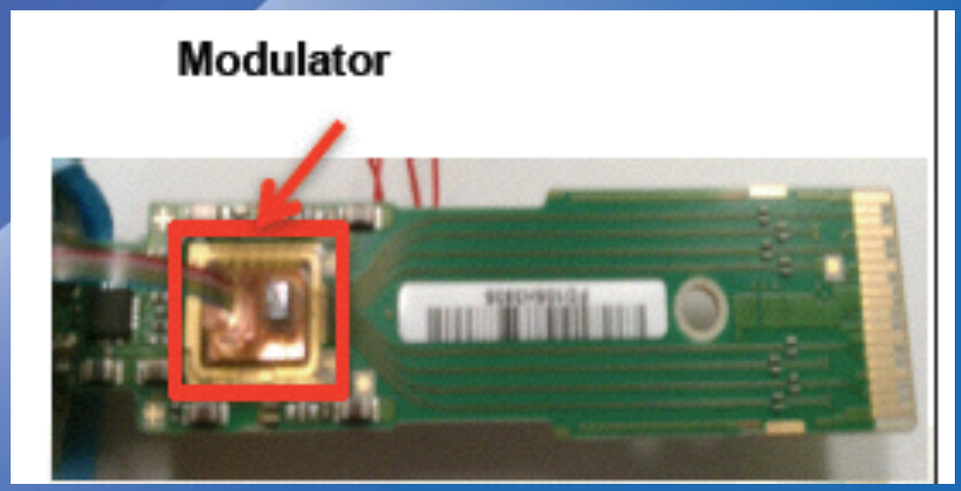
1. 3-in-1 board: based on COTS, revision of the current FE with higher radiation tolerance and lower noise components
2. QIE ASIC
3. FATALIC ASIC (IBM CMOS 130nm):
   - current conveyor
   - Shaping stage w. 3 gain settings
   - TACTIC 3x12-bit ADC
   - v. 4 prototype ready soon

### Data transmission:

- Kintex-7 FPGA (triple redundancy), GBTx
- 8 readout links: 1+1(redundancy) 4 mini-drawers

### Luxtera optical modulators *(130 nm SoI CMOS)*:

- 4 bi-directional channels: <14 Gbps/ch
- Excellent error rate: BER < $10^{-18}$
- SEE: no Tx errors for hadron fluence of $1.2 \times 10^{12}$ p/cm$^2$



# Summary

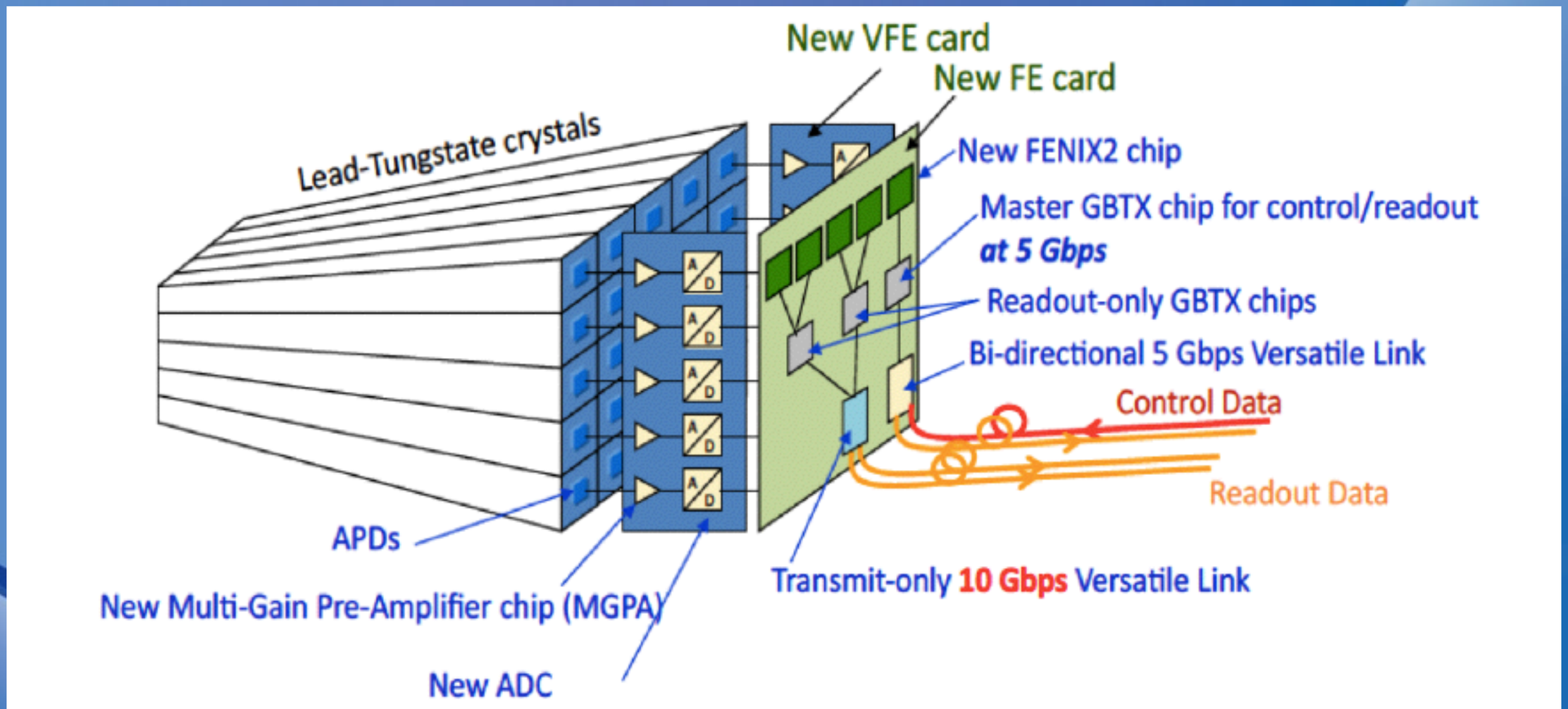
- **Common goal for the readout electronics of all the calorimeters is to meet the challenging pile-up conditions, radiation doses and fluence, and new requirements imposed by the upgrade of the trigger systems**
  - High detector granularity, and better timing measurements for improved triggers.
  - All channel readout @ 40 MHz
  - Radiation tolerant
- **Analog front-end (preamplifier, shaper) ASIC design detector specific.**
- **Possible (highly desirable) common developments across experiments for front-end ASIC designs**
  - IP block for a 16-bit, 11-12 ENOB, 40+ MHz digitizer
  - IP block for a fast serialiser
  - IP block for a high bandwidth laser driver
- **For each calorimeter ASIC developments with integration of different among the previous functional blocks may be beneficial to:**
  - simplify architecture of the front-end boards
  - reduce significantly power and complexity of the services and infrastructure (e.g. power and cooling)
- **Possible common developments for modular back-end electronics based on large FPGAs and very high density optical interconnects for signal processing** (e.g. energy scale calibration for each single detector element, signal feature extraction for object(s) reconstruction in the trigger readout)

# Additional Slides

# Calorimeter readout evolution toward HL-LHC

***Readout architecture w/o pipelines nor Level-1 trigger logic: data digitised and streamed off detector @ 40MHz.***

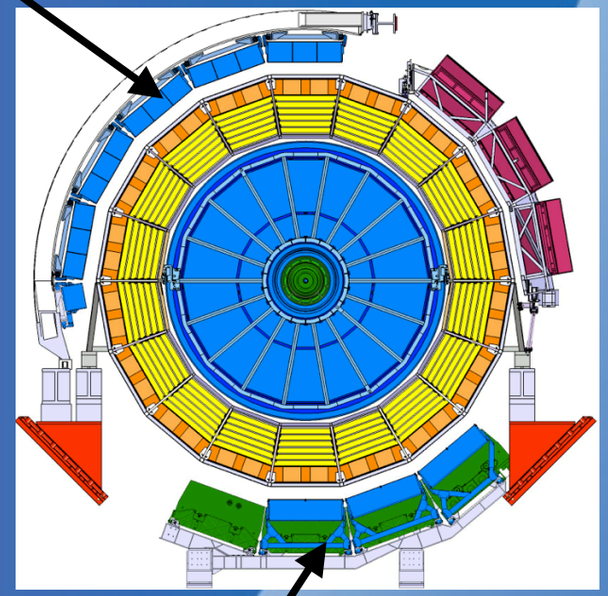
**CMS ECAL** upgrade: **Readout module with 2 links @ 10Gbps** (3 links @ 5Gbps) to be compared to 2 links @ 800Mbps in the current system



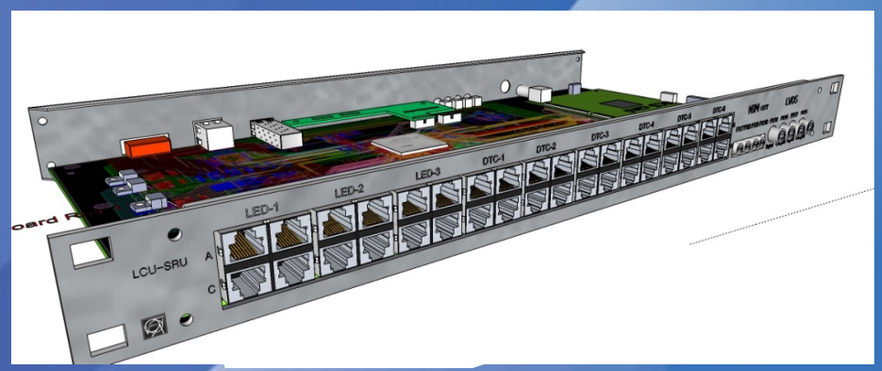
# ALICE Calorimeter Upgrades

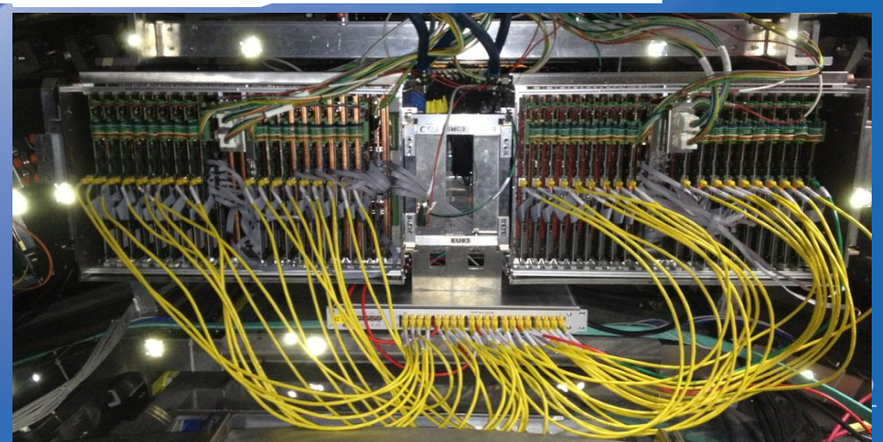
- Readout upgrade with Scalable Readout Unit (SRU) in LS1 (40% more readout channels)
- Direct front-end to network connection (point-to-point): 40Mbps input and 1 Gbps Ethernet output
- SRU installed for EMCal in May 2013
- Installation for PHOS being completed
- No further electronics upgrades foreseen for these two detectors
- Possible new Forward Calorimeter (FoCAL) after LS2

EMCal Pb-Scintillator
(after LS1: 17664 towers for trigger and readout)



PHOS PbWO4
(after LS1: 14336 channels)

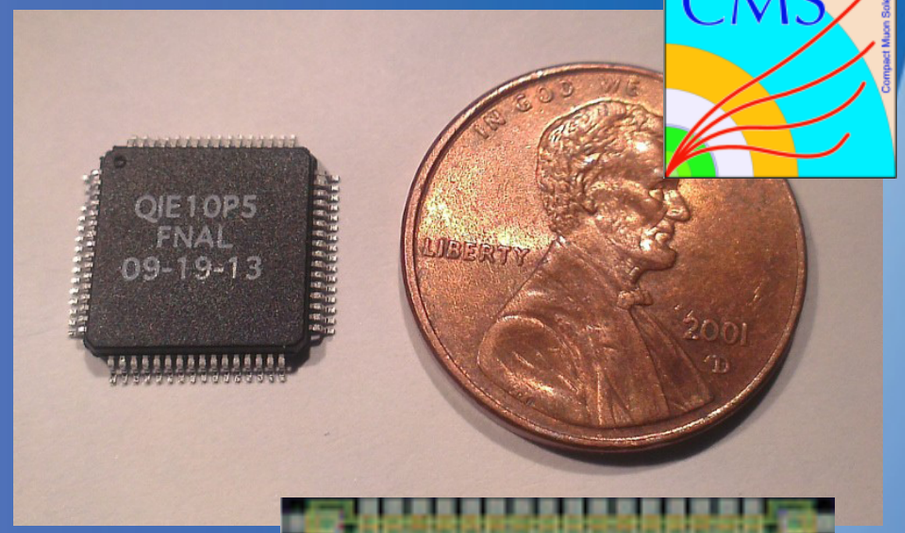


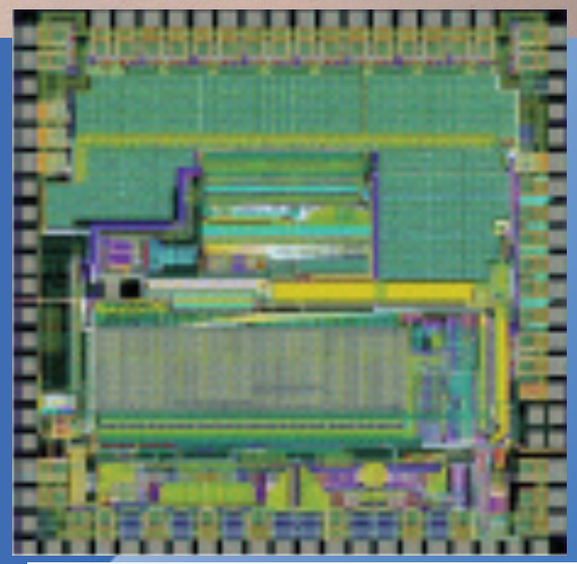



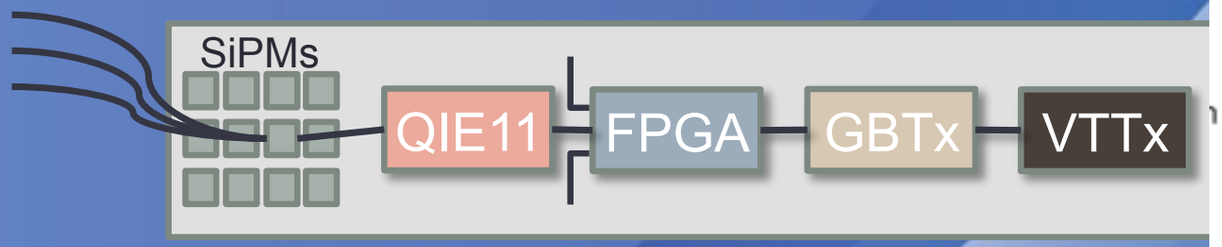
# HCAL/HF Front-end

**Charge Integrator and Encoder (QIE) ASIC in AMS 0.35um SiGe BiCMOS process**

- Radiation Tolerant (TID: 10kRad, NIEL: $2\times10^{12}$ $cm^{-2}$ 1 MeV eq., Hadron Fluence: $10^{10}$ $cm^{-2}$)
- Integration and digitisation in 25ns buckets (deadtimeless)
- Rising edge TDC, resolution <800ps
- 17-bit dynamic range: 3fC-330pC (1 TeV)
- 4 gain range digitisation: 6 bit mantissa and 2 bit exponent)

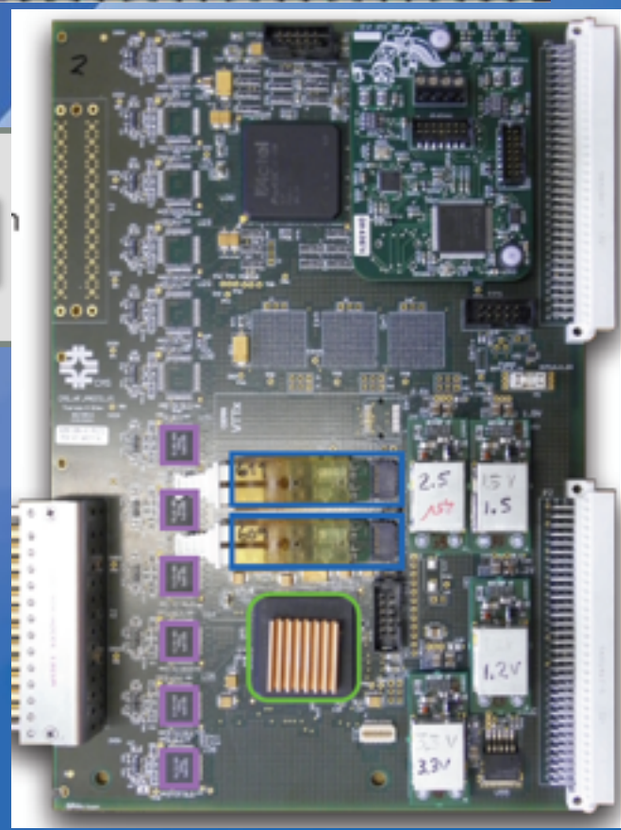


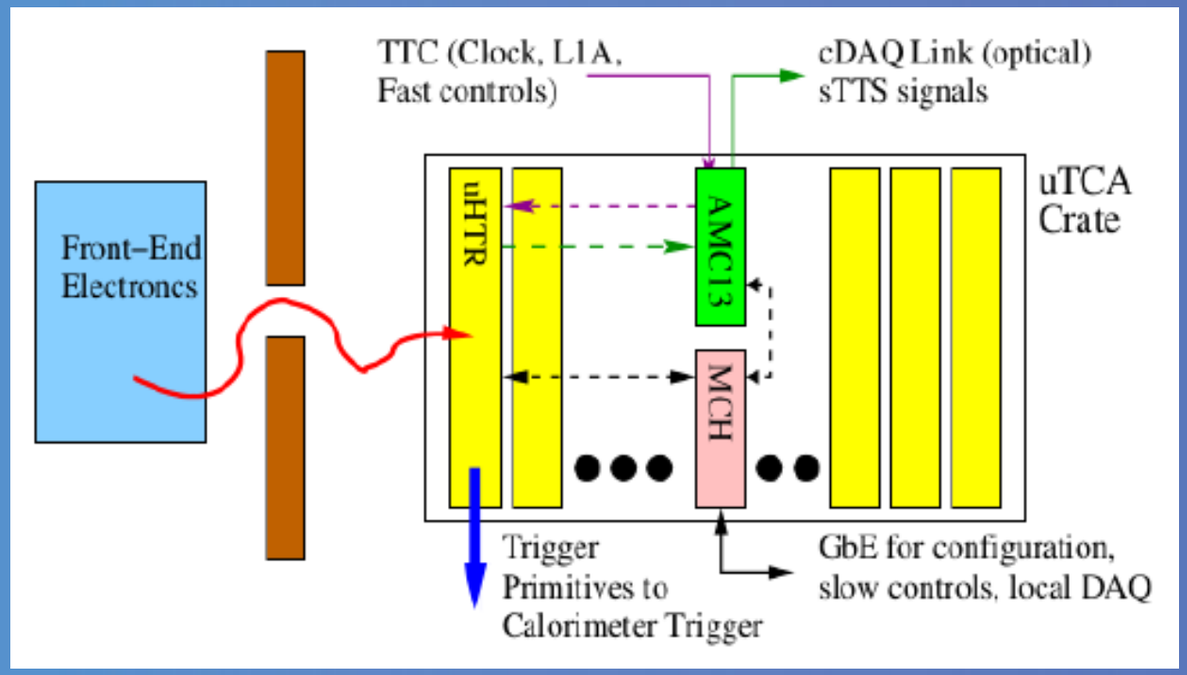


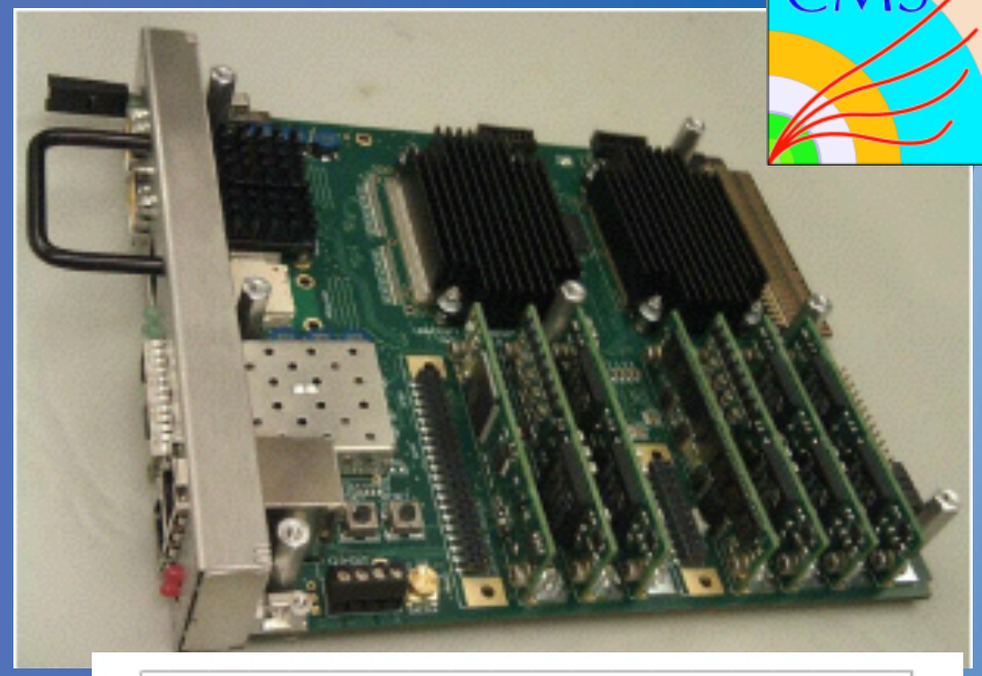

## Front-end Electronics

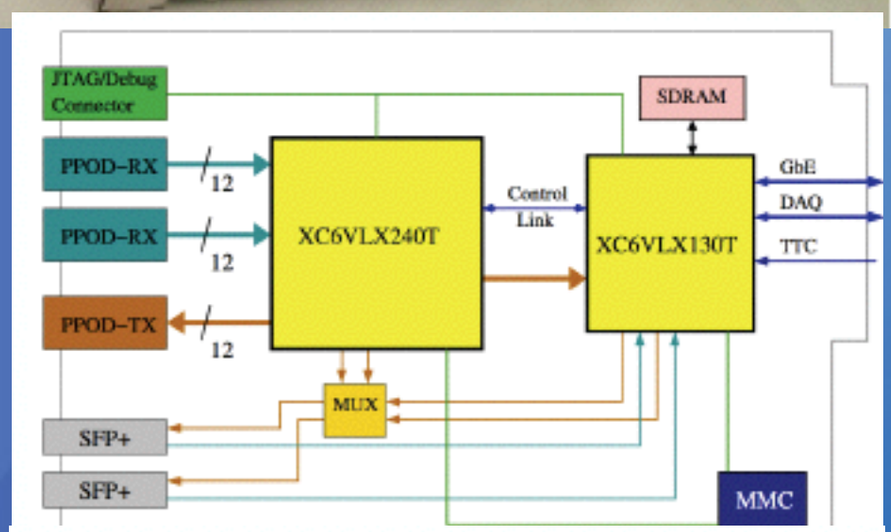
- Rad tolerant FPGA (ProASIC3) to synchronize and format data from several QIEs
- CERN GBTx (4.8 Gbps data link) and VTTx to transmit data optically to the back-end

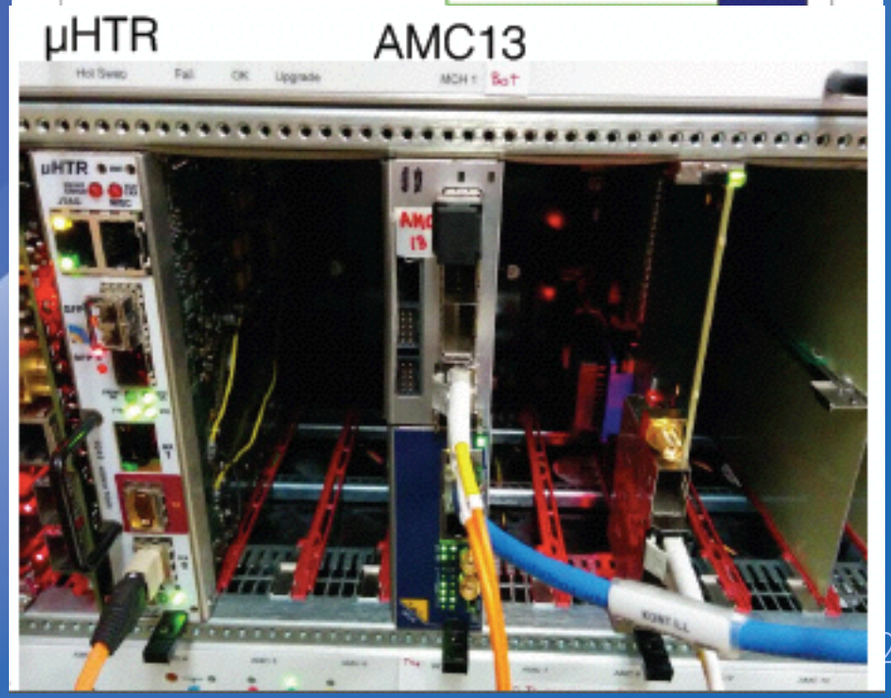


# HCAL/HF Back-end





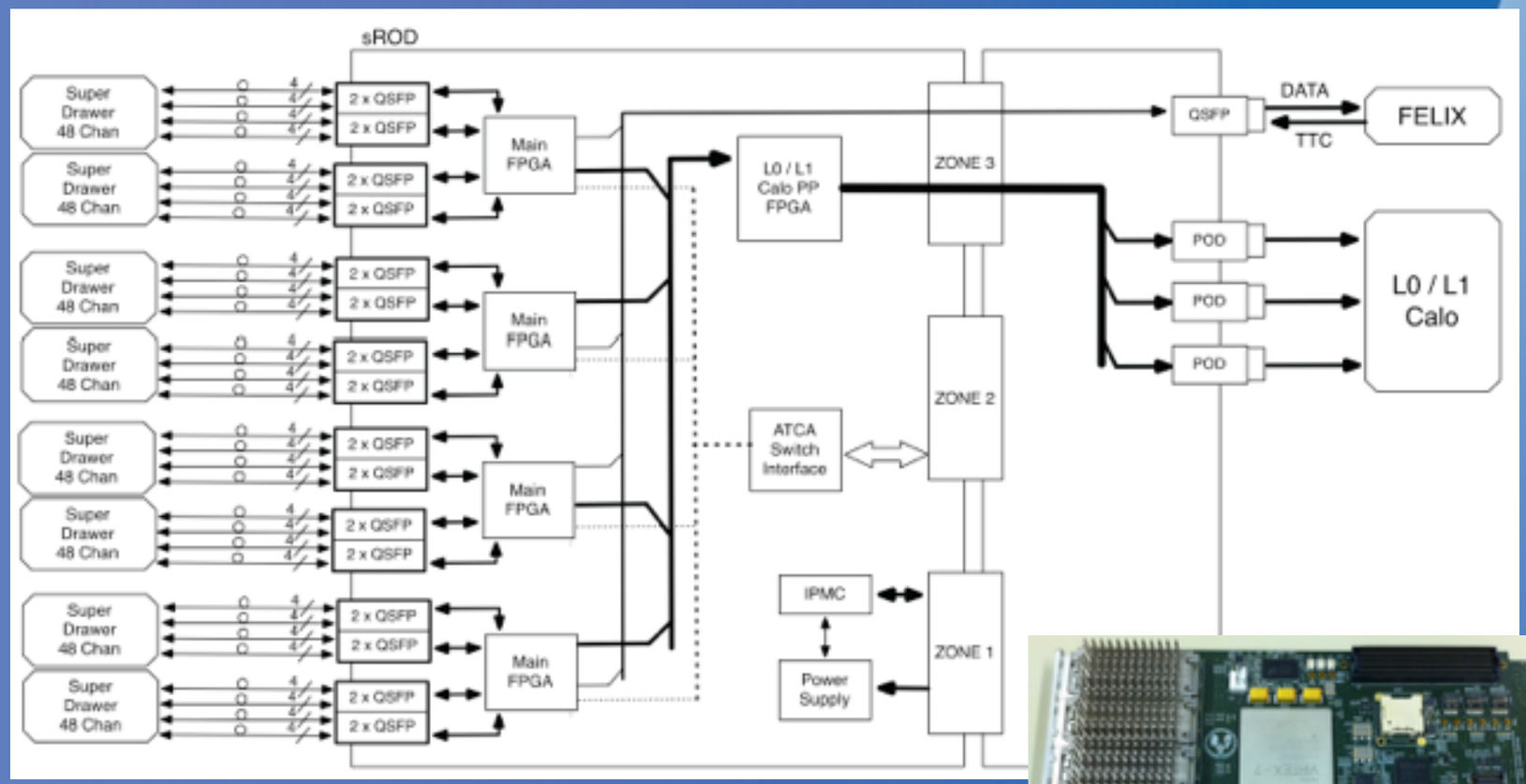

**Modular electronics in the back-end based on µTCA**

- **µHTR modules:**
  - 2 Virtex-6 FPGAs
  - Receive data from front-end (24 links)
  - Compute trigger primitives
  - Transmit to L1 trigger processors
  - Buffer data for readout and apply zero suppression
- **AMC13 boards:**
  - Build event collecting fragments on L1 through backplane and transmit to DAQ
  - Also used for the upgraded mTCA trigger system

# Tile Calorimeter

## sROD architecture and format

- ATCA blade
- 32 QSFP input links
- 4 Main processing FPGAs
- 1 Output FPGA for interface to L0/L1 Trigger Processor




## demonstrator prototype: readout of 4 mini-drawers

- compliant with midsize AMC
- 4 QSFP inputs (4x12 PMTs)
- 1 Xilinx V7 48 GTX@10Gbps for data/DCS
- 1 Xilinx K7 28 GTX@10Gbps to interface current ROD/TTC and L1Calo