ALICE electronics co-ordination for upgrade

A. Kluge, March 26, 2014

For the ALICE collaboration

Outline

- Overview
- Common read-out unit - CRU

Specifications

- **Interaction rate Pb-Pb:**
  - **from 8 kHz → 50 kHz**
- **Trigger rate Pb-Pb:**
  - **from max. 3.5 kHz → 50 kHz**
- **All interactions are read AND recorded**

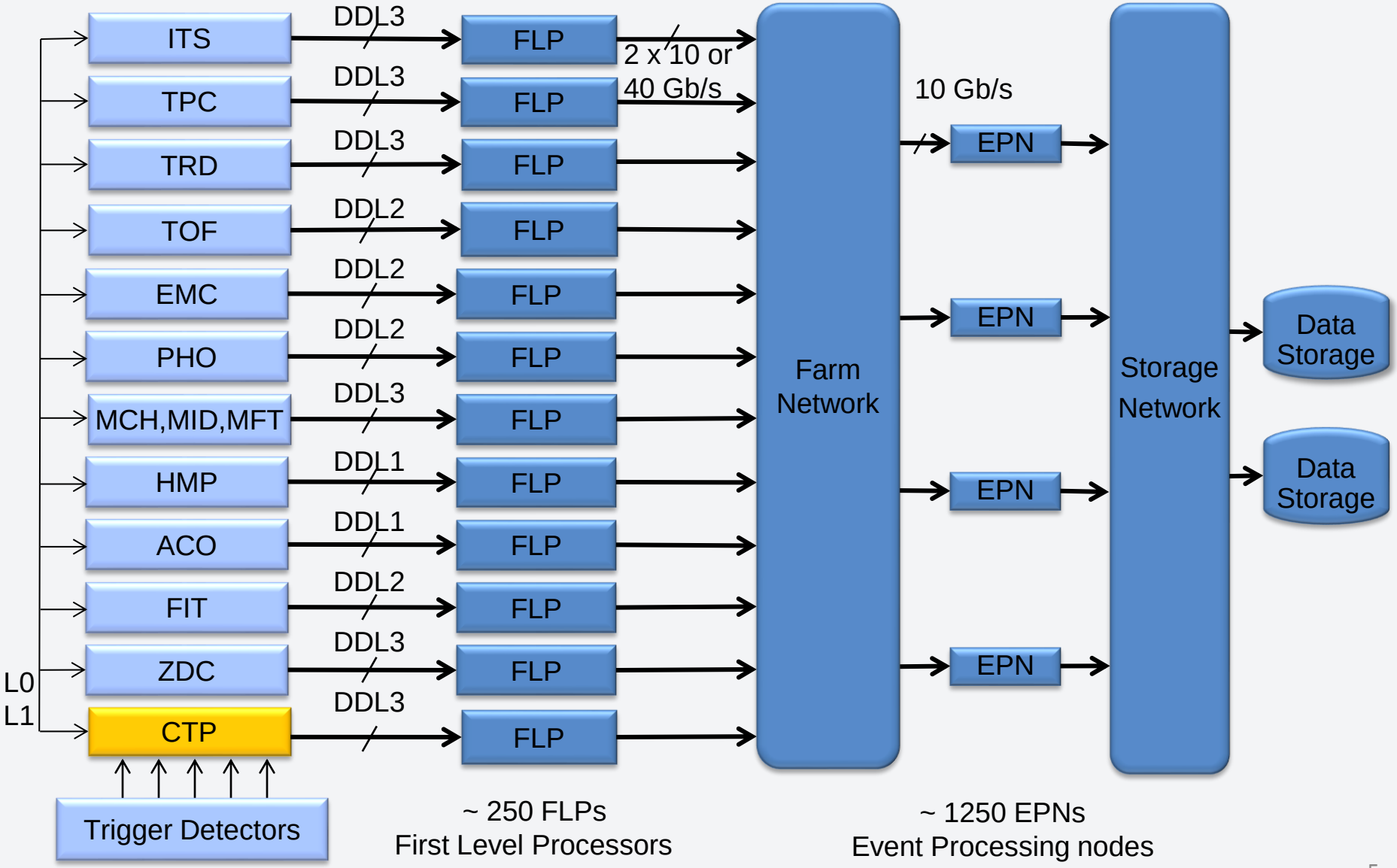
- **Interaction and trigger rate pp:**
  - **→ 200 kHz**
- **Data rate driven by Pb-Pb**

- **TPC is read continuous & trigger less**

Read-out & Trigger Upgrade architecture

O² hardware system

~ 2500 DDL links in total



Sub-detector parameter overview

Det	triggered by () = optional	Pb-Pb RO rate [kHz]	TTS FTL/TTC	CRU used
TPC	(L0 or L1)	50	FTL	y
MCH	(L0 or L1)	100	FTL	y
ITS	L0	100	FTL	*y
MID	L0 or L1	>100	FTL	y
ZDC	L0	>100	FTL	y
TOF	L0 or L1	>100	FTL	n
FIT	L0 or L1	100	FTL	n
ACO	L0 or L1	100	TTC	n
TRD	LM&(L0 or L1)	39	FTL&TTC	y
EMC	#L0&L1	46	TTC	n
PHO	#L0&L1	46	TTC	n
HMP	#L0&L1	2.5	TTC	n

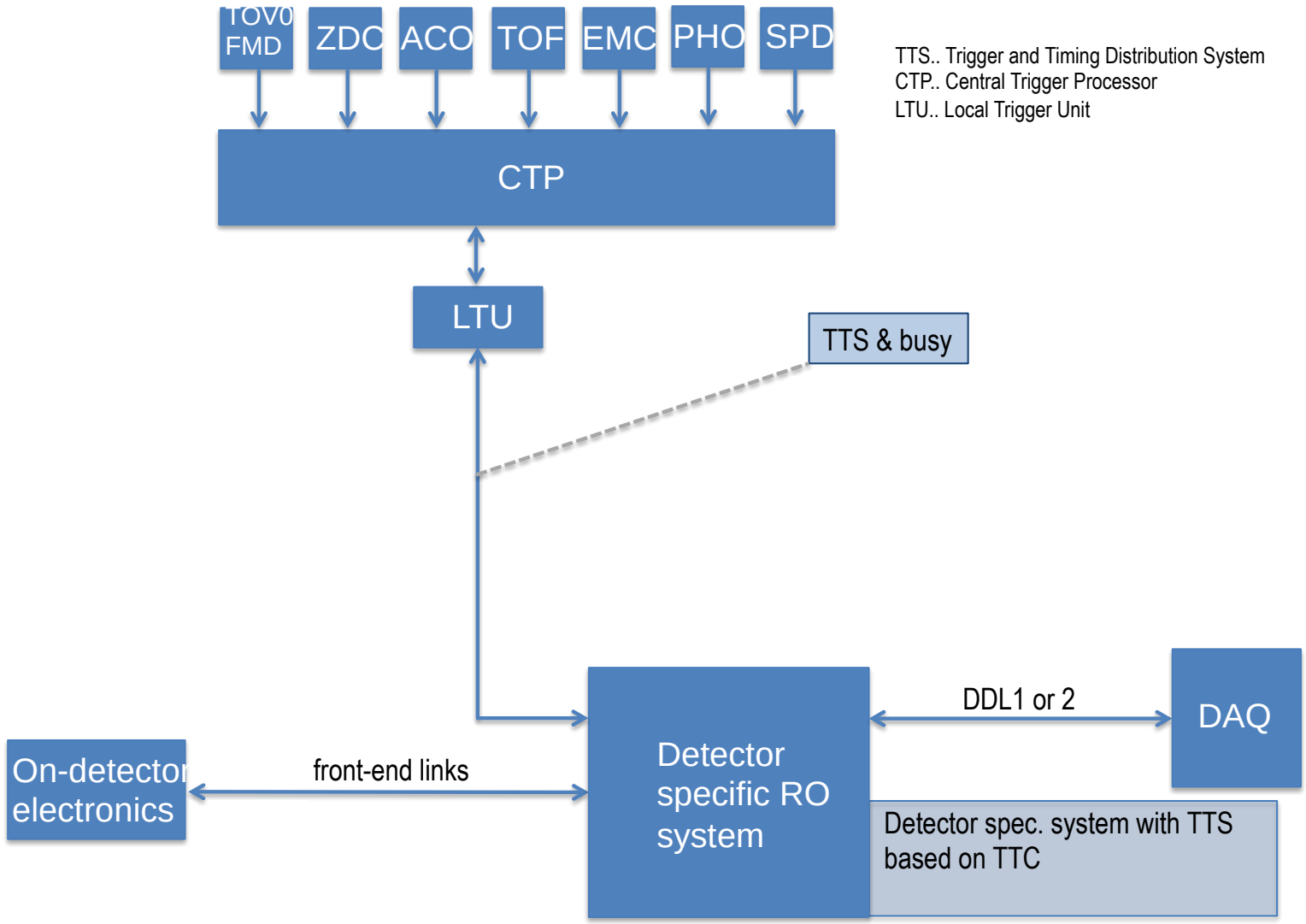
Sub-detector upgrade effort

Det	# channels	Run1&2 RO rate [kHz]	upgrade RO rate [kHz]	FE ASIC	FEC	ROC
TPC	5×10^5	3.5	50	17000 SAMPA	3400	CRU
MCH	10^6	1	100	33000 SAMPA	500	CRU
ITS	25×10^9	0.5	100	25000 ASICs	184	CRU
MID	21×10^3	1	100	FEERIC	234	CRU
ZDC	22	8	100		commercial&1 ZRC	CRU
TOF	1.6×10^5	40	100			72 DRM
FIT	$160 + 64$	80	100		upgrade	DRM(TOF)
ACO	120	100	100			
TRD	1.2×10^6	1	50			CRU
EMC	18×10^3	3.7	46			
PHO	17×10^3	3.7	46			
HMP	1.6×10^5	2.5	2.5			

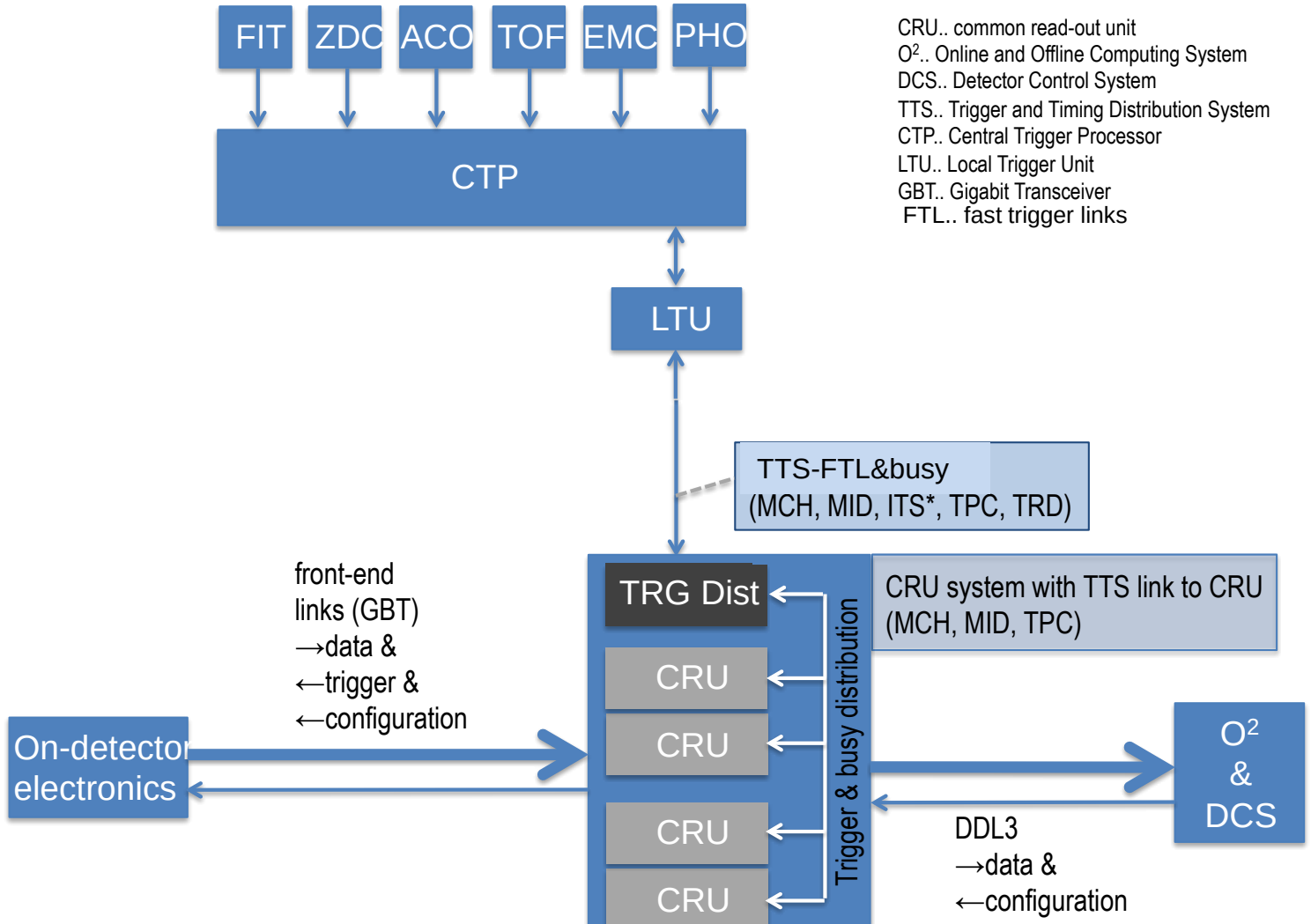
Links

Detector	DDL1	DDL2	DDL3	CRU-FE-links	TTS-FE links
	2.125 Gb/s	4.25-5.3125 Gb/s	10Gb/s	3.2 Gb/s	3.2 Gb/s
TPC			1200	6336	1764
MCH			250	500	500
ITS			*60	*184	0
MID			1	16	16
ZDC			1	1	
TOF		72			
FIT		2			
ACO	1				
TRD			36	1044	0
EMC		20			
PHO		16			
HMP	14				
Total	15	110	1555	8081	2244

Run1 and Run2 architecture

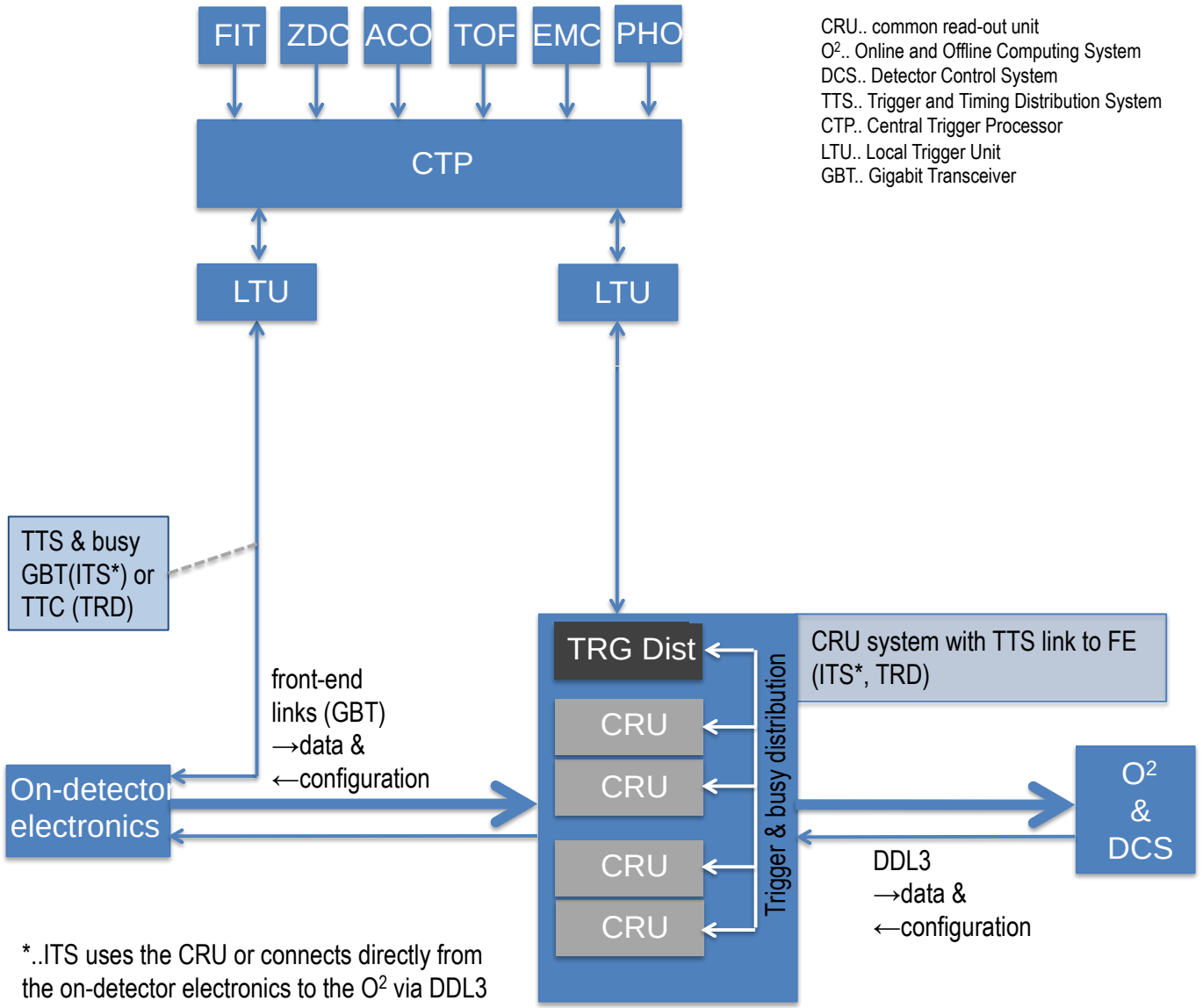


Common read-out unit - CRU & long trigger latency

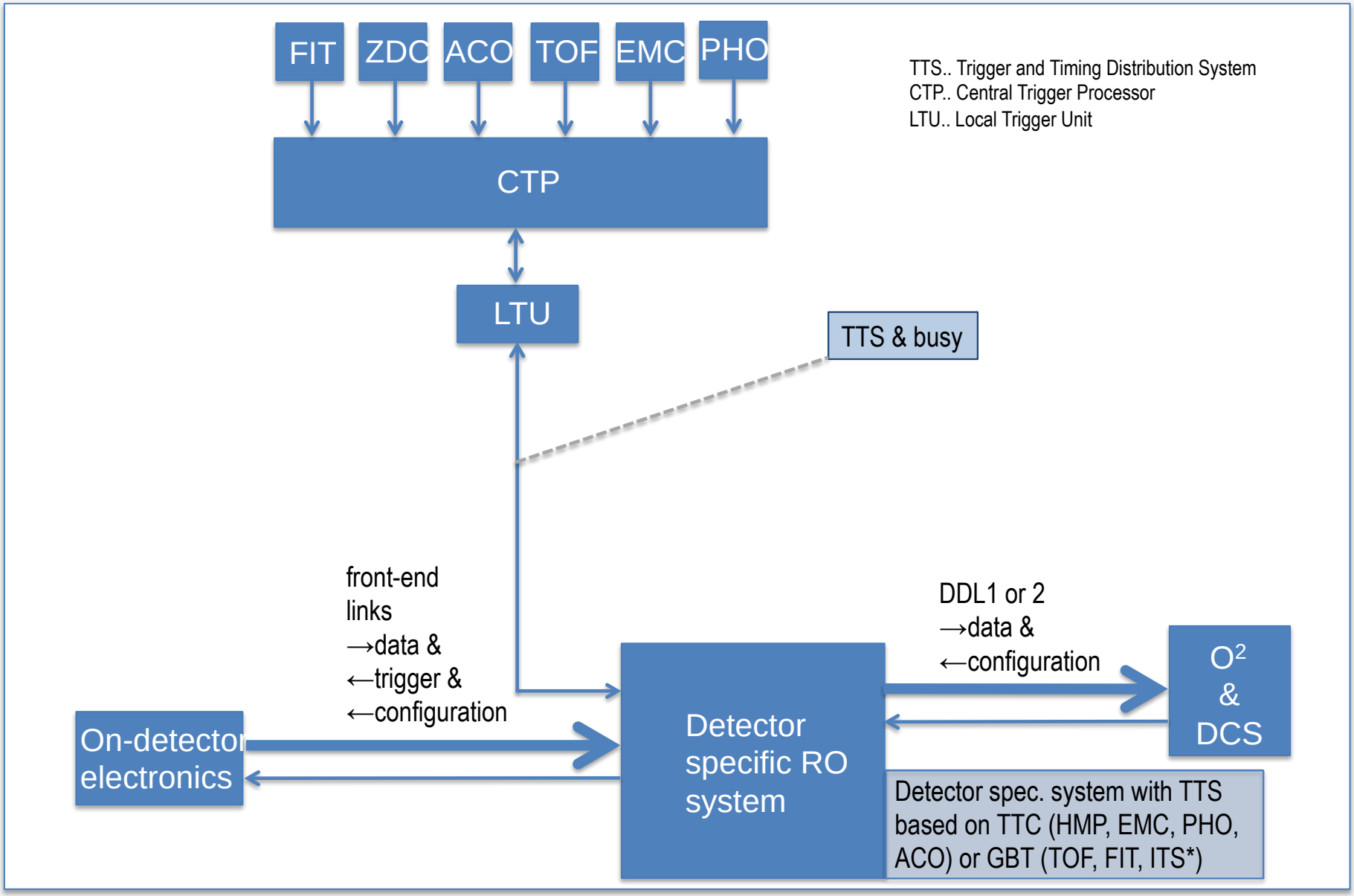


CRU.. common read-out unit
O^2.. Online and Offline Computing System
DCS.. Detector Control System
TTS.. Trigger and Timing Distribution System
CTP.. Central Trigger Processor
LTU.. Local Trigger Unit
GBT.. Gigabit Transceiver
FTL.. fast trigger links

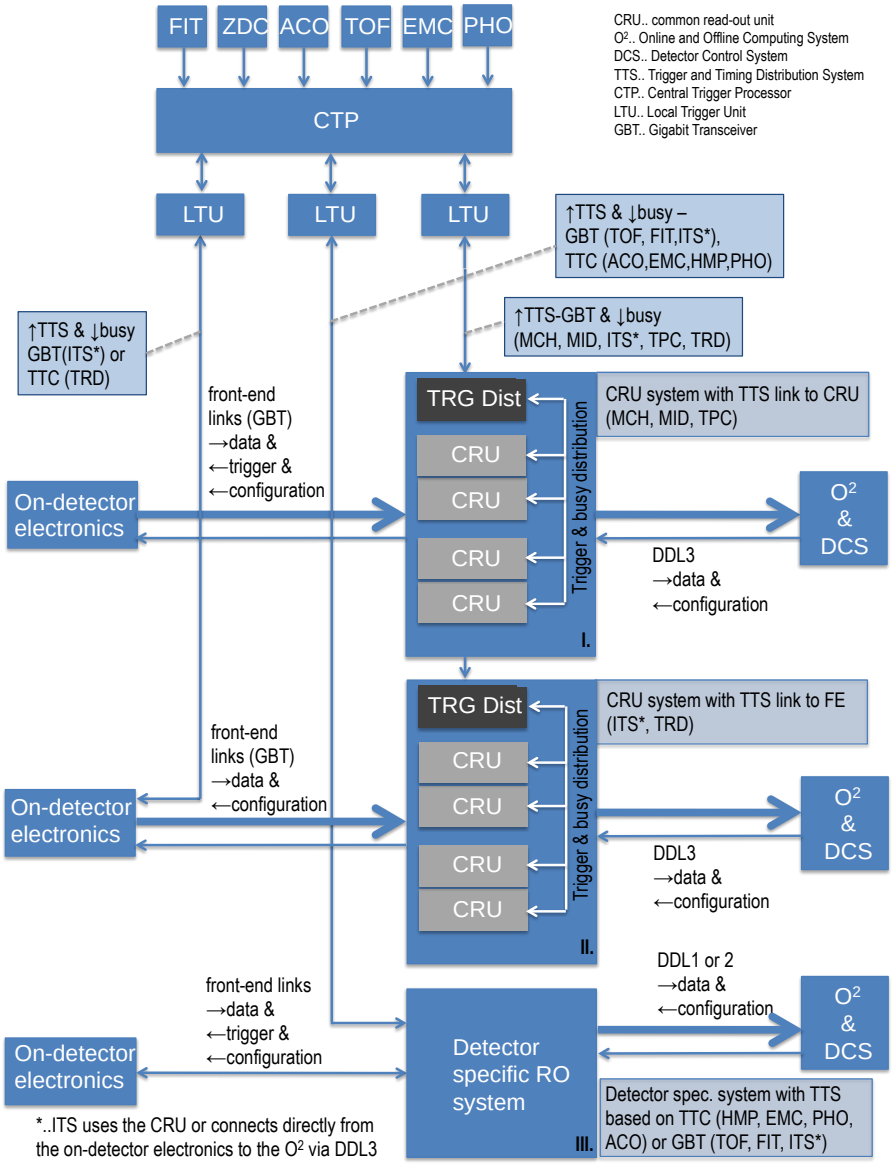
Common read-out unit - CRU & & short trigger latency



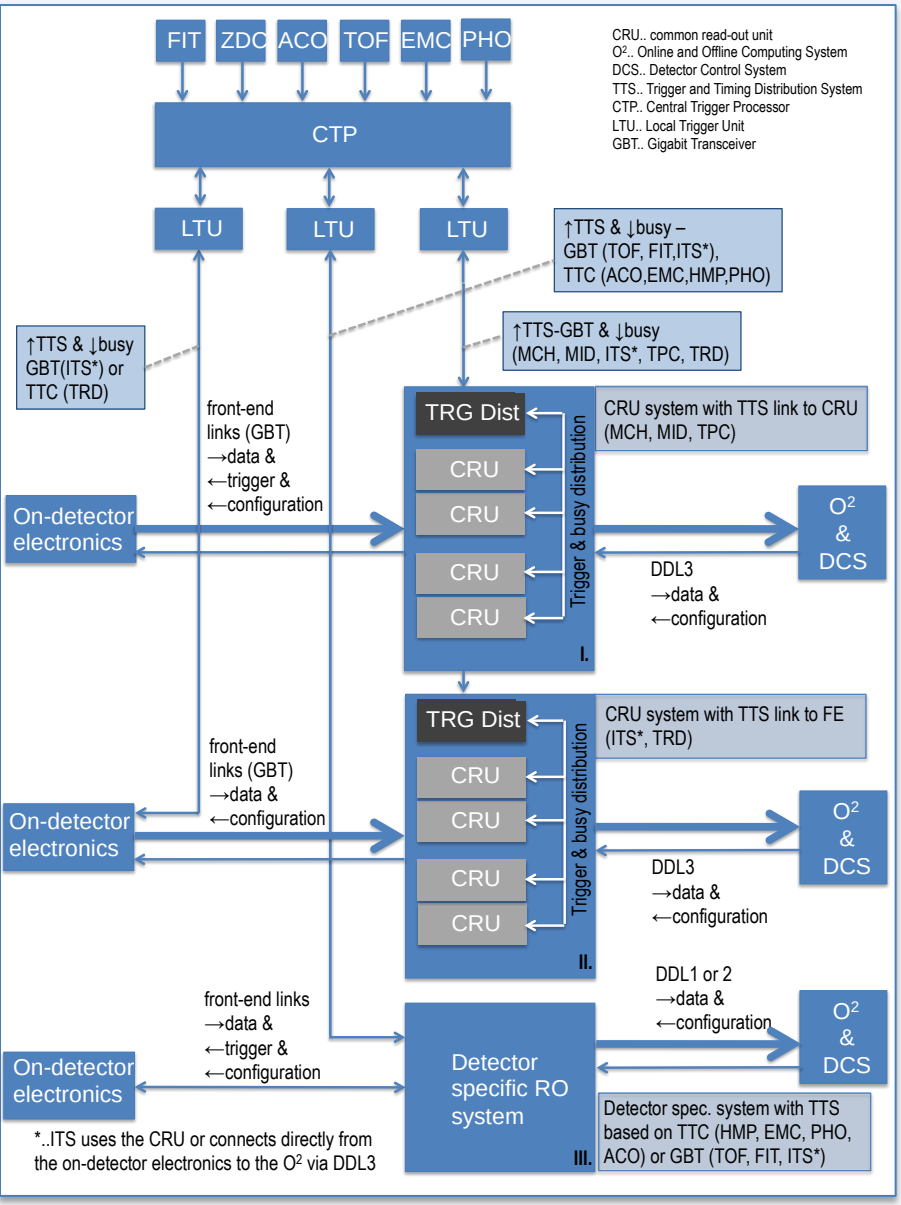
Upgrade architecture: det. spec. readout



Upgrade architecture: full read-out system



Upgrade architecture: system components



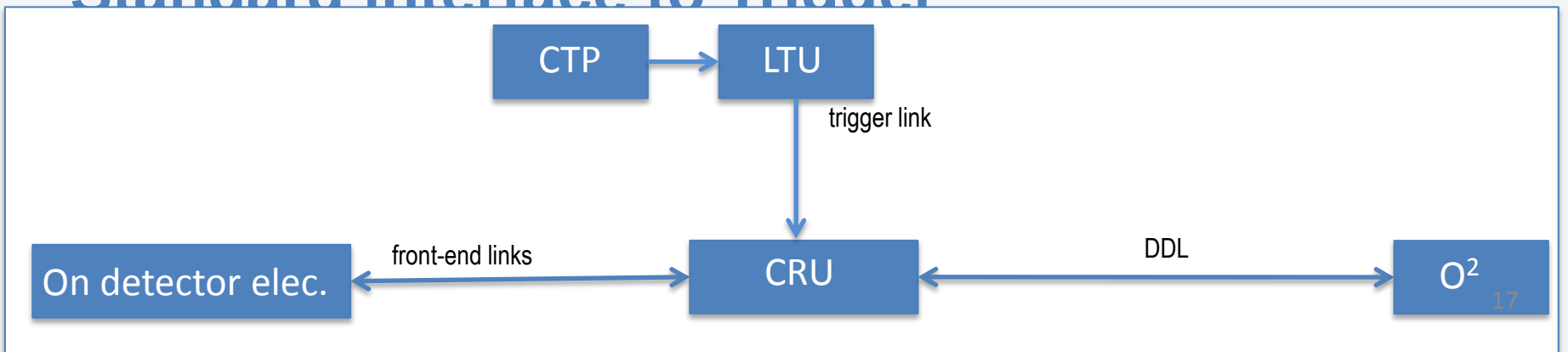
- DDL
  - common
- Off-detector read-out
  - common readout unit or custom
- Front-end links
  - versatile link (GBT) or custom
- CTP & LTU & TTS
  - fast serial trigger link (FTL) & TTC
- On-detector electronics
  - SAMPA & custom

Common components

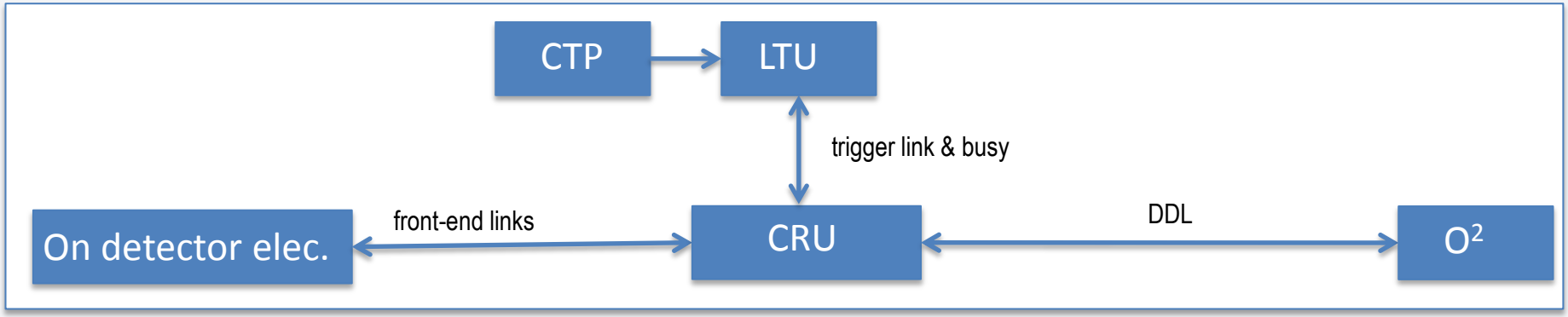
Common Readout Unit – CRU & Detector Data Link - DDL

Read-out architecture

- **Standard interface to DAQ/DCS**
  - **Detector Data Links DDL 1, 2 already developed**
    - 2.125 and 4.25/5.3125 Gb/s
  - **DDL3 based on commercial standard**
    - 10 Gb/s GbE or PCIe over cable or PCIe plug-in cards
- **Standard interface to Trigger**



Common readout unit (CRU)



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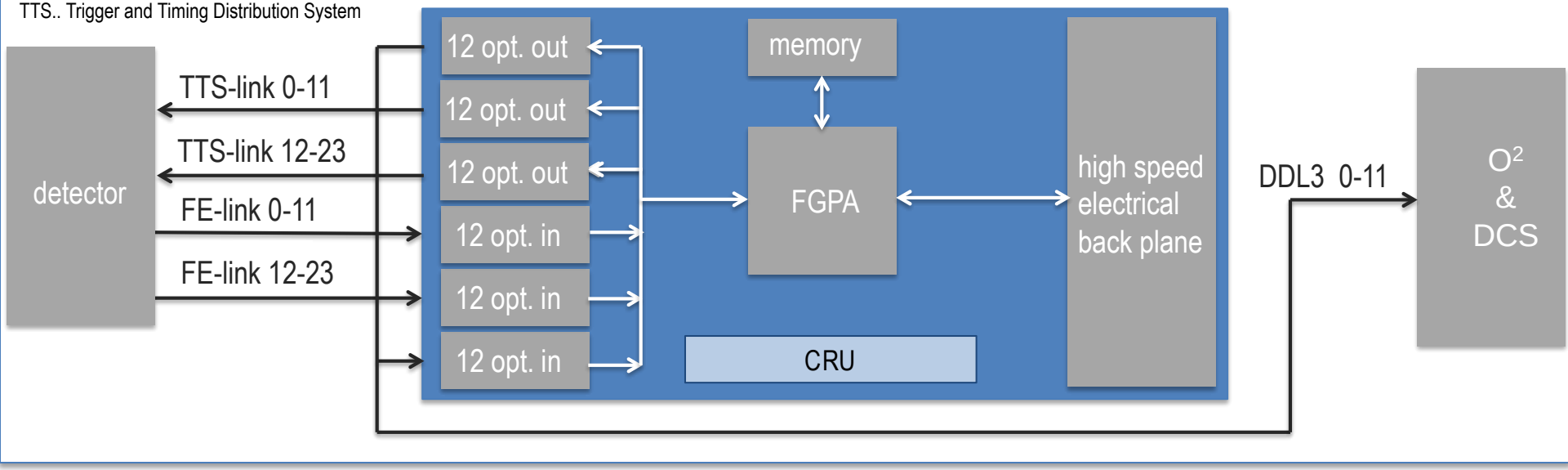
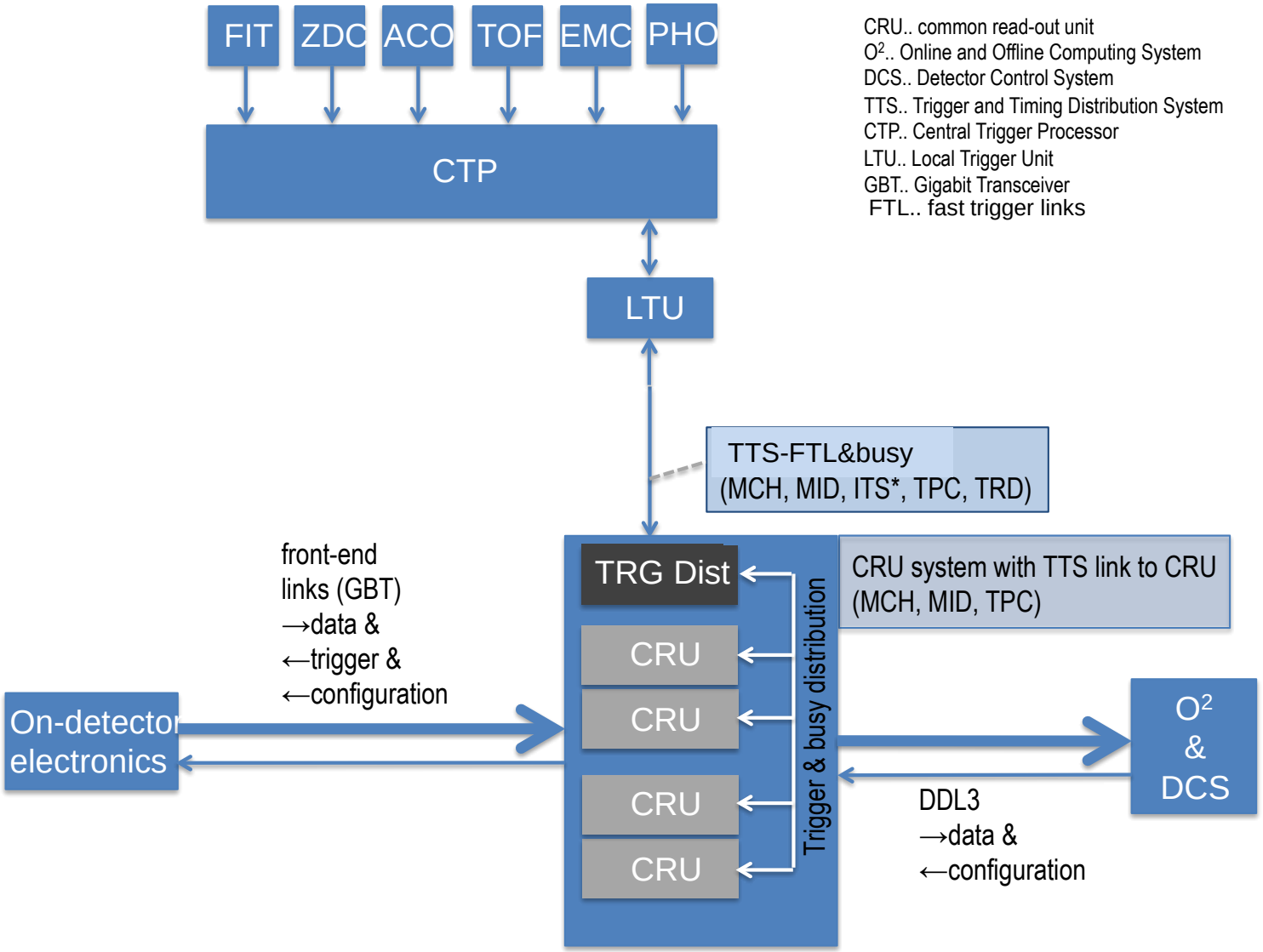
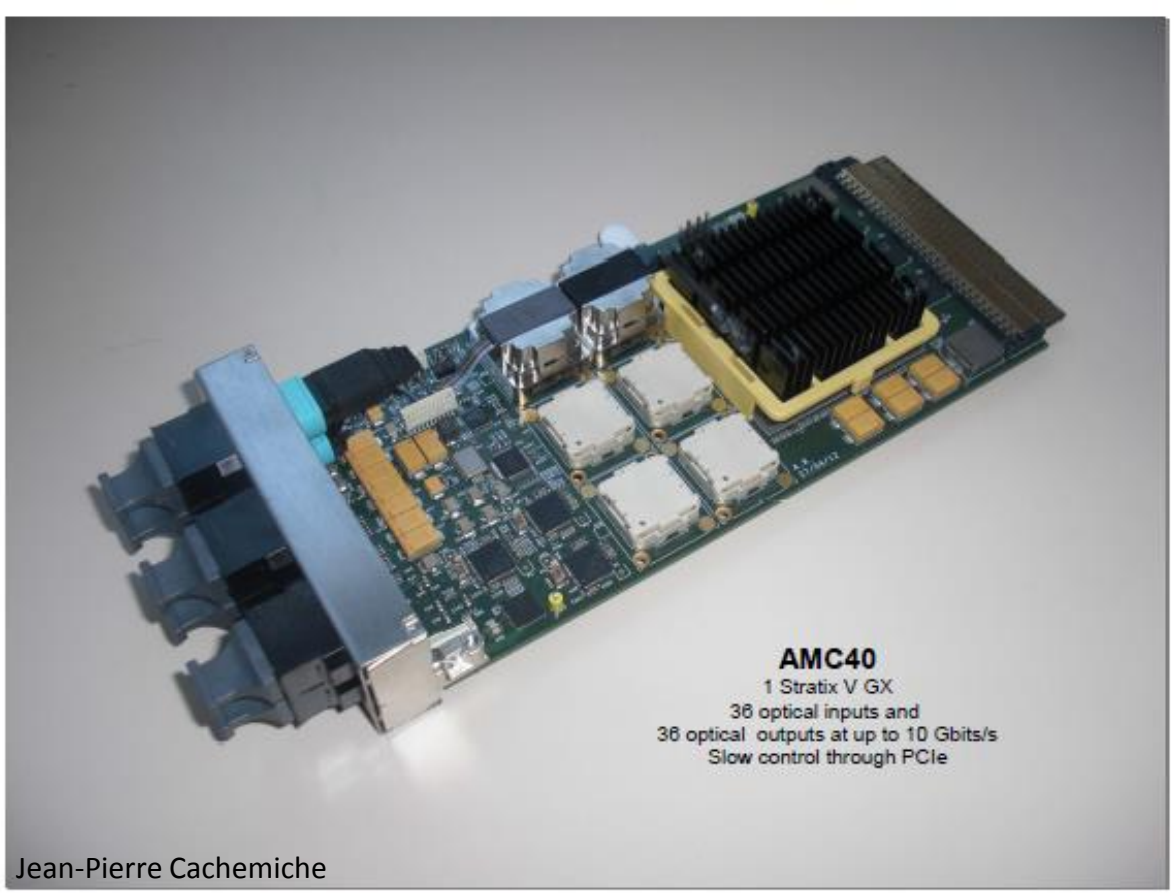


Common read-out unit - CRU



Common readout unit (CRU)

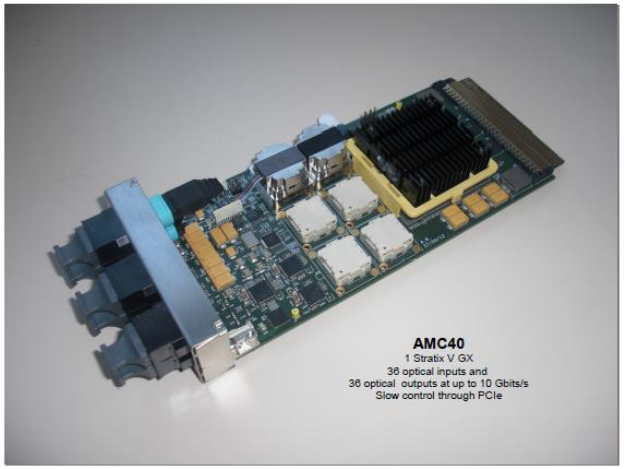
AMC40

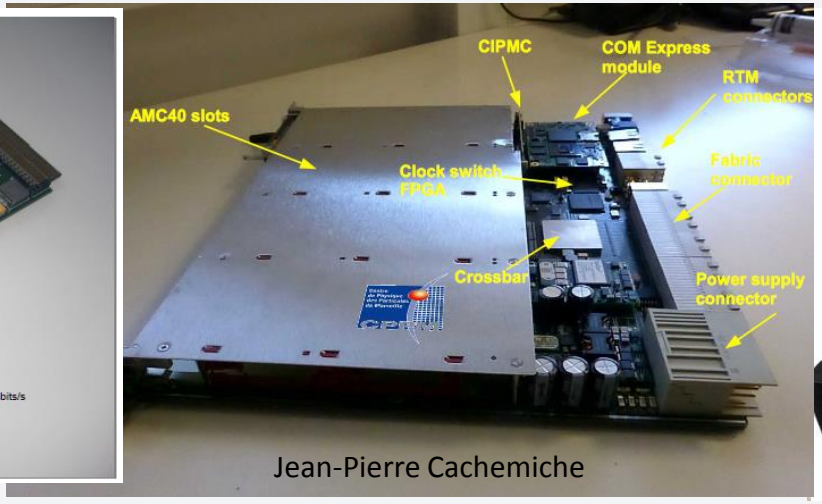


Jean-Pierre Cachemiche

- AMC40 (LHCb)
- LHCb moves to PCI40
- CRU project
  - evaluation of options
  - AMC40
  - PCI40

Common readout unit (CRU)





Jean-Pierre Cachemiche

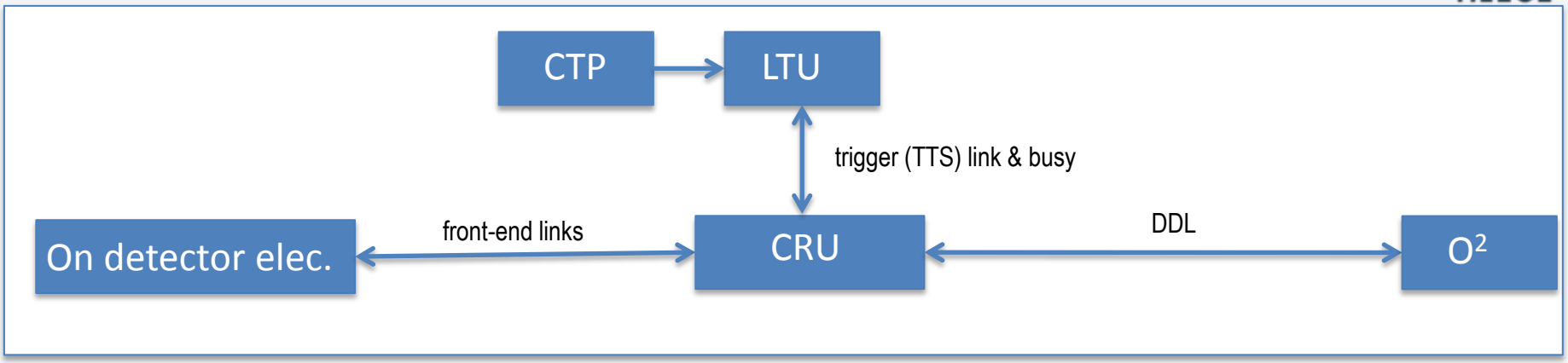
- 4 x AMC40 →
- 1 x motherboard→ 14 motherboards → 1 ATCA crate
- Trigger and timing distribution is via back plane

Common components

Front-end (FE) links &

Trigger and Timing Distribution System (TTS) Links

Common components



Front-end (FE) links &

Trigger and Timing Distribution System (TTS) Links

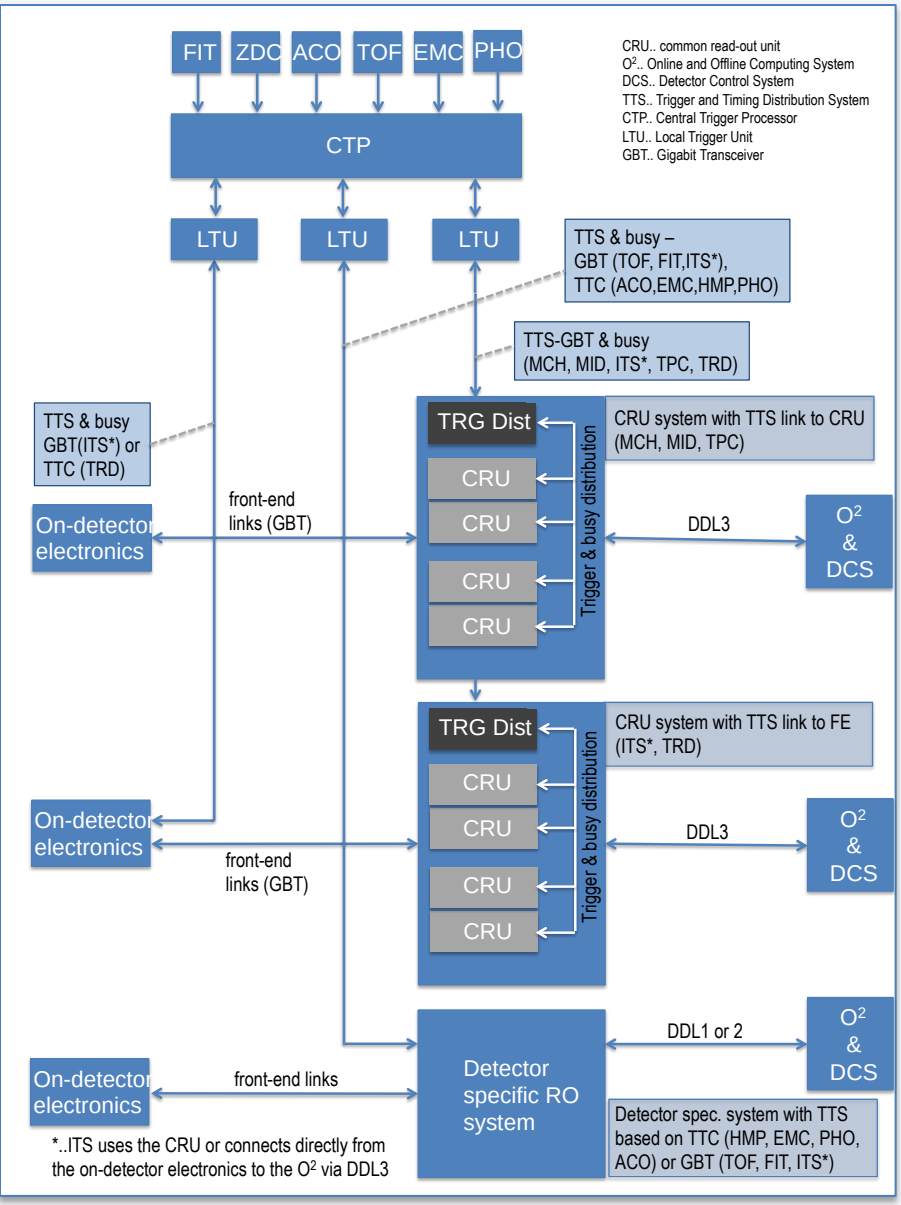
TTS links (ATCA crate)

Detector	TTS links	type	Position trigger interface
TPC	7	FTL	CR
MCH	1	FTL	CR
ITS	184	FTL	Cav
MID	1 & 1	FTL	CR/Cav
ZDC	1 & 1	FTL	CR & Cav
TOF	72	FTL	Cav
FIT	1	FTL	CTP area
TRD	1 & 1	FTL & TTC	CR/Cav
EMC	1	TTC	Cav
PHO	1	TTC	Cav
HMP	1	TTC	Cav
ACO	1	TTC	Cav

Common components

Central Trigger Processor (CTP) & Local Trigger Processor (LTU)

CTP & LTU



CTP & LTU: based on high performance FPGA processor

Logic combinations fully programmable

Use of AMC40 is evaluated

Summary

- **Interface:**
  - front-end links (GBT)
  - DDL3 → online system
  - Central trigger processor
- **Is common read-out unit**
- **Base-line is ATCA based AMC40 (LHCb)**