LHCb Readout implementation

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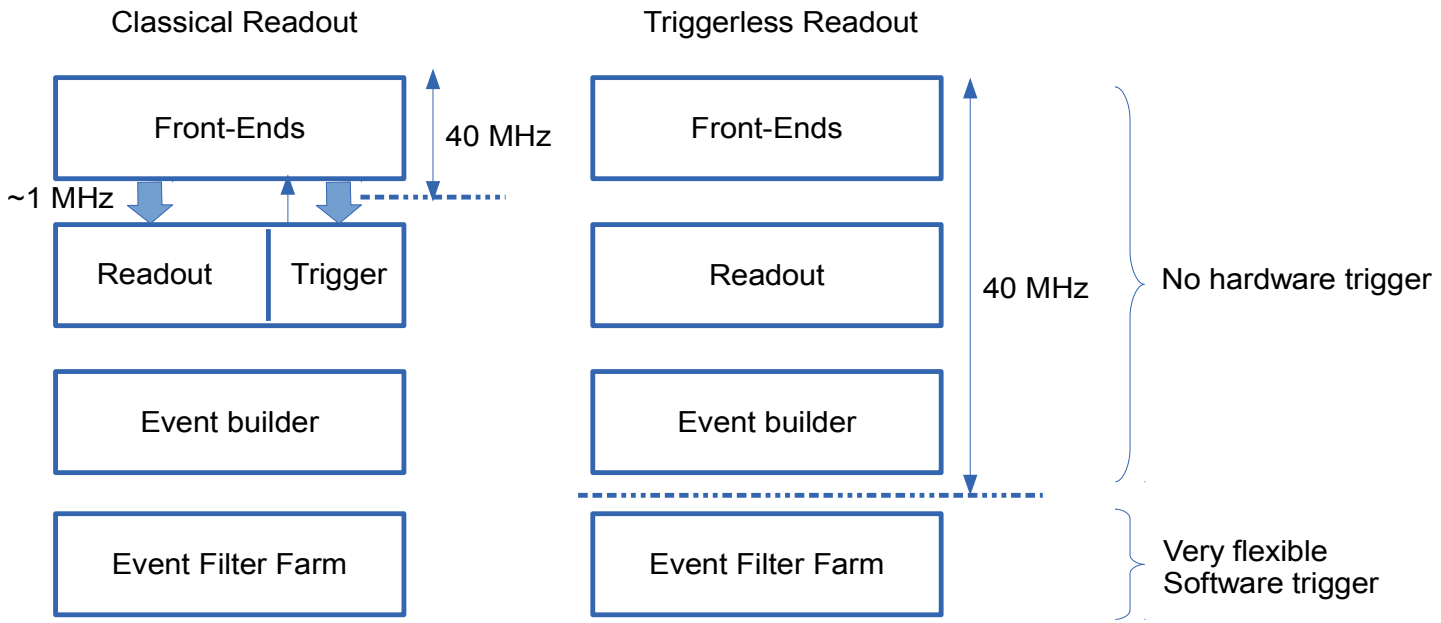
Outline

- General principle
- Initial architecture : ATCA based
  - AMC40
  - ATCA40
  - Flavours
  - MiniDAQ
- Reasons for changing
- New architecture
  - PCIe40
- Schedule

General principle

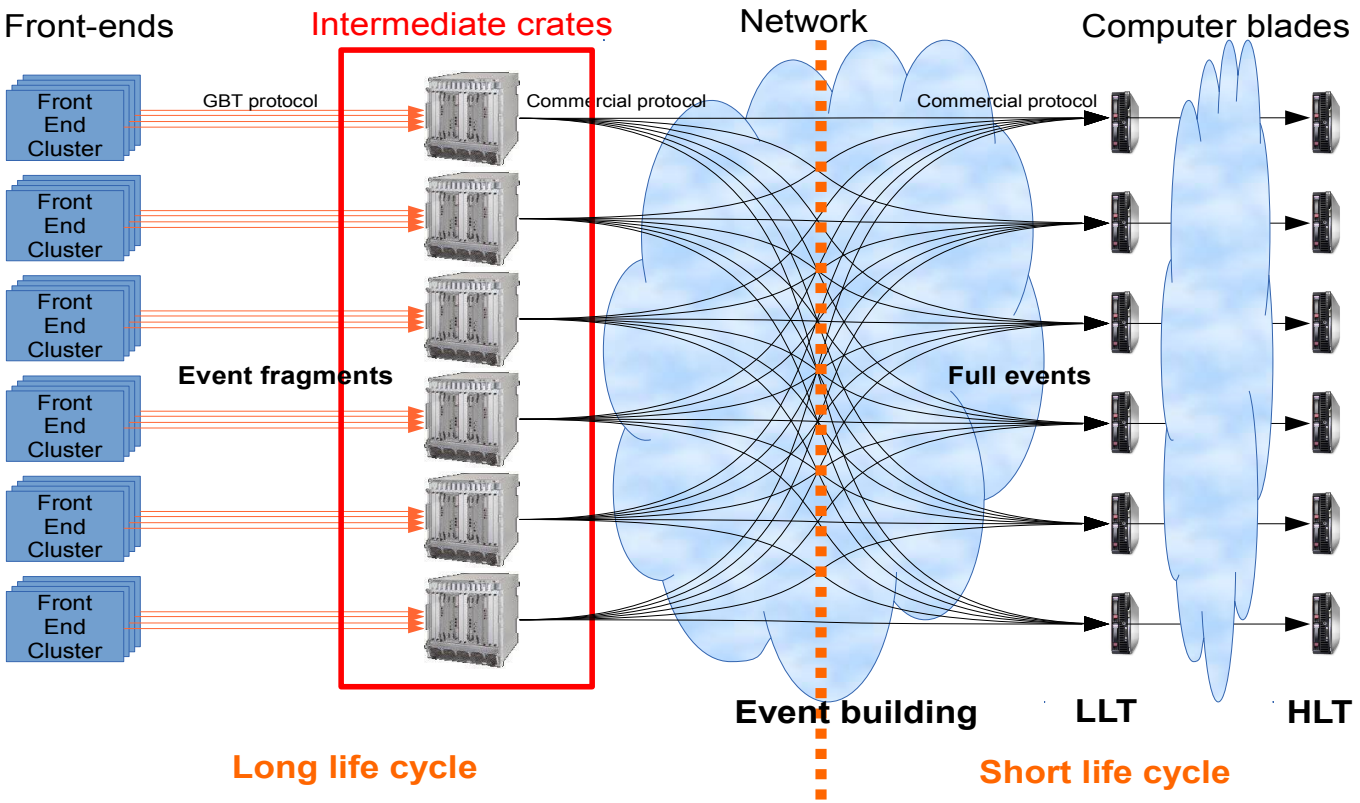
Trigger-less system

- No hardware trigger in the readout chain
- All events routed to the farm at 40 MHz
- Event building assured by readout boards + network switches



Initial implementation

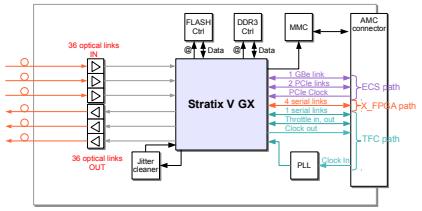
Back-end in intermediate crates



TELL40

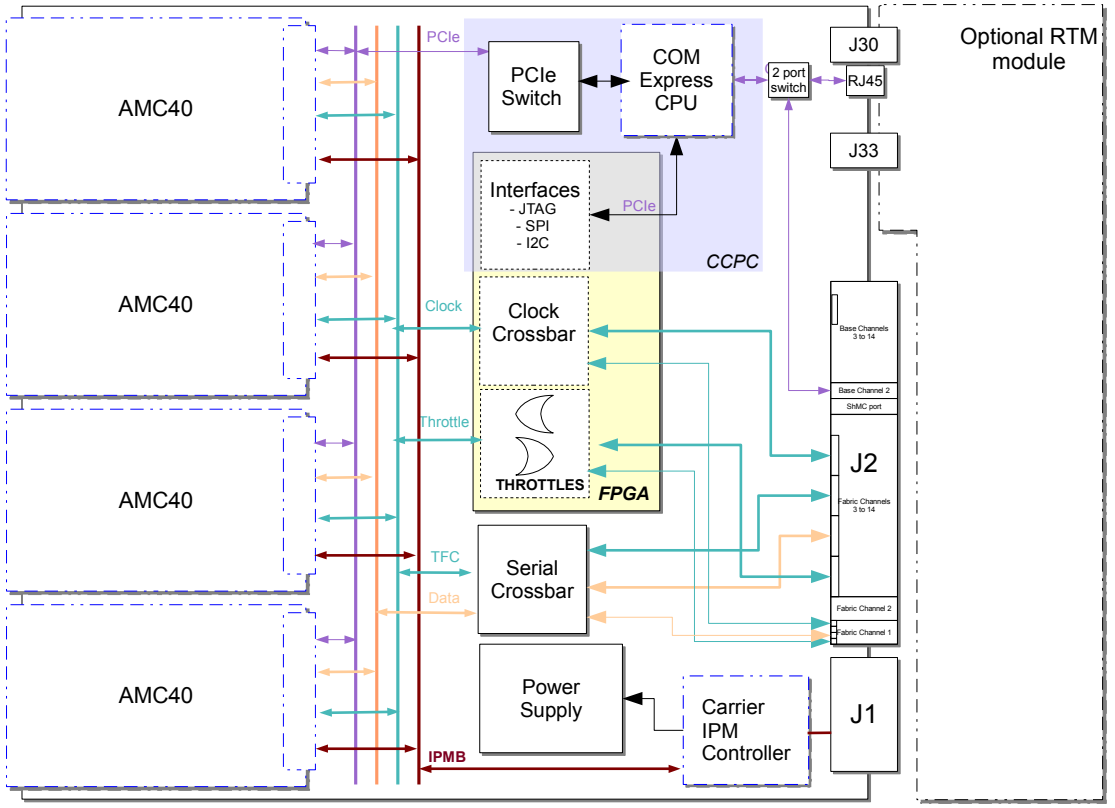
Implementation in ATCA format

ATCA carrier + 4 AMC boards



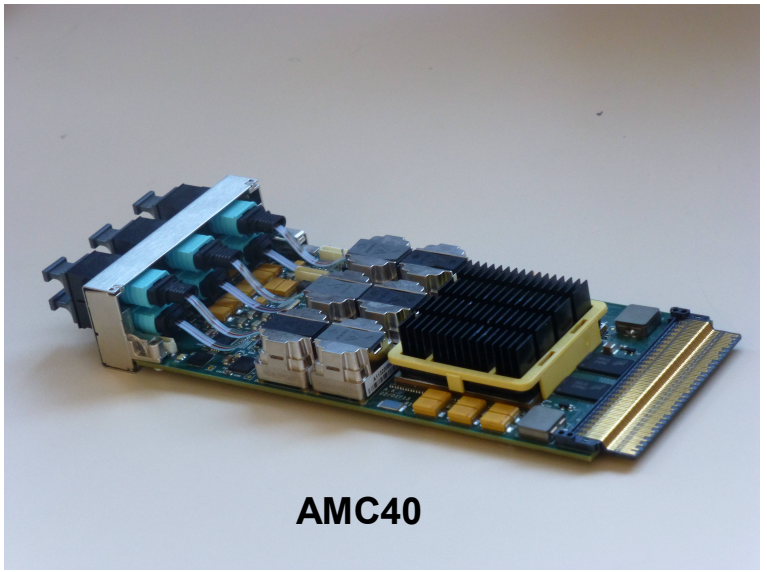
AMC40

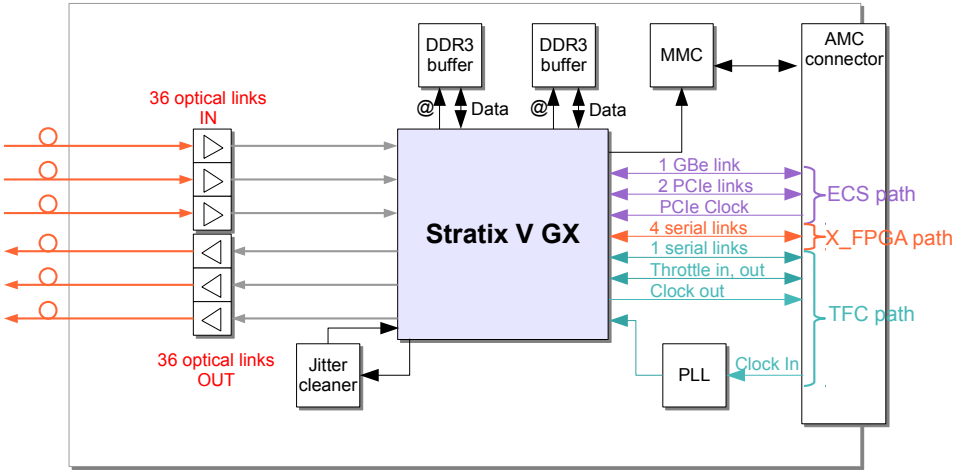
144 bidir optical links at up to 10 Gbits/s



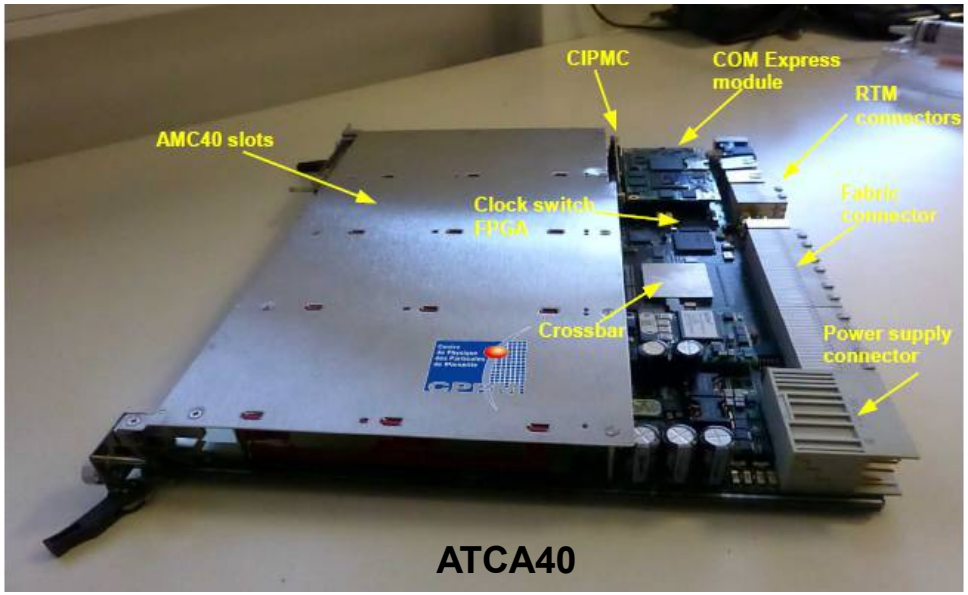
ATCA40

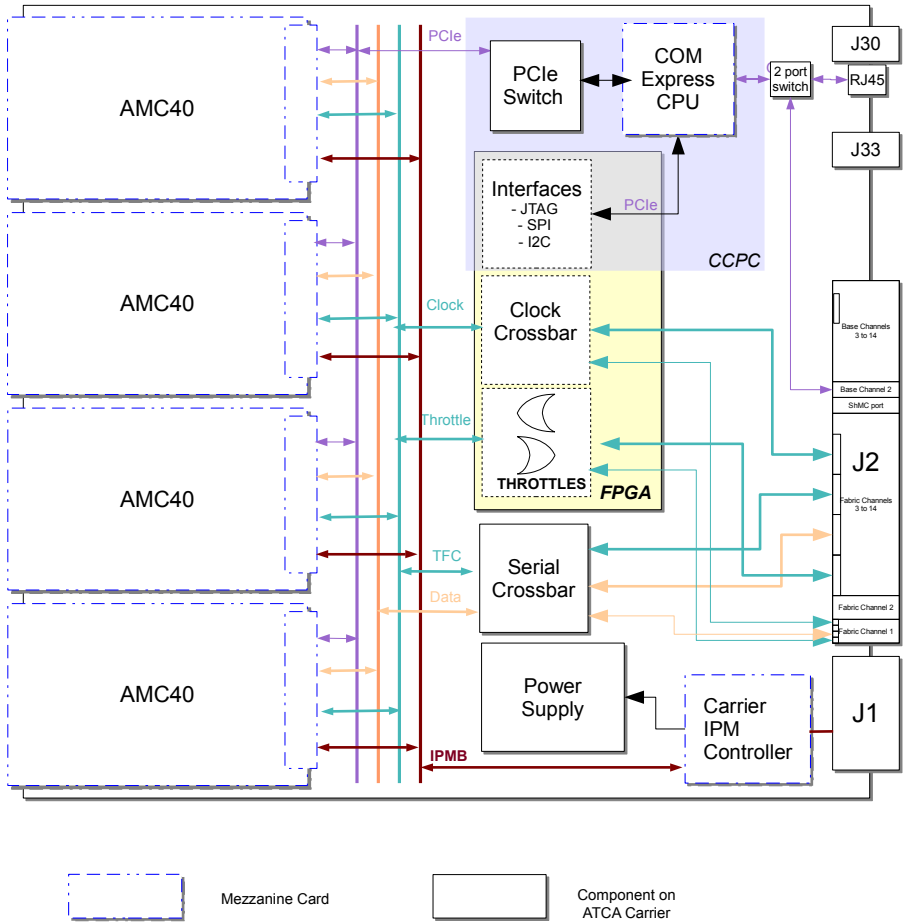
AMC40


AMC40

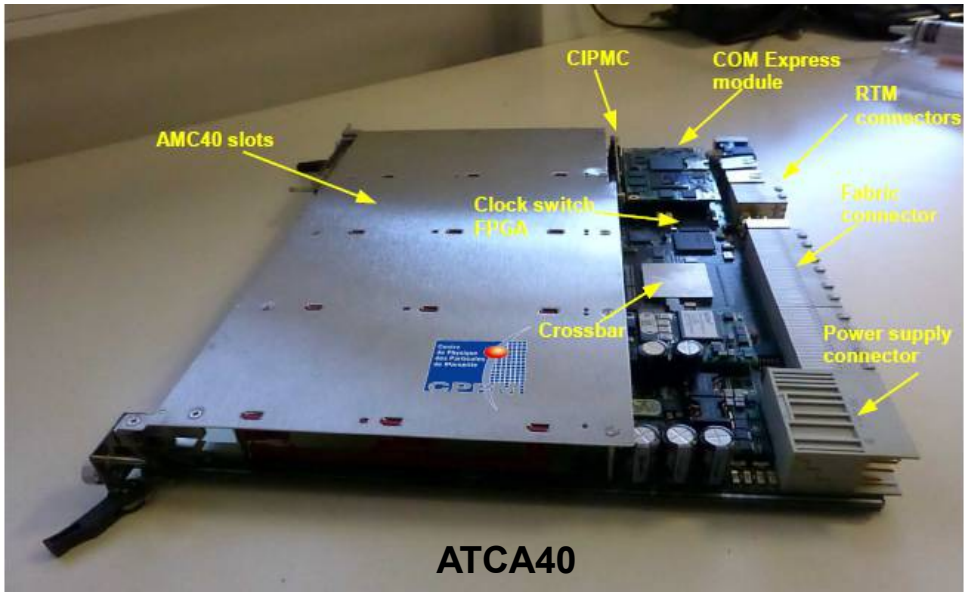

DDR3 buffer
DDR3 buffer
MMC
AMC connector
36 optical links IN
@ Data
@ Data
1 GBe link
2 PCIe links
PCIe Clock
4 serial links
1 serial links
Throttle in, out
Clock out
ECS path
X_FPGA path
TFC path
Stratix V GX
36 optical links OUT
Jitter cleaner
PLL
Clock In

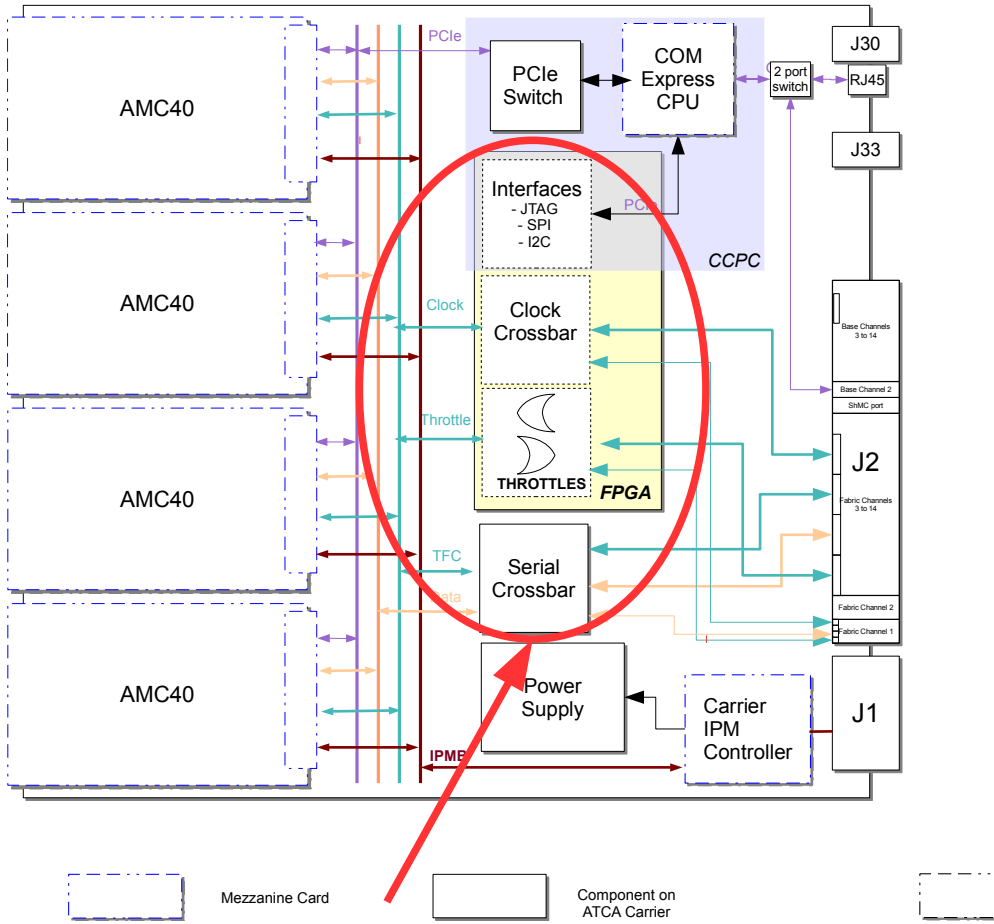
ATCA40


AMC40 slots
CIPMC
COM Express module
RTM connectors
Clock switch FPGA
Fabric connector
Crossbar
Power supply connector
ATCA40


AMC40
AMC40
AMC40
AMC40
PCIe
PCIe Switch
COM Express CPU
2 port switch
J30
RJ45
J33
Interfaces
- JTAG
- SPI
- I2C
PCIe
CCPC
Clock
Clock Crossbar
Throttle
THROTTLES
FPGA
J2
TFC
Data
Serial Crossbar
Power Supply
Carrier IPM Controller
J1
IPMB
Mezzanine Card
Component on ATCA Carrier

ATCA40



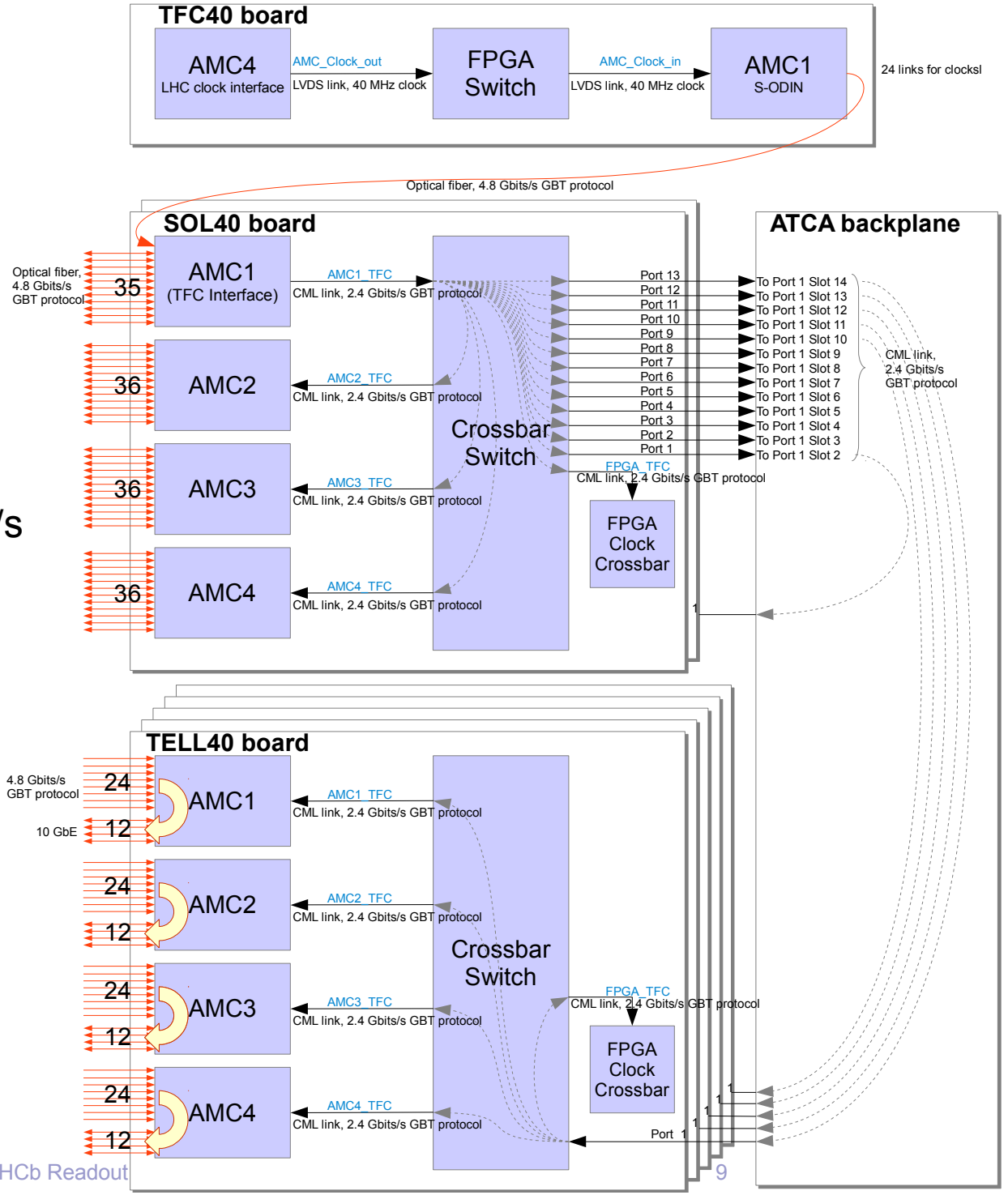


Programmable communication matrix

Flavours

From TFC40 to FE and TELL40s

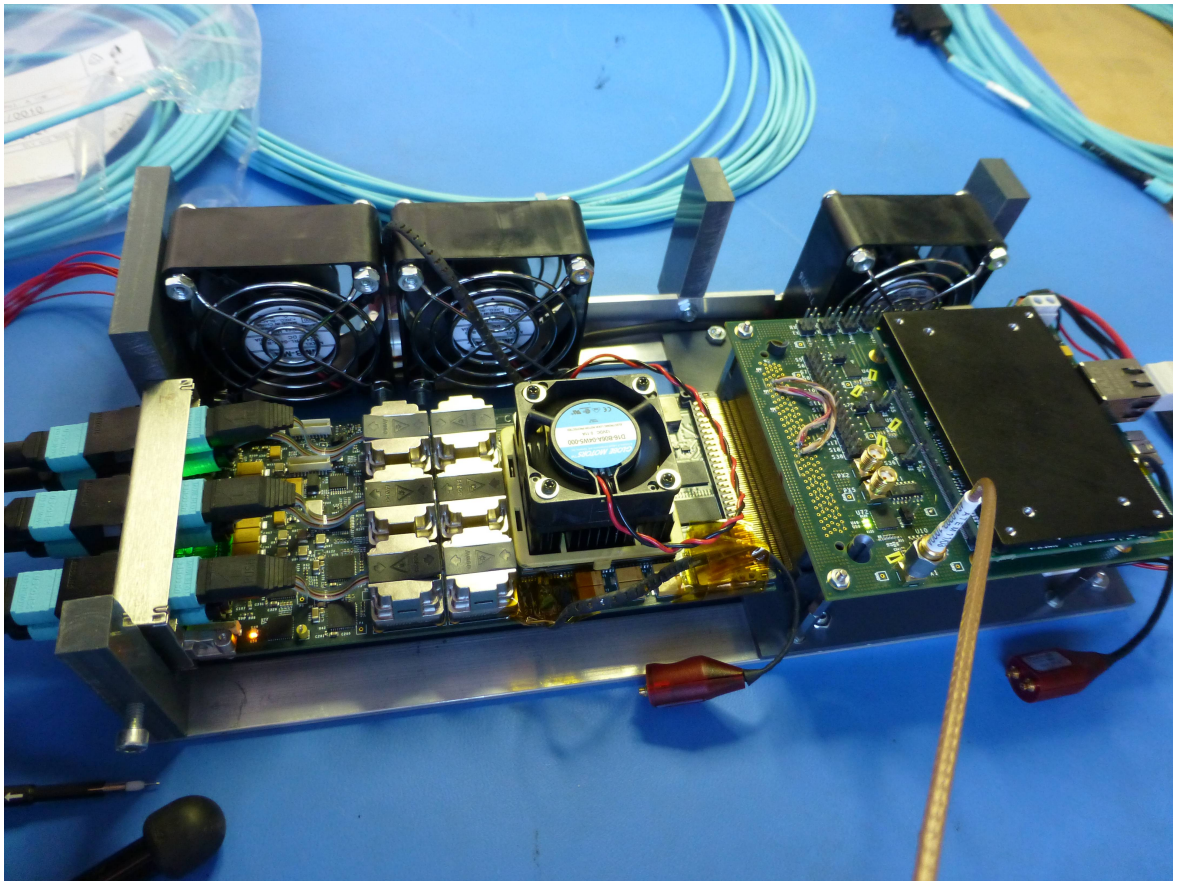
- Clocks and triggers broadcast over 2.4 Gbits/s serial lines
- Relies on flexibility of FPGA and Crossbar switches



The miniDAQ

Light setup for controlling Front Ends prototypes

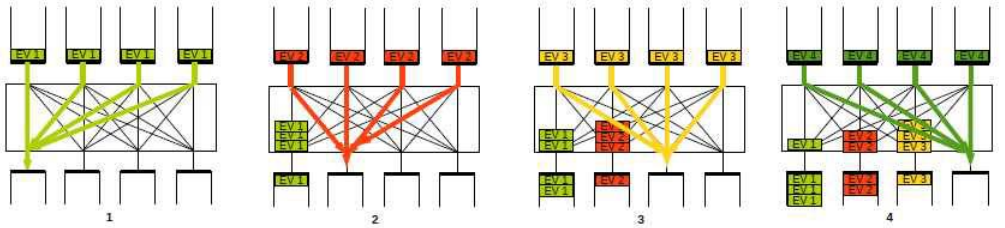
- Provides :
  - Power supply,
  - Clocks
  - Cooling
  - Slow control



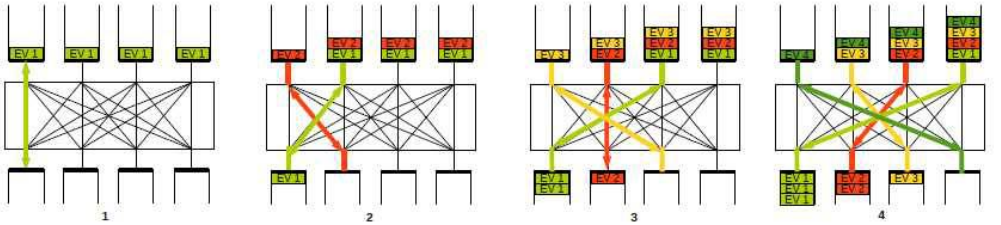
Reasons for changing

Bufferization issue

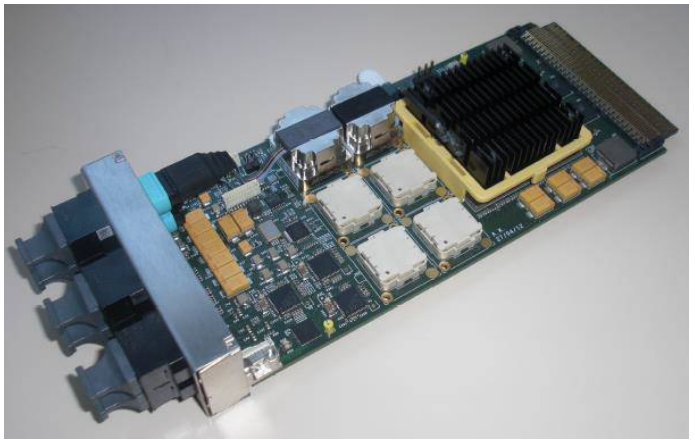
Push mode

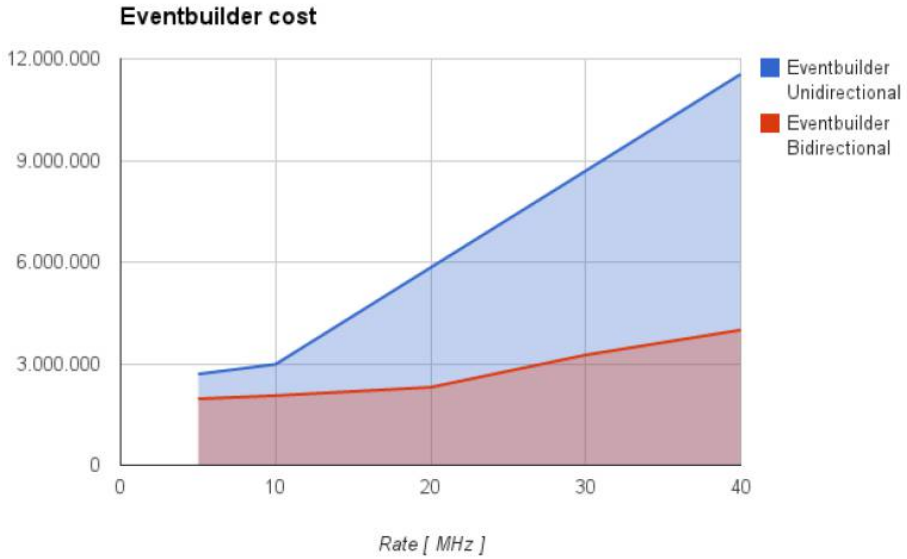


Pull mode



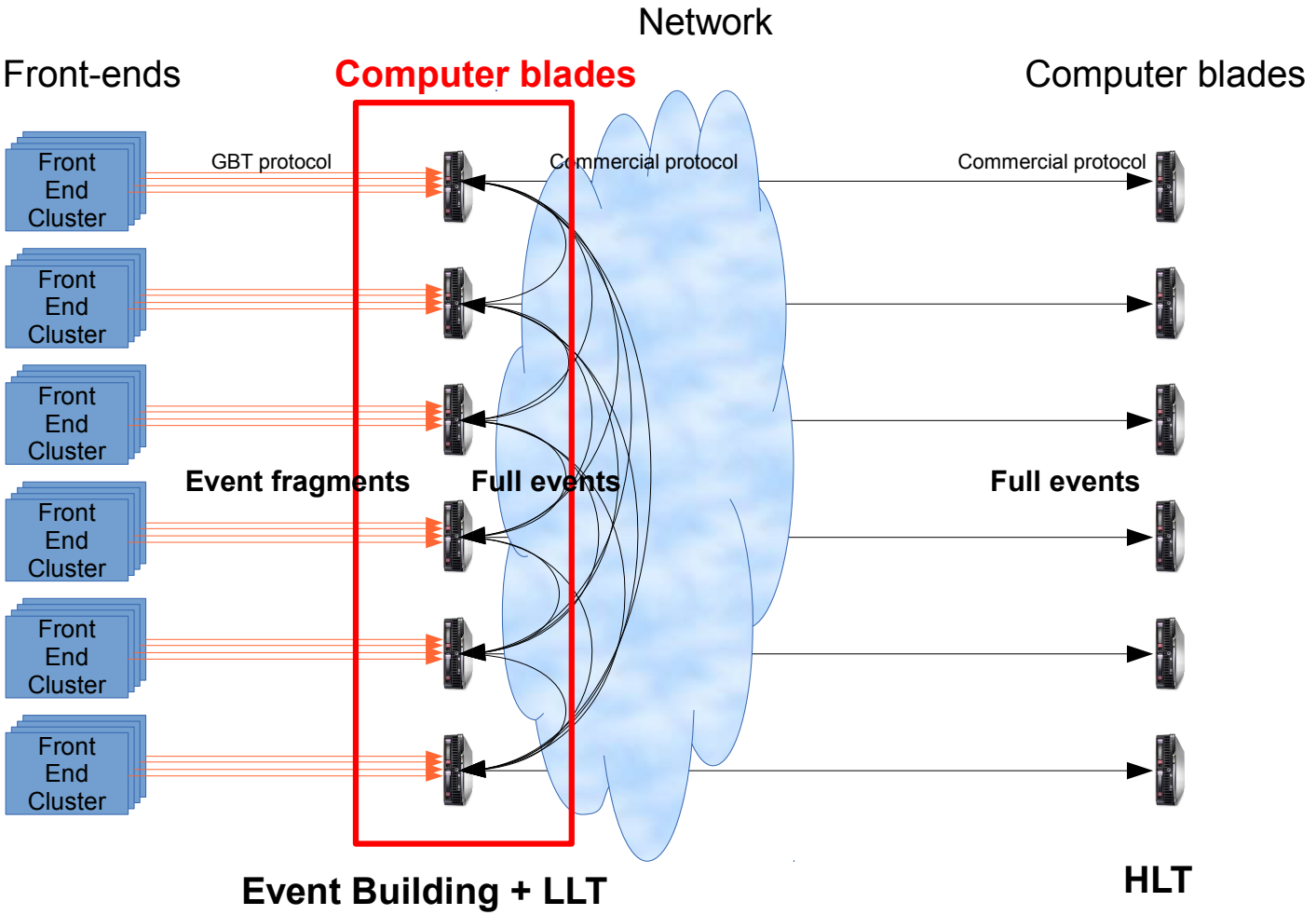
- Pull : memory on already very dense back-end boards
- Push : requires expensive switches with memory inside



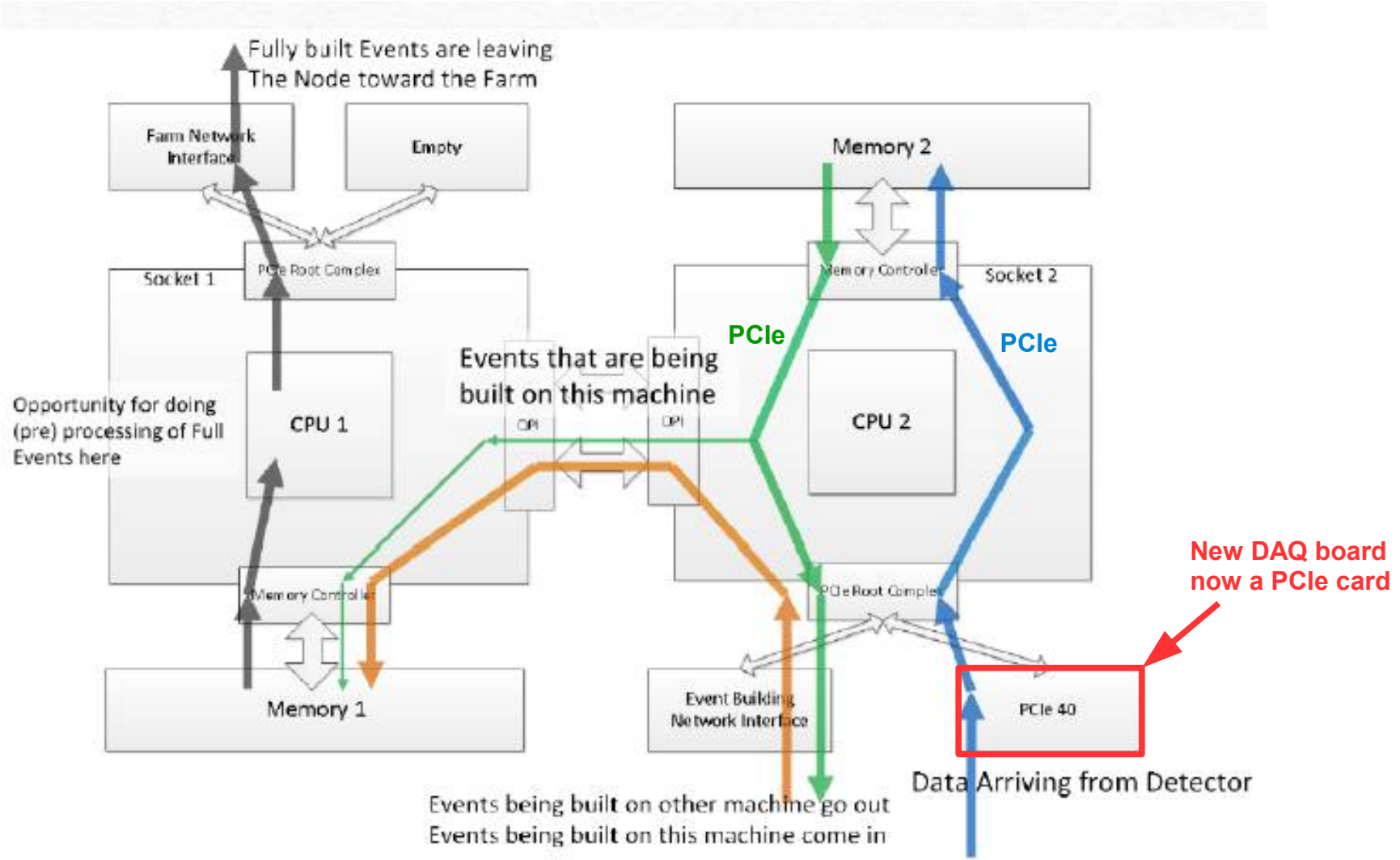


New implementation

Full event building in the farm



Data path


Fully built Events are leaving
The Node toward the Farm
Farm Network Interface
Empty
Memory 2
Socket 1
PCIe Root Complex
Memory Controler
Socket 2
PCIe
PCIe
Events that are being built on this machine
Opportunity for doing (pre) processing of Full Events here
CPU 1
CPU 2
Memory Controller
PCIe Root Complex
New DAQ board now a PCIe card
Memory 1
Event Building Network Interface
PCIe 40
Data Arriving from Detector
Events being built on other machine go out
Events being built on this machine come in

PCIe40 board

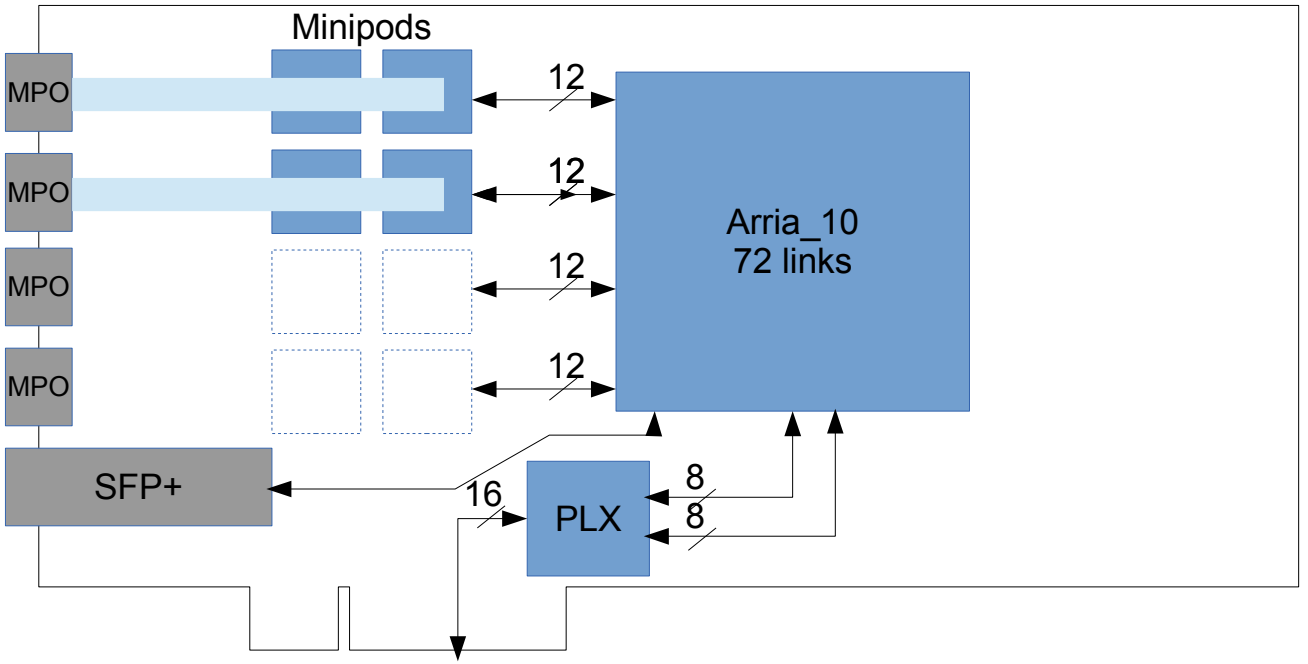
Nominal configuration:

1 bidir link for TFC

24 GBT inputs → limited by PCIe output bandwidth

- PCIe GEN3 x16 = 110 Gbits/s
- 24 GBT wide bus = 107 Gbits/s

Up to 48 bidir links available on board for low luminosity sub detectors → decrease the costs



FPGA

FPGA 10AX115S4F45I3SGES from Altera

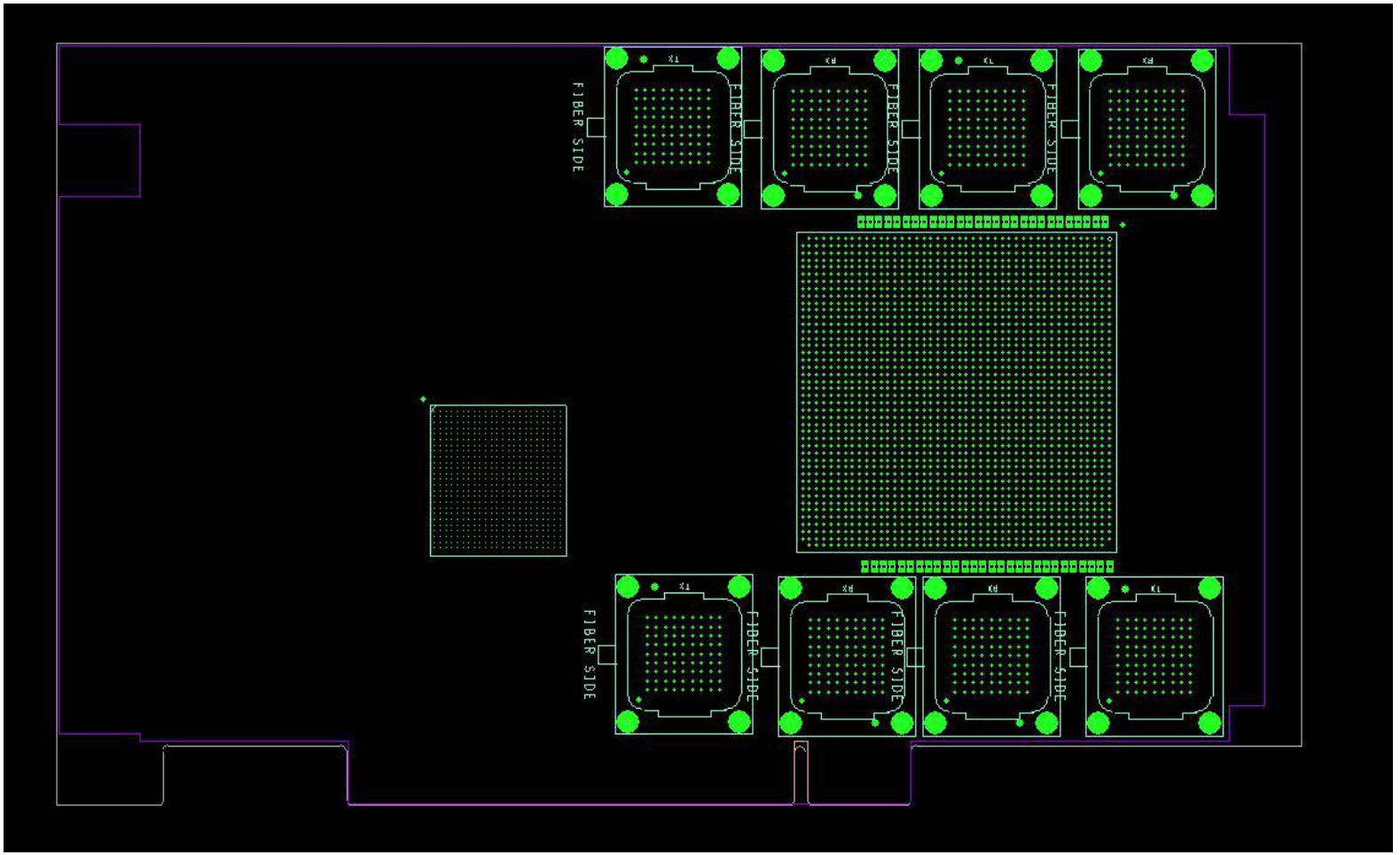
- Features

Resource		Product Line								
		GX 160	GX 220	GX 270	GX 320	GX 480	GX 570	GX 660	GX 900	GX 1150
Logic Elements (LE) (K)		160	220	270	320	480	570	660	900	1,150
ALM		61,510	83,730	101,620	118,730	181,790	217,080	250,540	339,620	427,200
Register		246,040	334,920	406,480	474,920	727,160	868,320	1,002,160	1,358,480	1,708,800
Memory (Kb)	M20K	8,800	11,760	15,000	17,820	28,760	36,000	42,660	48,460	54,260
	MLAB	1,050	1,833	2,451	2,864	4,404	5,096	5,788	9,386	12,984
Variable-precision DSP Block		156	191	830	985	1,368	1,523	1,678	1,518	1,518
18 x 19 Multiplier		312	382	1,660	1,970	2,736	3,046	3,356	3,036	3,036
PLL	Fractional Synthesis	6	6	8	8	12	16	16	32	32
	I/O	6	6	8	8	12	16	16	16	16

Product Line	KF40 (40 mm × 40 mm, 1517-pin FBGA)		NF40 (40 mm × 40 mm, 1517-pin FBGA)		RF40 (40 mm × 40 mm, 1517-pin FBGA)		NF45 (45 mm × 45 mm) 1932-pin FBGA)		SF45 (45 mm × 45 mm) 1932-pin FBGA)		UF45 (45 mm × 45 mm) 1932-pin FBGA)	
	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR
GX 900	—	—	600	48	342	66	768	48	624	72	480	96
GX 1150	—	—	600	48	342	66	768	48	624	72	480	96

Implementation

Design on-going



Schedule and manpower

Nominal scenario	2014		2015		2016		2017		2018		2019	
	S1	*S2*	*S1*	*S2*	*S1*	*S2*	*S1*	*S2*	*S1*	*S2*	*S1*	*S2*
Duplication miniDAQ												
PCIe40 or AMC40_V3 design												
Preseries production												
Series production												
LLT porting												
Commissionning												
LS2												

	2014	2015	2016	2017	2018	2019
Readout card						
Project coordination	0,6	0,6	0,6	0,6	0,6	0,6
Design, pre-series, production	3,5	3,5	3	1,5	0,5	
LLT						
Coordination	0,5	0,5	0,5	0,5	0,5	0,5
Muon Firmware development			0,5	2	1,5	
Integration						
Commissionning					1,5	3

Conclusion

Many advantages with the new architecture:

- Independance of network interface
- Large memory buffer
- More room in the FPGA (Hard IP)
- Powerful slow control
- Cheaper solution

Few points to closely study

- PC life cycle vs experience duration
- Cooling