Upgrade of the ALICE Inner Tracking System

L. Musa - CERN

PH Detector Seminar
CERN, 17 April, 2015

Upgrade of the ALICE Inner Tracking System

OUTLINE

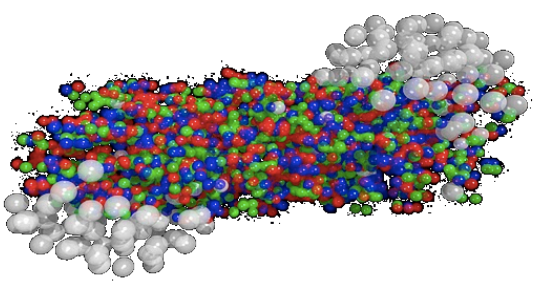
- ALICE upgrade motivations and strategy
- ALICE current set-up and Inner Tracking System
- ITS upgrade design objectives
- ITS upgrade layout and main components
- Detector simulated performance: some examples

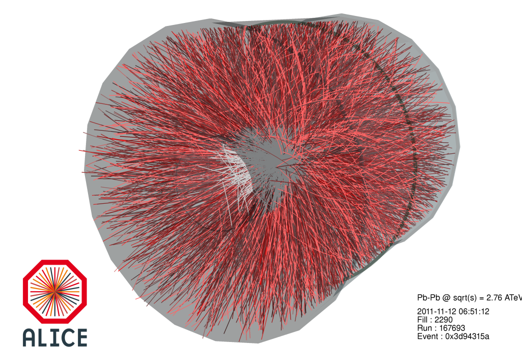
ALICE: study QGP properties

ALICE is designed to study the physics of strongly interacting matter at extreme conditions of energy density and temperature, and in particular the properties of the Quark Gluon Plasma (QGP), using A-A, p-A and pp collisions

Prior to LHC Heavy Ion programme, nature of QGP – "a nearly perfect liquid" – emerged from experiments at CERN SPS and BNL RHIC

ALICE confirms basic picture: observation of hot hadronic matter at unprecedented values of temperatures, densities and volumes ….





… and exceeding the precision and kinematic reach of all significant probes of the QGP measured in the past decades

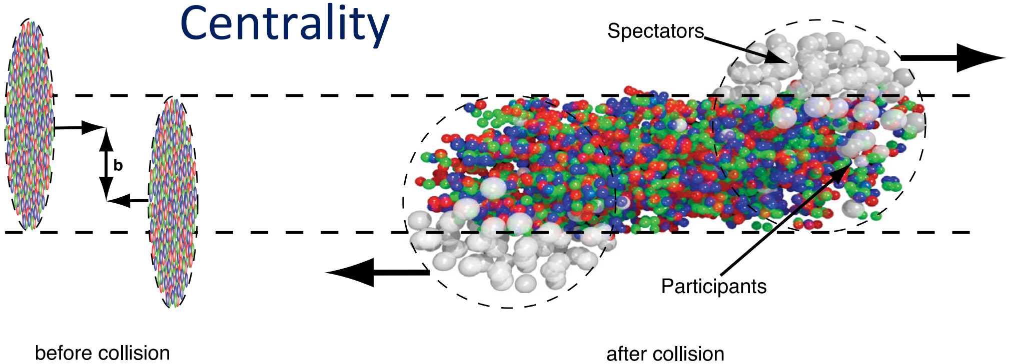
➡ Excellent capabilities to measure high-energy nuclear collisions at LHC

ALICE: study QGP properties

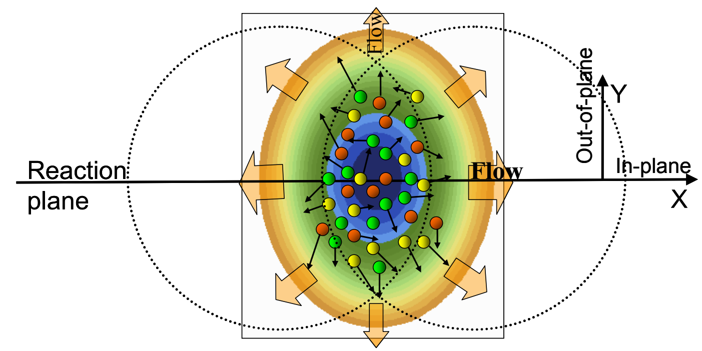
Progress on the characterization of QGP properties requires

- precision measurements of rare probes
- over a large kinematic range (from high to very low transverse momenta)
- and as function of multi-differential observables: centrality, reaction plane, …

Centrality



Reaction plane



One example:

precision measurements of spectra, correlations and flow of heavy flavour hadrons and quarkonia at low transverse momenta (not possible to trigger!!)

ALICE Upgrade Strategy

This requires statistics (luminosity) and precision measurements

Target for **upgrade programme** (Run3 + Run4)

- Pb-Pb recorded luminosity $\geq 10\ nb^{-1}$ ➡ 8×10^{10} events

I. Upgrade detectors, readout systems and online systems to

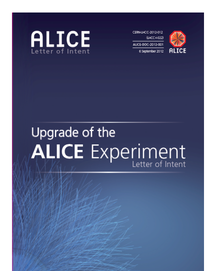
- read out all Pb-Pb interactions at a maximum rate of 50kHz (i.e. $L = 6 \times 10^{27}\ cm^{-2}s^{-1}$), with a minimum bias trigger (at present 500Hz)

➡ Gain a factor **100** in statistics over originally approved programme (Run1 + Run2)

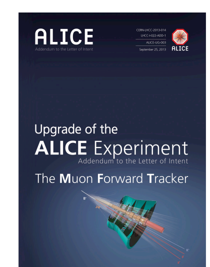
II. Significant improvement of vertexing and tracking capabilities at low p_T

- **New Inner tracking System**

It targets LHC 2^{nd} Long Shutdown (2018/19)

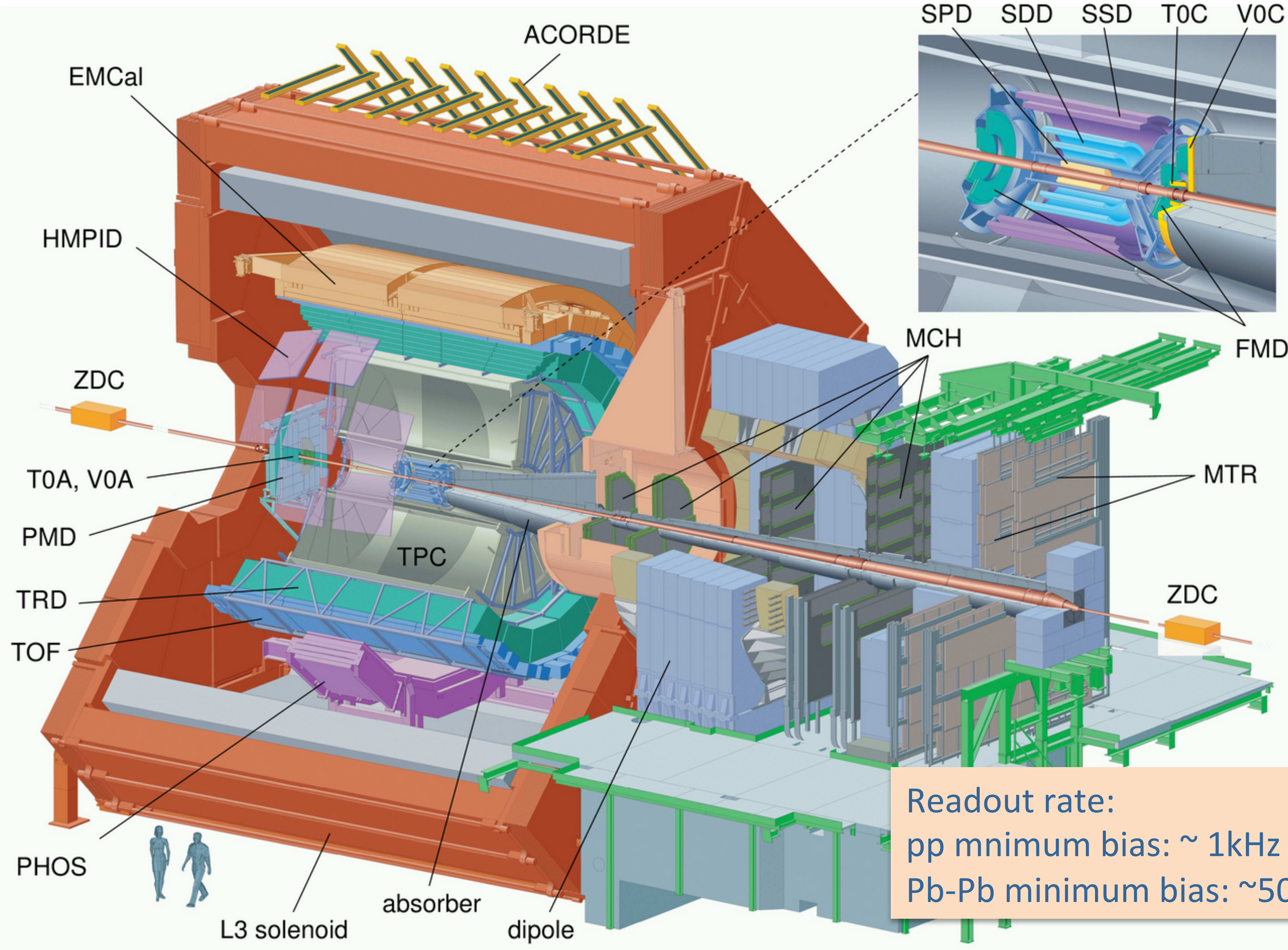


ALICE Upgrade LoI
September 2012



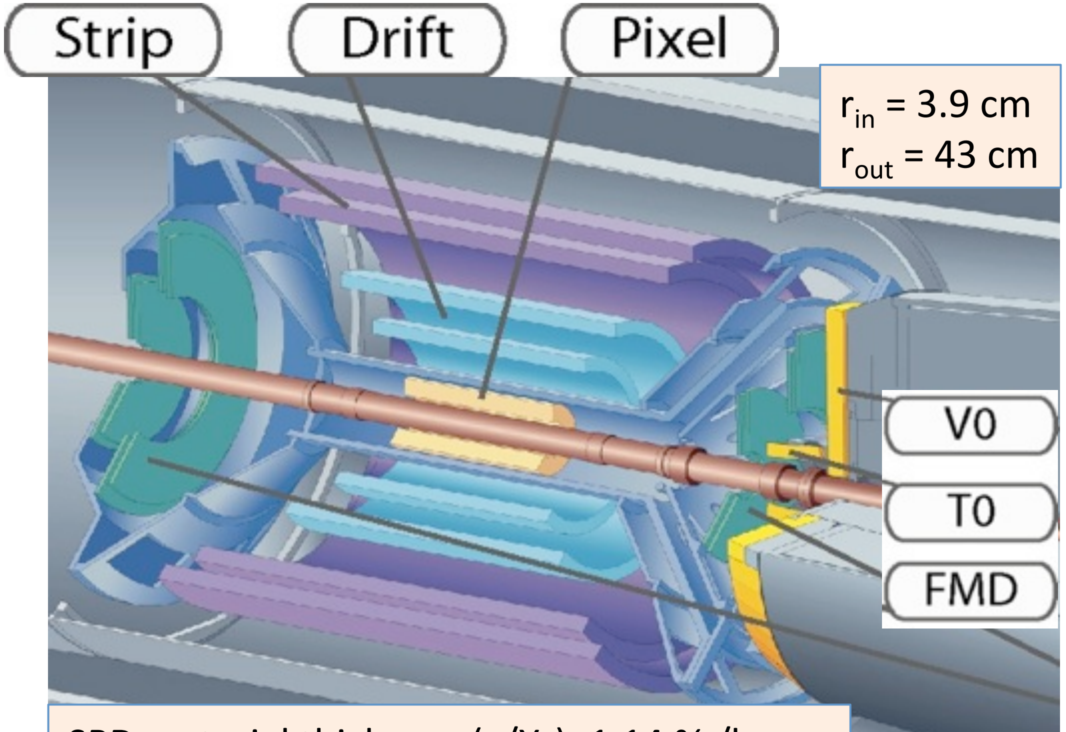
Addendum
September 2013

The Current ALICE Detector

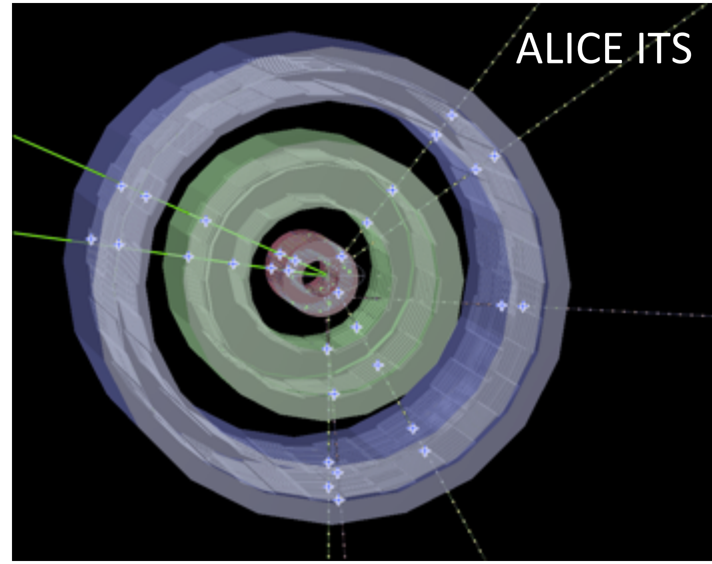


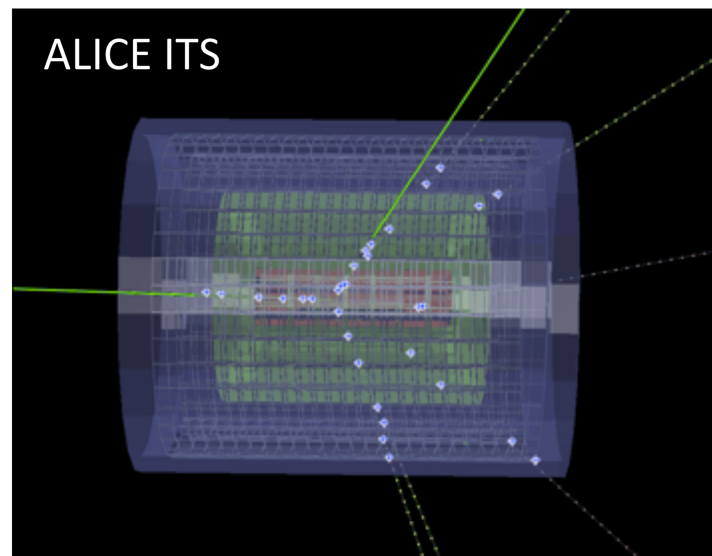
Readout rate:
pp mnimum bias: ~ 1kHz
Pb-Pb minimum bias: ~500 Hz

The Current ALICE Inner Tracking System



SPD material thickness (x/X_0): 1.14 % /layer





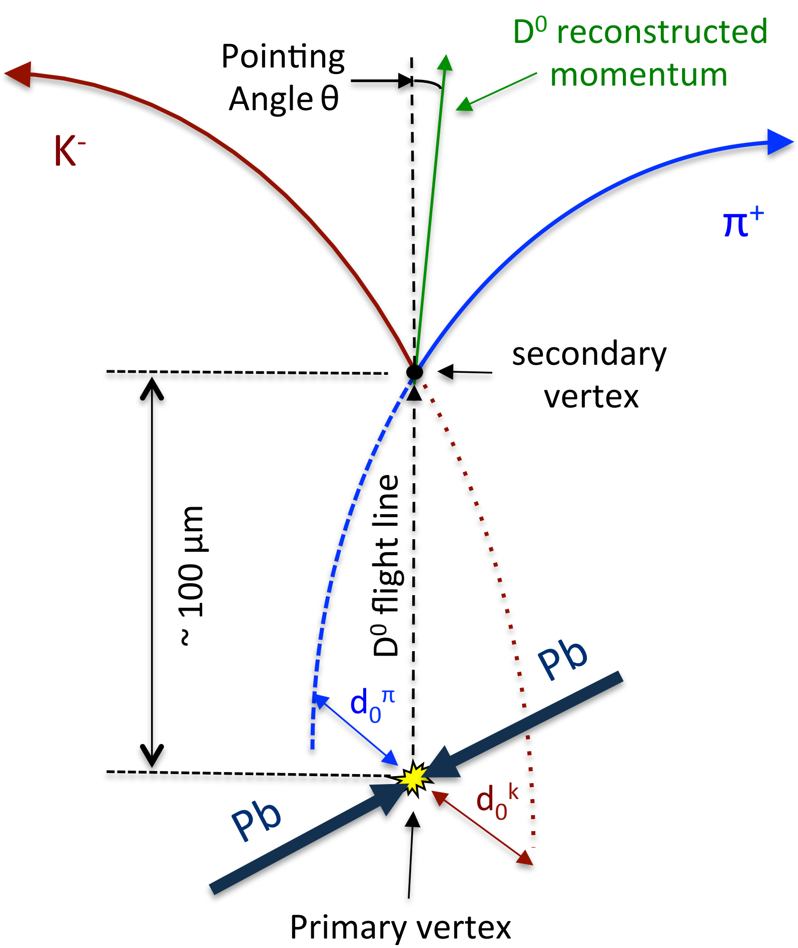
Current ITS

6 concentric barrels, 3 different technologies

- 2 layers of silicon pixel (SPD)
- 2 layers of silicon drift (SDD)
- 2 layers of silicon strips (SSD)

ITS – Secondary vertex determination

Example: D^0 meson



Analysis based on decay topology and invariant mass technique

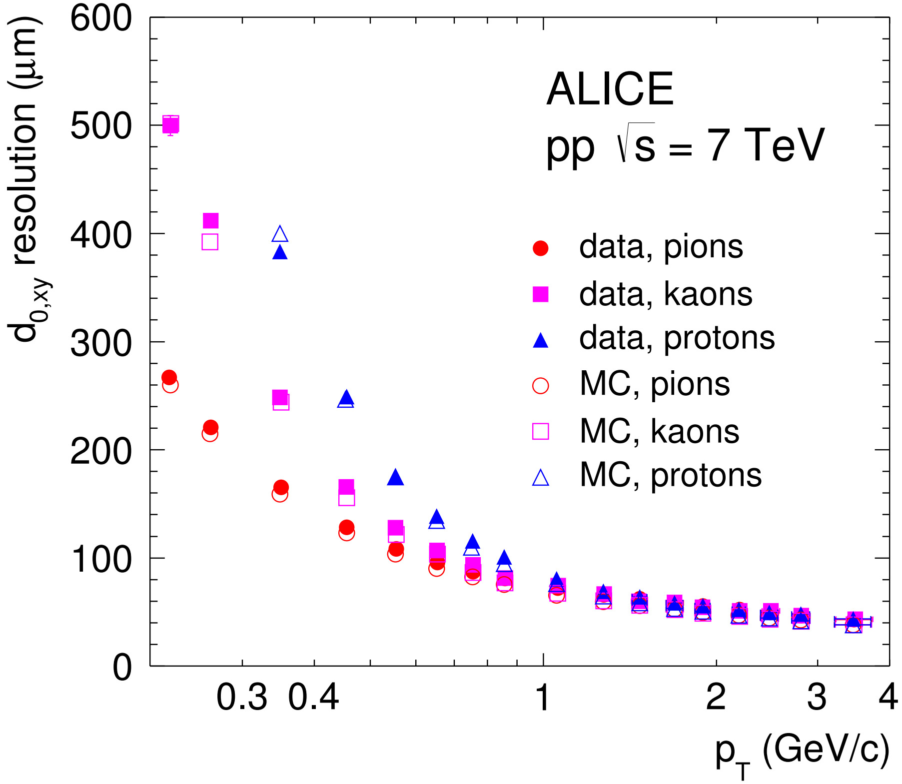
Open charm

Particle	Decay Channel	cτ (μm)
D^0	$K^- \pi^+$ (3.8%)	123
D^+	$K^- \pi^+ \pi^+$ (9.5%)	312
D_s^+	$K^+ K^- \pi^+$ (5.2%)	150
Λ_c^+	$p K^- \pi^+$ (5.0%)	60

How precisely is d_0 measured with the current ITS detector?

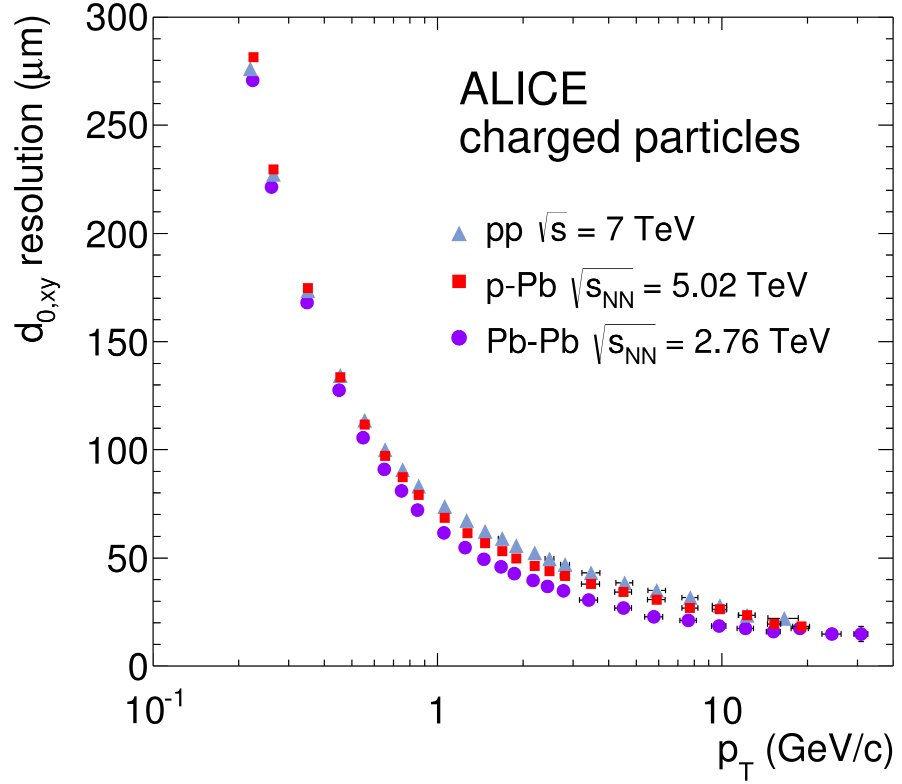
ALICE ITS Upgrade – Impact parameter resolution

Very good MC description



ALICE, Int. J. Mod. Phys. A29 (2014) 1430044

Very weak dependence on the colliding system



ALICE, Int. J. Mod. Phys. A29 (2014) 1430044

70 μm at p_T = 1 GeV/c

What determines the impact parameter resolution

Vertex projection from two points: a simplified approach (telescope equation)

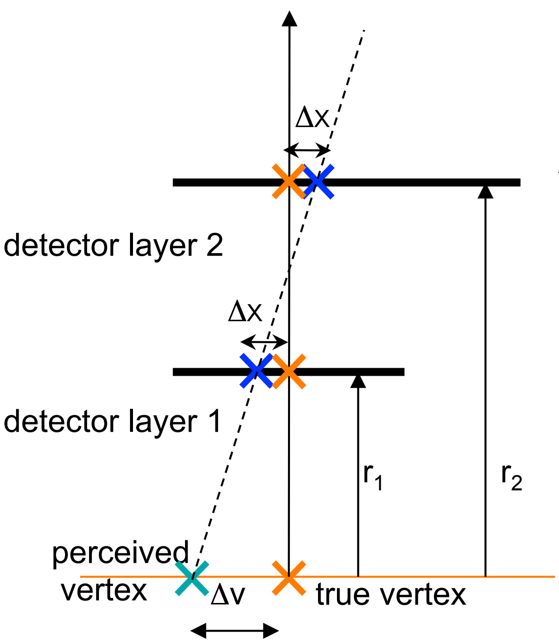
expectations for the ITS upgraded ➡ pointing resolution = (5 ⊕ 22GeV/p·c) μm

from detector position error

from coulomb scattering

first pixel layer

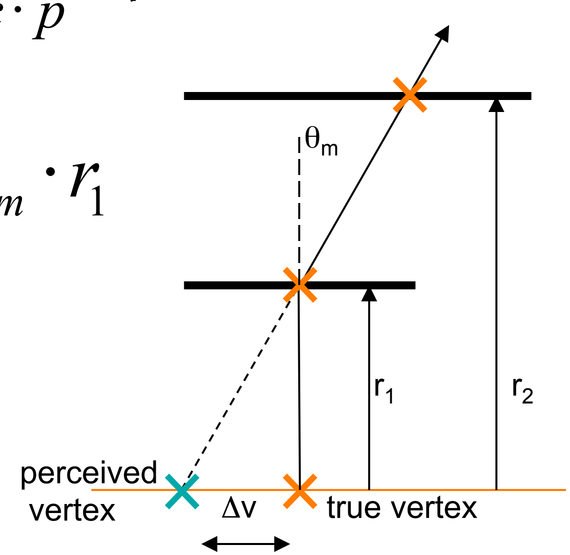
$$X_0 = 0.3\%$$



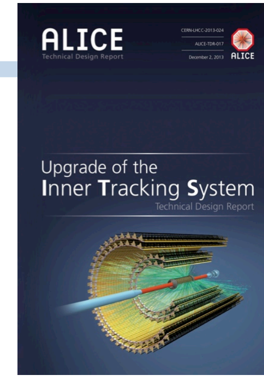
$$\Delta v = \Delta x \bullet \sqrt{\frac{r_2^2 + r_1^2}{(r_2 - r_1)^2}}$$

$$\theta_m = \frac{13.6 Mev}{\beta \cdot c \cdot p} \cdot \sqrt{X_0}$$

$$\Delta v = \theta_m \cdot r_1$$



ITS upgrade design objectives



CERN-LHCC-2013-24

1. Improve impact parameter resolution by a factor of ~3

- Get closer to IP (position of first layer): 39mm → 23mm
- Reduce x/X_0 /layer: ~1.14% → ~ 0.3% (for inner layers)
- Reduce pixel size: currently 50μm x 425μm → O(30μm x 30μm)

J. Phys. G (41) 087002

2. Improve tracking efficiency and p_T resolution at low p_T

- Increase granularity:
  - 6 layers → 7 layers
  - silicon drift and strips → pixels

3. Fast readout

- readout Pb-Pb interactions at > 100 kHz and pp interactions at ~ several 10^5 Hz (currently limited at 1kHz with full ITS)

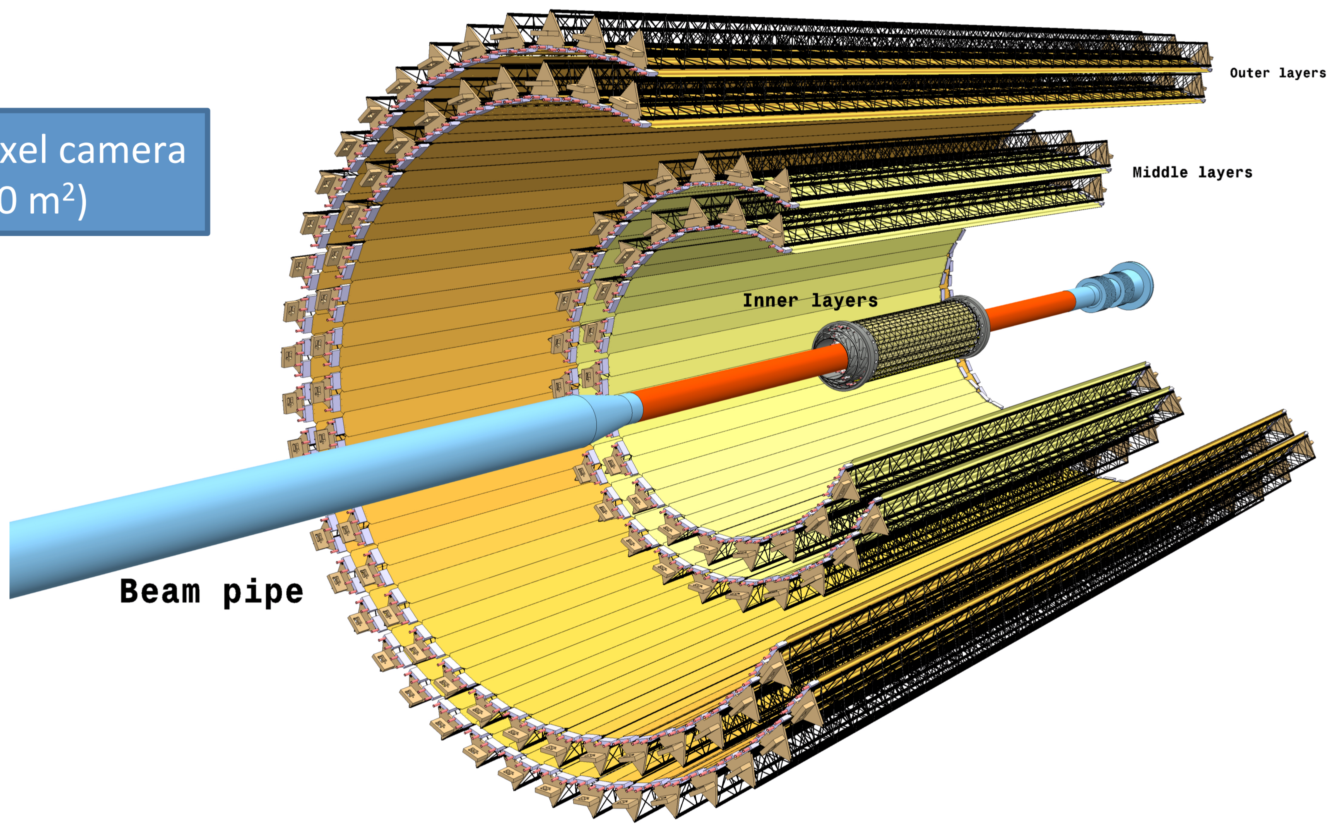
4. Fast insertion/removal for yearly maintenance

- possibility to replace non functioning detector modules during yearly shutdown

Install detector during LHCC LS2 (2018-19)

New ITS Layout

12.5 G-pixel camera
(~10 m²)



7-layer barrel geometry based on MAPS

r coverage: 23 – 400 mm

η coverage: $|\eta| \leq 1.22$
for tracks from 90% most luminous region

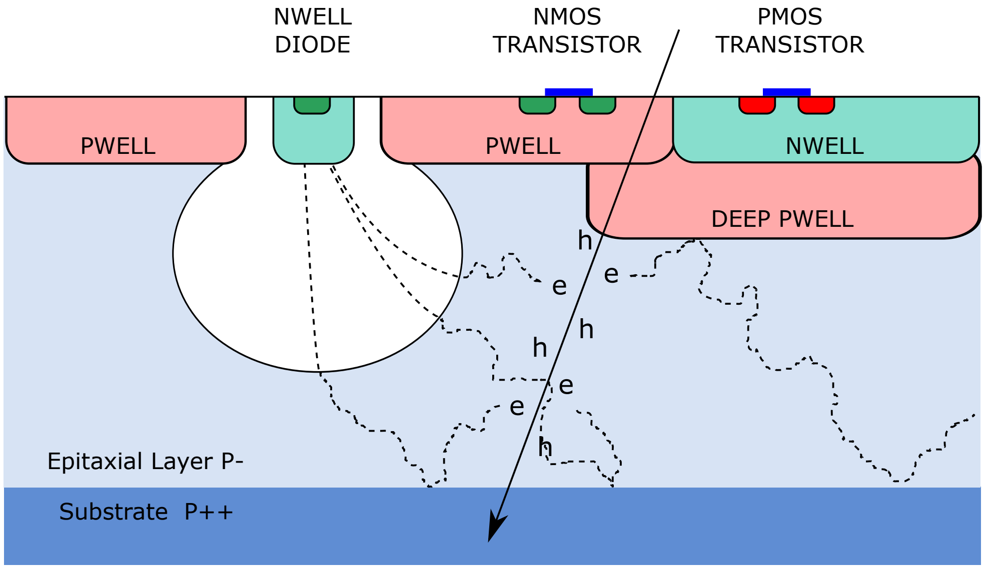
3 Inner Barrel layers (**IB**)

4 Outer Barrel layers (**OB**)

Material /layer : 0.3% X_0 (IB), 1% X_0 (OB)

ITS Pixel Chip – technology choice

CMOS Pixel Sensor using TowerJazz 0.18μm CMOS Imaging Process



Tower Jazz 0.18 μm CMOS

- feature size 180 nm
- metal layers 6

➔ Suited for high-density, low-power

- Gate oxide 3nm

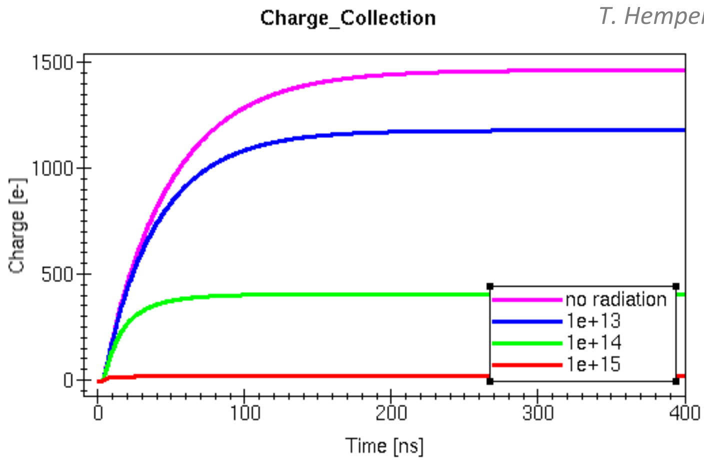
➔ Circuit rad-tolerant

- High-resistivity (> 1kΩ cm) p-type epitaxial layer (20μm - 40μm thick) on p-type substrate
- Small n-well diode (2-3 μm diameter), ~100 times smaller than pixel => low capacitance
- Application of (moderate) reverse bias voltage to substrate can be used to increase depletion zone around NWELL collection diode
- Quadruple well process: deep PWELL shields NWELL of PMOS transistors, allowing for full CMOS circuitry within active area

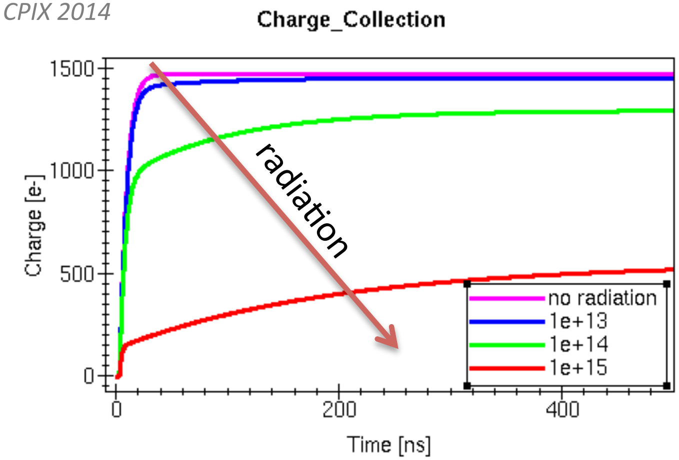
ITS Pixel Chip – starting material

Charge collection time and recombination depend on doping concentration (Si resistivity) and radiation induced dislocations

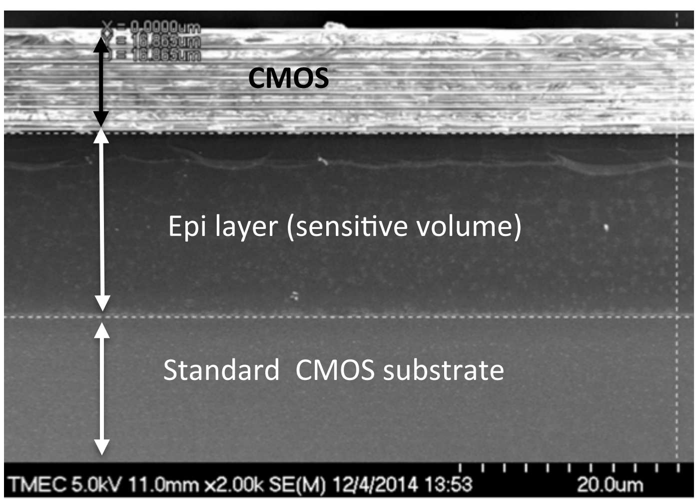
T. Hemperek (Uni Bonn) – CPIX 2014



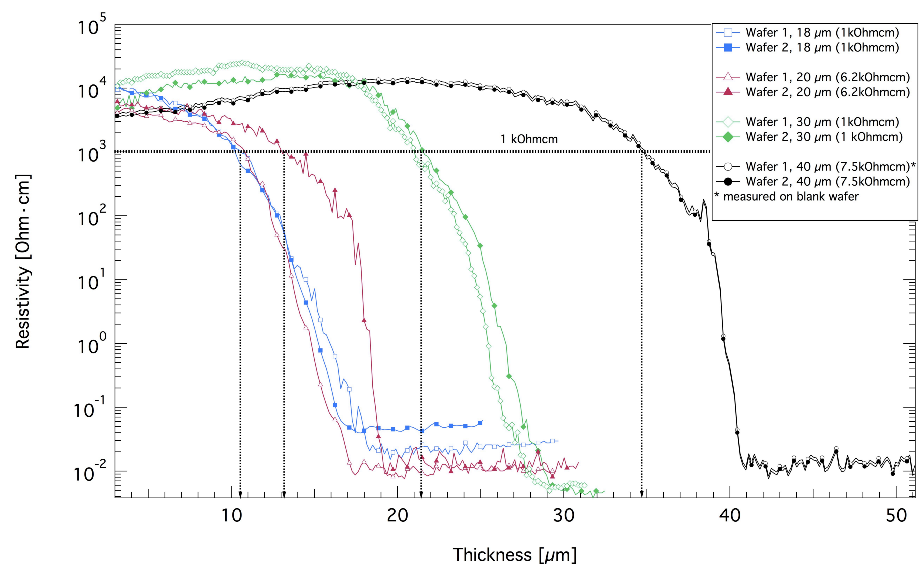
Substrate: 10 Ohm cm, NWELL: @1V PW: @ 0V



Substrate: 2k Ohm cm, NWELL: @1V PW: @ 0V



SEM picture: epi thickness 20μm



ITS Pixel Chip – starting material

Thicker epitaxial layers will yield more charge but … diffusion increases cluster size

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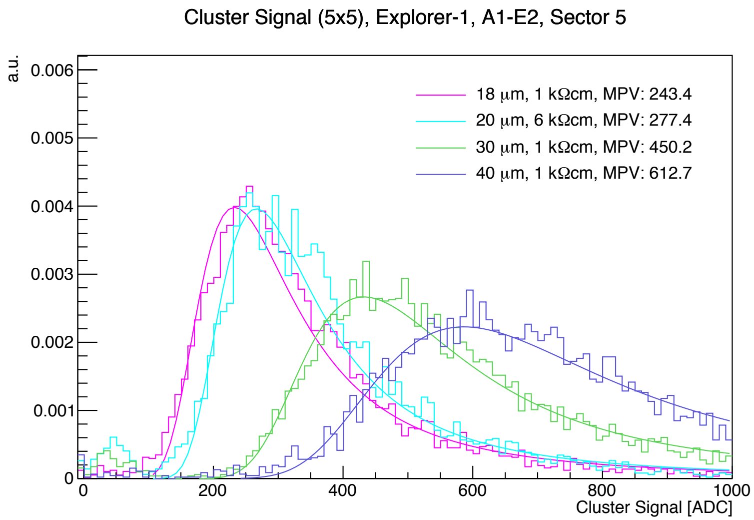
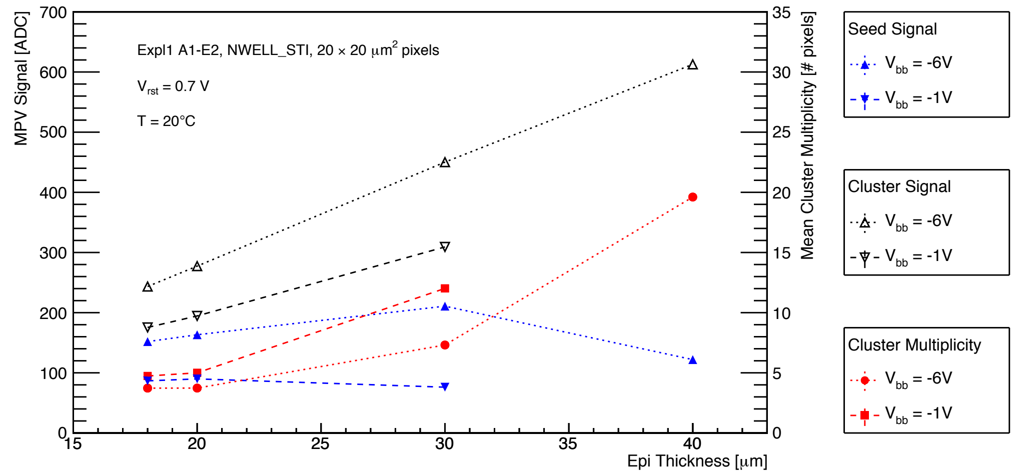




J. Van Hoorne, TIPP2014

Measurements done at Desy test beam with 3.2 Gev/c positrons

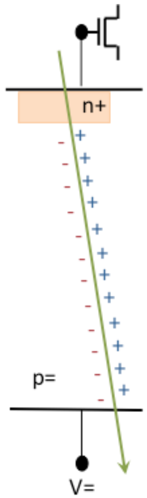
- Cluster charge increases linearly with epi-layer thickness
- Cluster size increases with epi-layer thickness

optimum epi thickness (maximum seed signal) increases by increasing depletion volume

ITS Pixel Chip – starting material

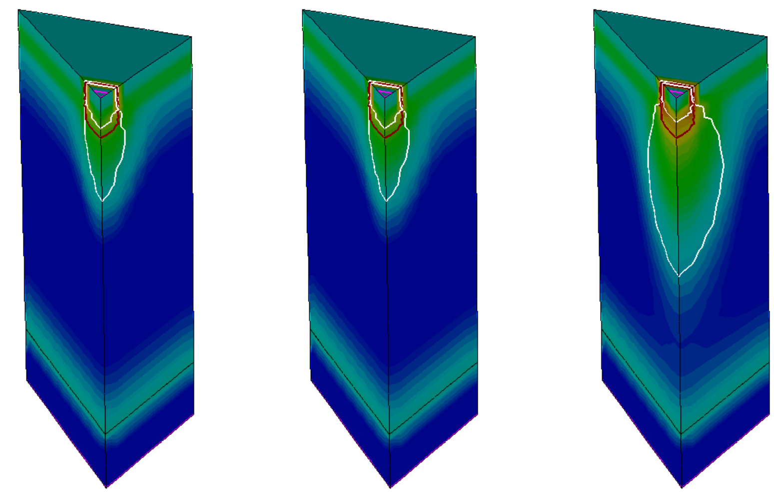
Low input capacitance decisive to achieve large S/N at low power

(W. Snoeys, NIMA 731 (2013) 125-130)



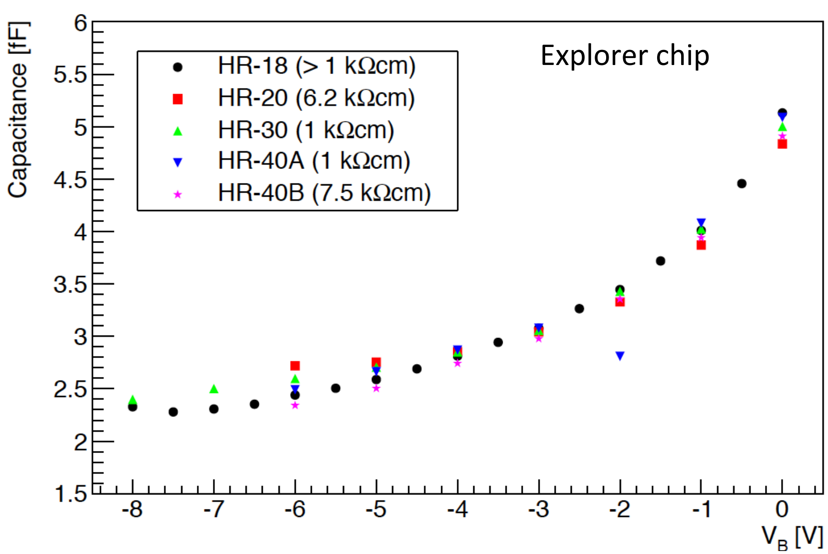
NWELL DIODE output signal = Q /C

- Minimize spread of charge over many pixels
- minimize capacitance:
  - ➡ small diode surface
  - ➡ large depletion volume



-1V, $1x10^{13}$ cm^{-3} -1V, $1x10^{12}$ cm^{-3} -6V, $1x10^{12}$ cm^{-3}

Diode 3μm x 3μm square n-well , White line: boundaries of depletion region



☞ Pixel input capacitance decreases with increasing reverse bias, in agreement with simulated size of depletion region

☞ Minor influence of epi resistivity for current pixel layout

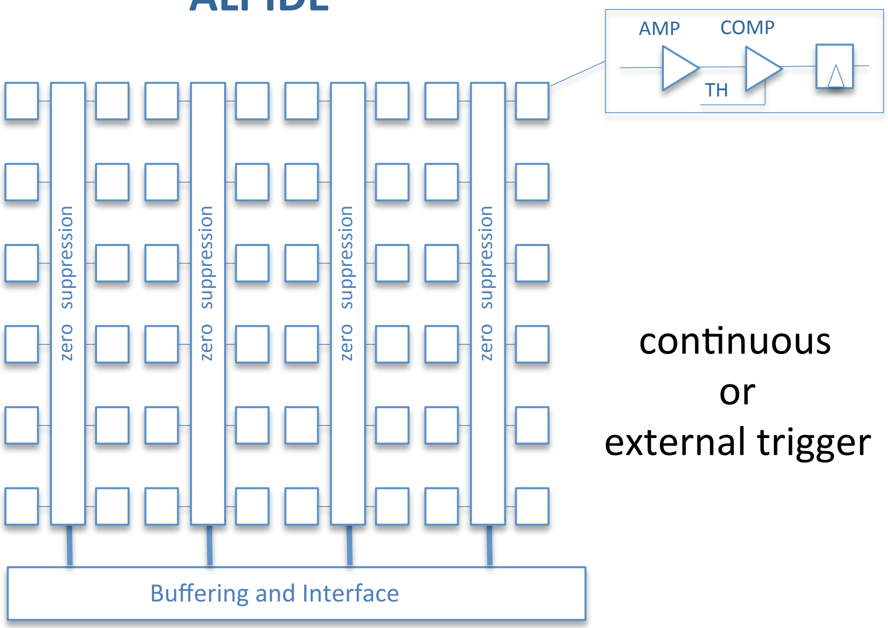
PIXEL Chip – General Requirements

Parameter	Inner Barrel	Outer Barrel
Silicon thickness	50 μm	
Spatial resolution	5 μm	10 μm
chip dimensions	15 mm x 30 mm	
Power density	< 300 mW/cm^2	< 100 mW/cm^2
Event time resolution	< 30 μs	
Detection efficiency	> 99%	
Fake hit rate	< 10^{-5} per readout frame	
TID radiation hardness (*)	2700 krad	100 krad
NIEL radiation hardness (*)	1.7×10^{13} 1MeV n_{eq}/cm^2	10^{12} 1MeV n_{eq} / cm^2

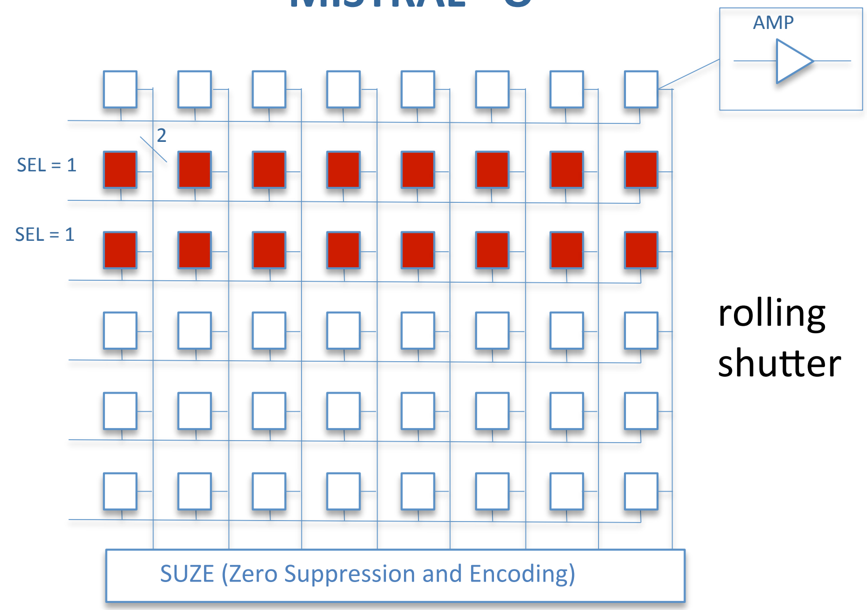
(*) 10 x radiation load integrated over approved programme (~ 6 years of operation)

ITS Pixel Chip – two architectures

ALPIDE



MISTRAL - O



Pixel pitch	28μm x 28μm	Pixel pitch	36μm x 64μm
Event time resolution	<2μs	Event time resolution	~20μs
Power consumption	39mW/cm^2	Power consumption$^{(*)}$	97mW/cm^2
Dead area	1.1 mm x 30mm	Dead area	1.7 mm x 30mm

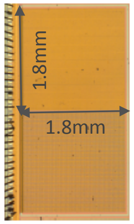
ALPIDE and MISTRAL-O have same dimensions (15mm x 30mm), identical physical and electrical interfaces: position of interface pads, electrical signaling, protocol

$^{(*)}$ might further reduce to 73mW/cm^2

ALPIDE Development

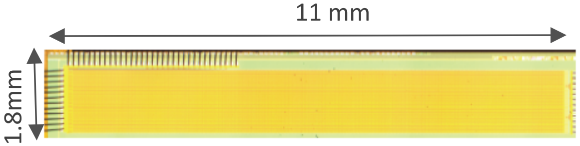
2012 — Explorer

- 20μm x 20μm and 30μm x 30μm pixels (analogue readout)
- pixel geometry, starting material, sensitivity to radiation



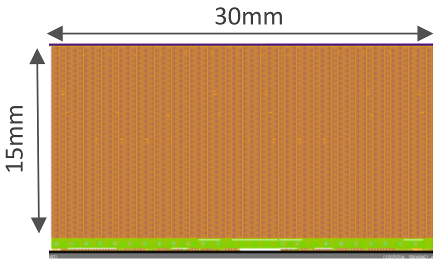
2013 — pALPIDEss-0

- Matrix with 64 columns x 512 rows
- 22μm x 22μm pixels
- (in-pixel discrimination and buffering)
- zero suppression within pixel matrix



May-2014 — pALPIDE-1

- **Full-scale prototype:** 1024 x 512
- 4 sectors with different pixels
- Final pixel pitch: 28μm x 28μm
- Interface pads over matrix
- 1 register/pixel, no final interface



Apr-2015 — pALPIDE-2

- Optimization of some circuit blocks
- Final interface: allows integration into ITS modules
- NO high-speed output link (1.2 Gbit/sec replaced by a 40Mb/s)

pALPIDE-1 – Main Design Features

ALPIDE Full Scale prototype

- Dimensions: 30mm x 15 mm
- Pixel Matrix: 1024 cols x 512 rows
- Pixel pitch: 28μm x 28μm
- Peaking time (defines time res): <2μs
- Pulse length: 10-20μs
- In-pixel discriminator + 1 register
- Power consumption: < 40mW/cm^2
- 4 sectors with different pixels

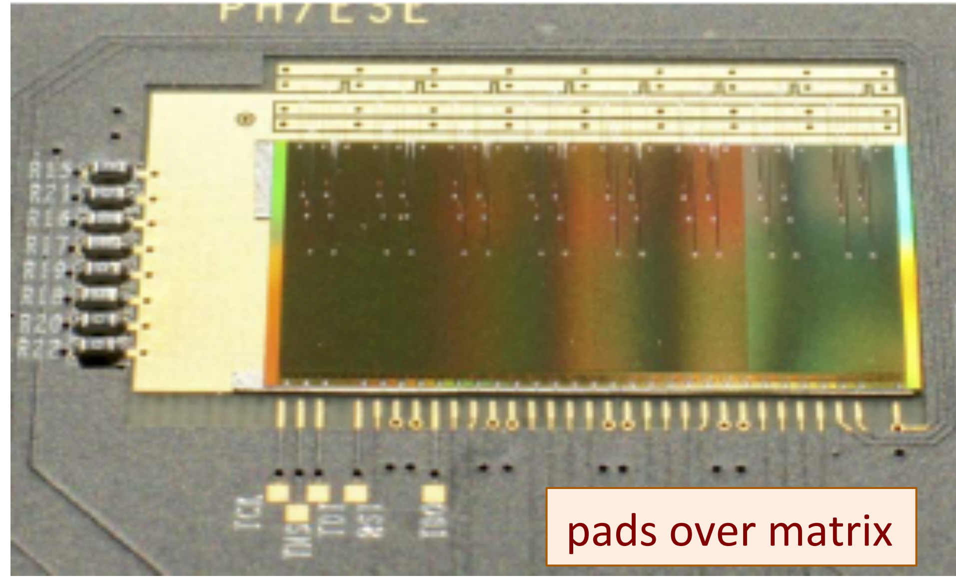
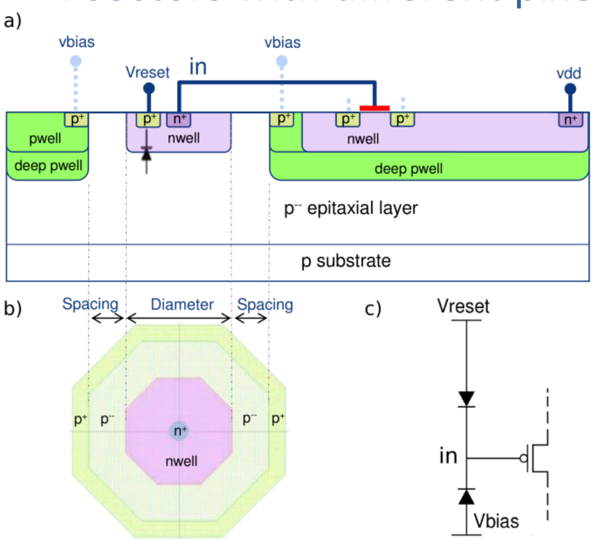


Figure: picture of pALPIDE-1



Sector	nwell diameter	spacing	pwell opening	reset
0	2μm	1μm	4μm	PMOS
1	2μm	2μm	6μm	PMOS
2	2μm	2μm	6μm	Diode
3	2μm	4μm	10μm	PMOS

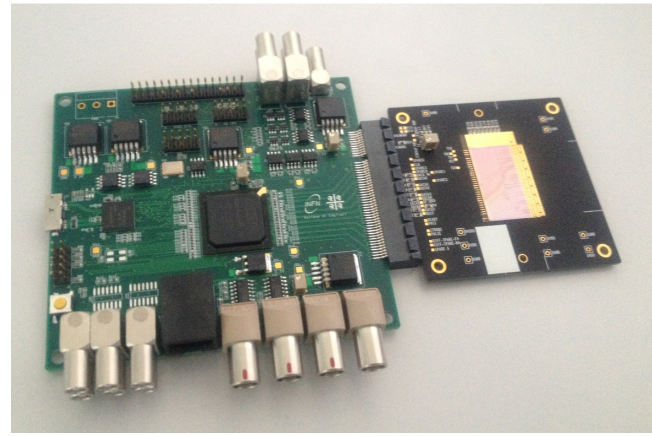
pALPIDE-1 Characterization

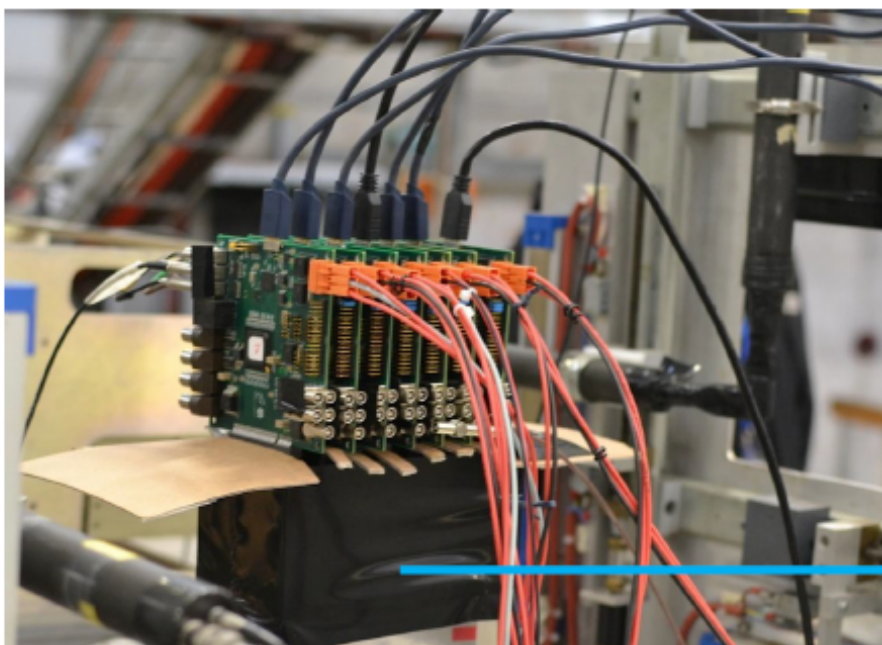
Intensive test beam campaign

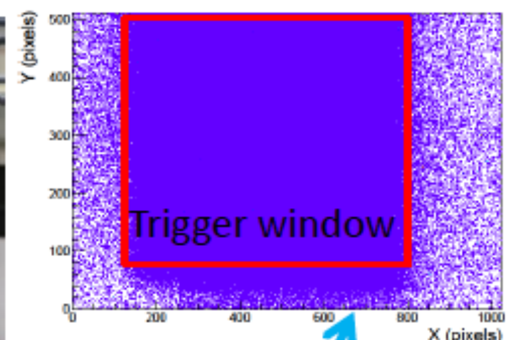
- PS: 5-7 Gev π^-
- SPS: 120 Gev π^-
- PAL (Korea): 60 MeV e^-
- BTF (Frascati): 450 MeV e^-
- DESY: 5.8 Gev e^+

Scan of main parameters → ~ 200 settings

7-plane telescope based on pALPIDE-1 chip



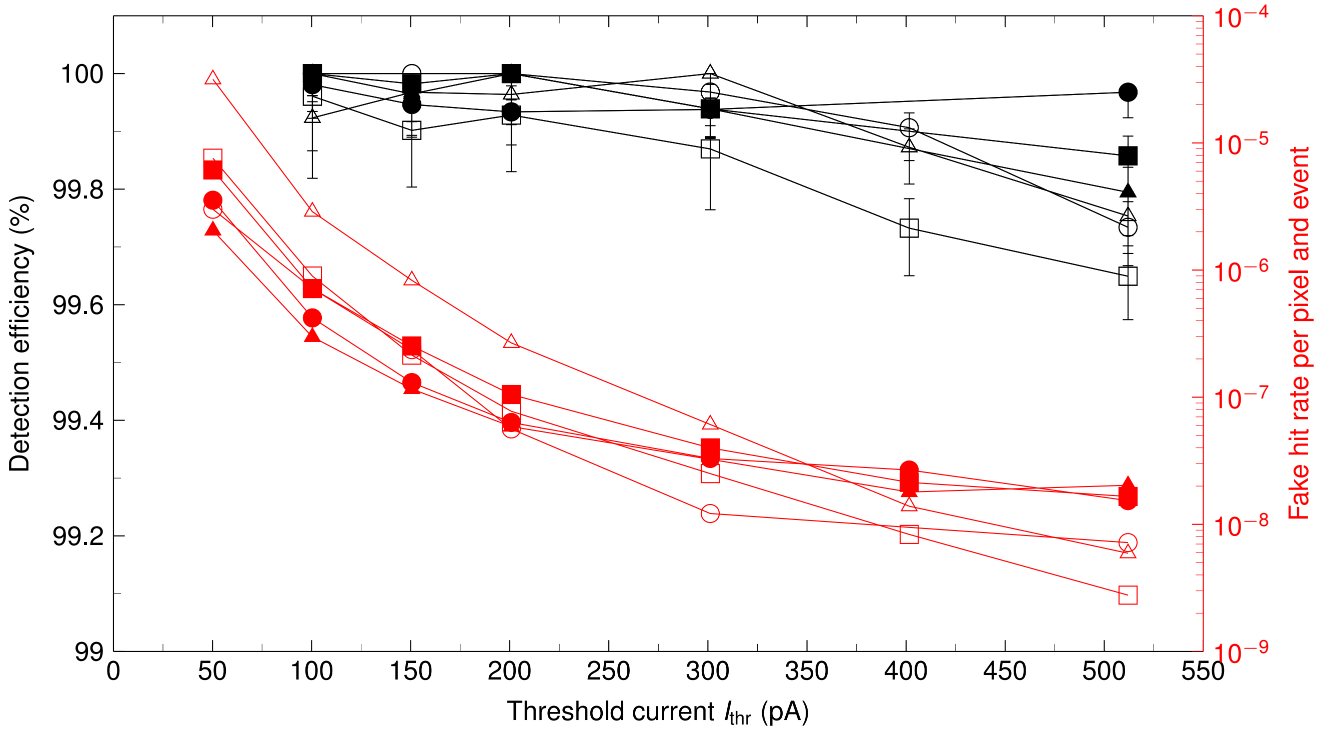




hit map

pALPIDE-1 – PS test beam (Sep 2014)

Efficiency and fake hit rate



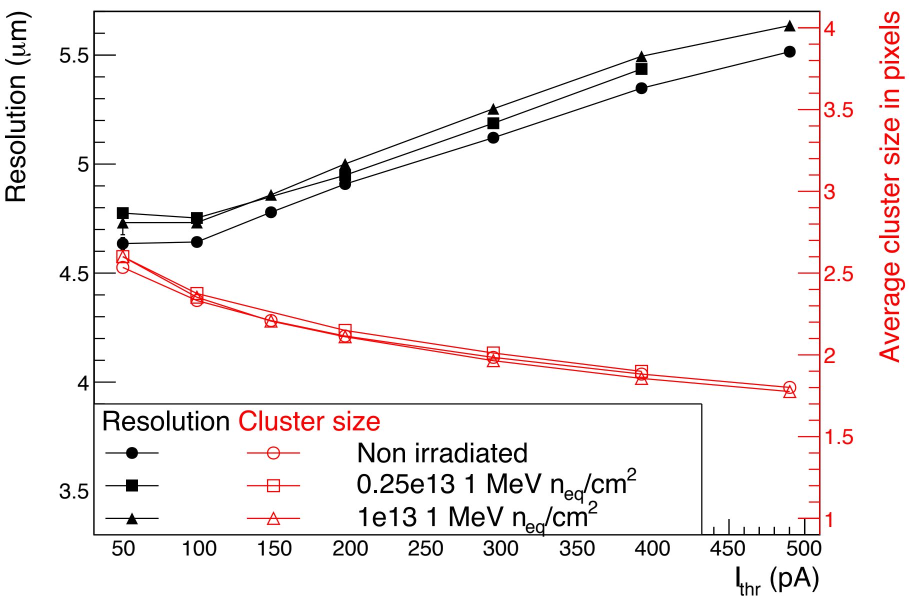
50 pA ➔ ~80 e
500 pA ➔ ~180 e

$\lambda_{fake} << 10^{-5}$ / event/pixel @ $\varepsilon_{det} > 99\%$ ➡ very large margin over design requirements

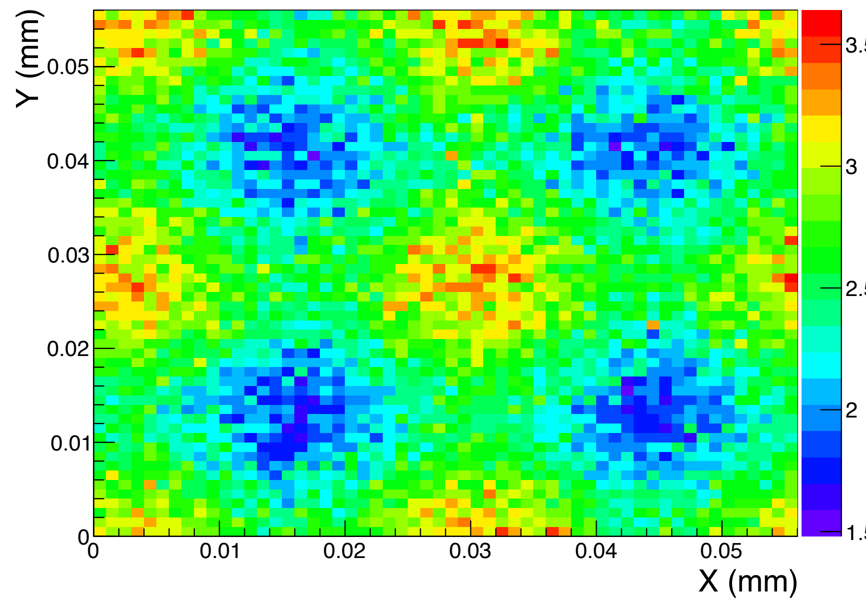
- Measurements at PS: 5 – 7 GeV π^- December 2014
- Results refer to 50 μm thick chips: 3 non irradiated and 3 irradiated with neutrons at 10^{13} 1MeV n_{eq} / cm^2

pALPIDE-1 – PS test beam (Sep 2014)

Spatial resolution



Cluster size vs. position within pixel



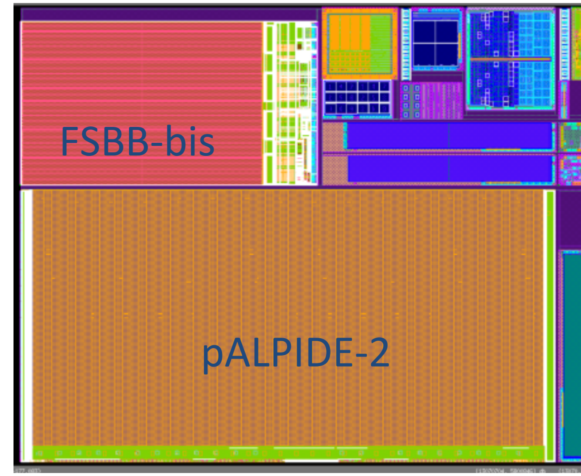
$\sigma_{det} < 5\ \mu m$ is achieved with sufficient margin of operation

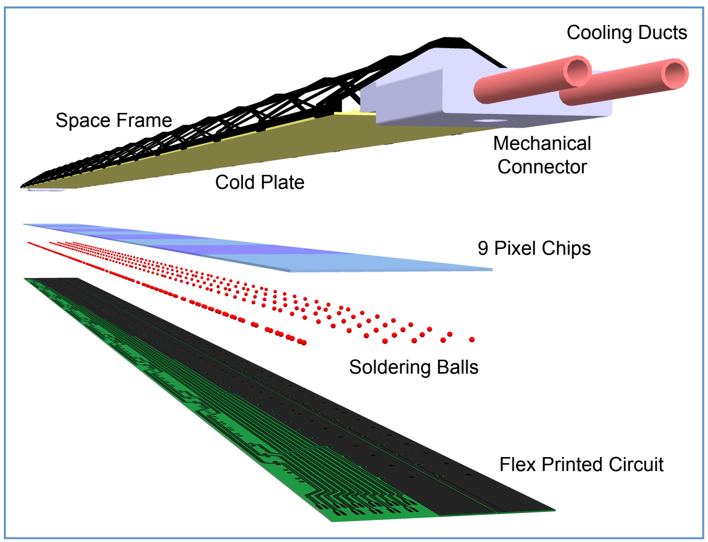
- Measurements at PS: 5 – 7 GeV π^- September 2014
- Results refer to 50 μm thick chips: non irradiated and irradiated with neutrons 0.25 x 10^{13} and 10^{13} 1MeV n_{eq} / cm^2

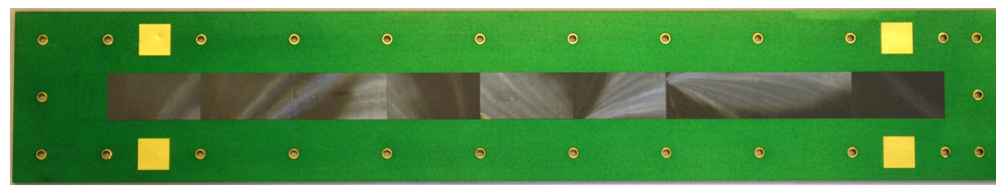
ALPIDE finalization

p-ALPIDE-2: 2nd full-scale prototype

- Optimization of some circuit blocks
- NO high-speed output link (1.2 Gbit/sec replaced by a 40Mb/s)
- Full Integration in IB and OB Module: main focus in 2015
- Delivery: April







p-ALPIDE-3: 3rd full-scale prototype

- Contains all final elements
- Submission: May '15 Delivery: July '15

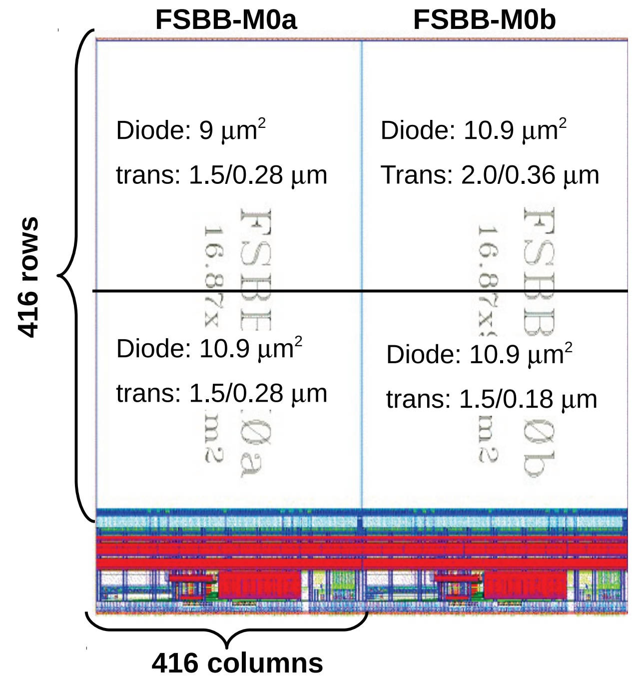
p-ALPIDE-4: pre-series production

- Submission Dec '15

MISTRAL FSBB-M0

FSBB Main Features

- About 1/3 of complete sensor (approx. 9mm x 17mm)
- Pixel Matrix: 416 Columns x 416 Rows
- Staggered Pixel: 22μm x 33μm (final chip 36μm x 64μm)
- In-pixel pre-amplification and clamping (6 metals)
- Double row-readout at 160MHz
- Integration time: 40μs (final chip 20μs)
- 2 versions (FSBB-M0 a & b): only results for M0-a will be shown



NB: the FSBB is not opimized in some respects (pixel dimensions, speed, power consumption, pads over matrix, ...)

Currently MISTRAL-O is being optimized for use in the outer layers:

- less need for spatial resolution: ~10μm
- more stringent power consumption limit: < 100mW/cm^2

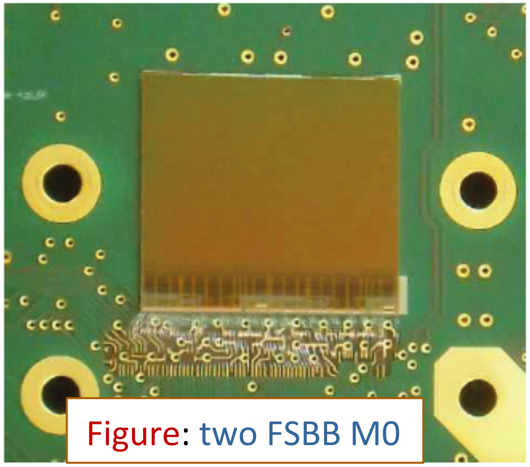
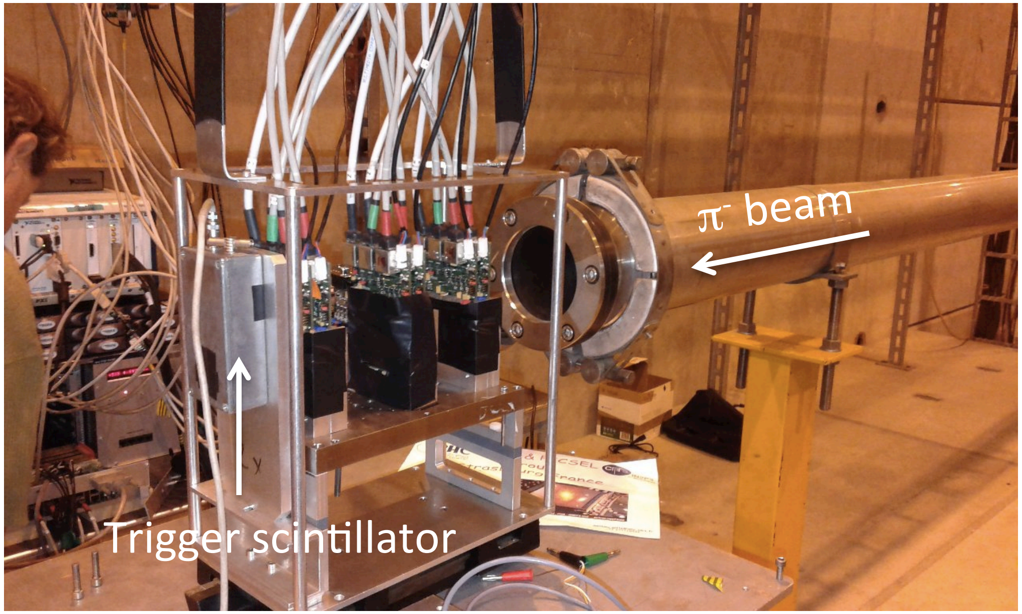
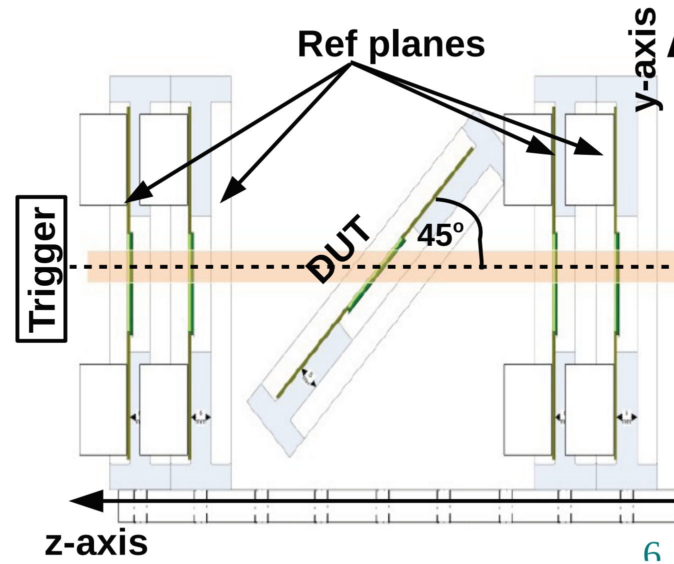


Figure: two FSBB M0

MISTRAL FSBB-M0 – SPS test beam (Oct 2014)

ALICE





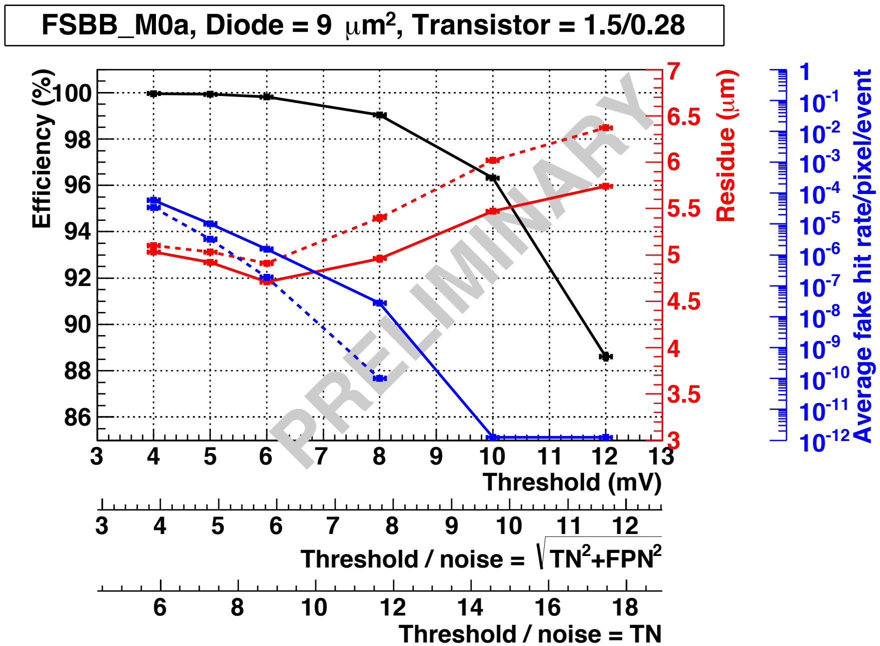
Beam conditions

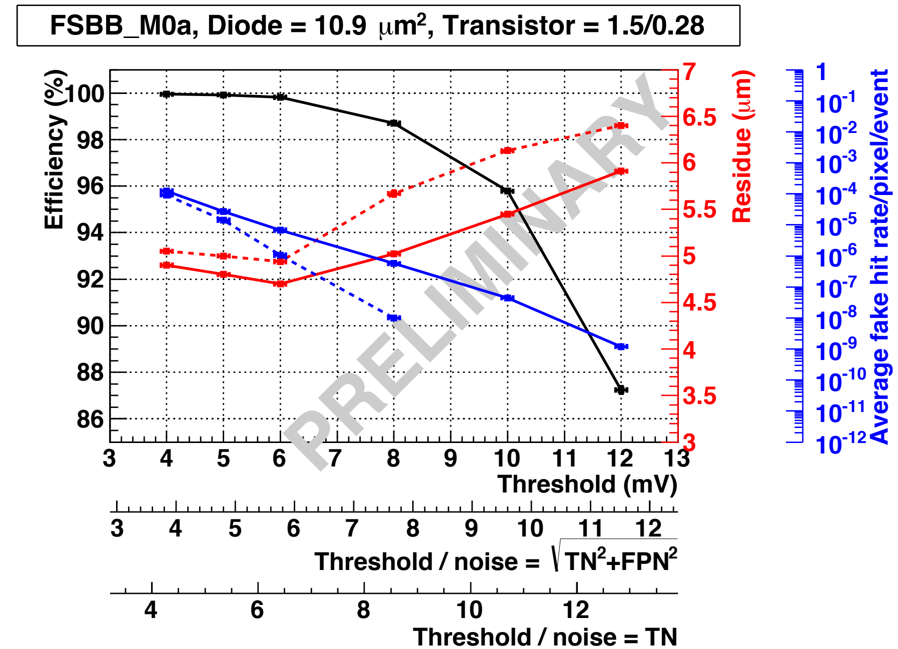
- SPS H6A area, 120 Gev π^-
- Particle flux: trigger rate in the range 2.5 to 100 kHz / 5x10 mm^2

Device and operational conditions

- 6 FSBB-M0a thinned to 50μm
- All measurements performed at T_{op} = 30 °C

MISTRAL FSBB-M0 – detection performance

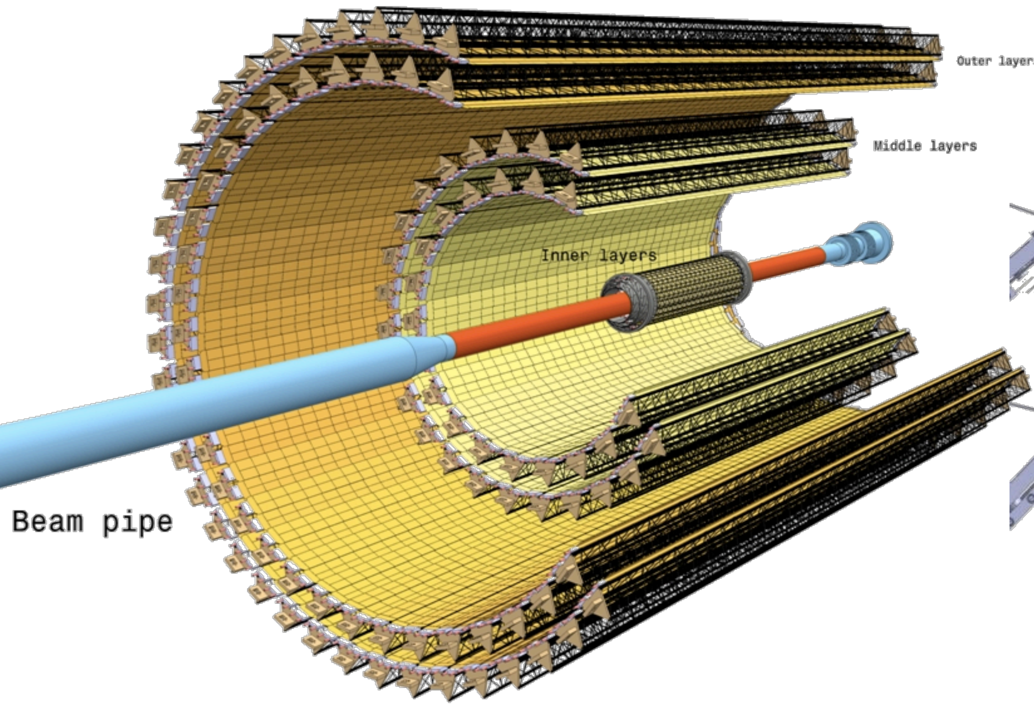


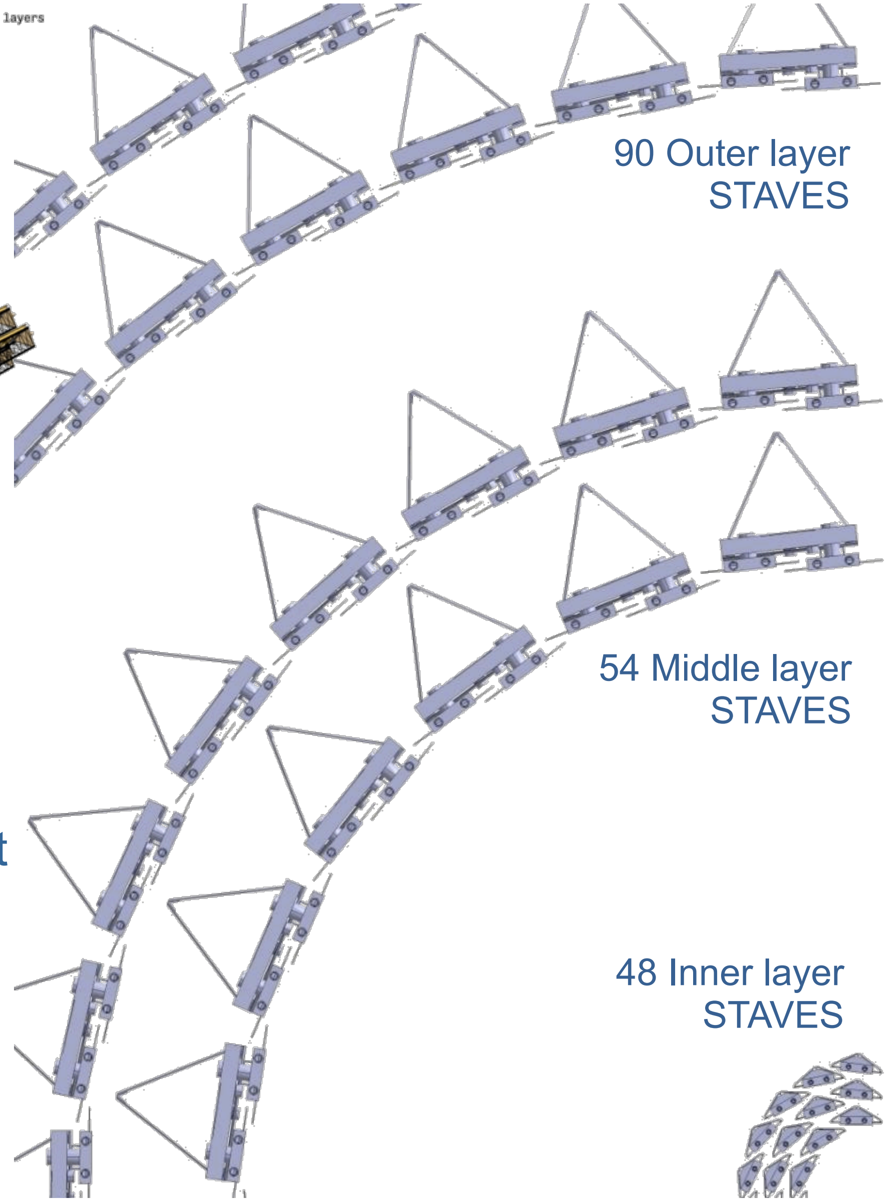


Diode size (μm^2)	$\varepsilon_{det} \geq 99.8\%$	$\varepsilon_{det} \geq 99.5\%$	$\varepsilon_{det} \geq 99.0\%$	$\lambda_{fake}^{(*)} \leq 10^{-5}$
11	Thr ≤ 6.0 mV	Thr ≤ 6.5 mV	Thr ≤ 8.0 mV	Thr ≥ 6.0 mV
9	Thr ≤ 6.0 mV	Thr ≤ 7.0 mV	Thr ≤ 8.0 mV	Thr ≥ 5.0 mV

(*)
- Fake rate drops by O(10) masking 20 noisiest pixels.
- Final chip includes masking feature

New ITS layout

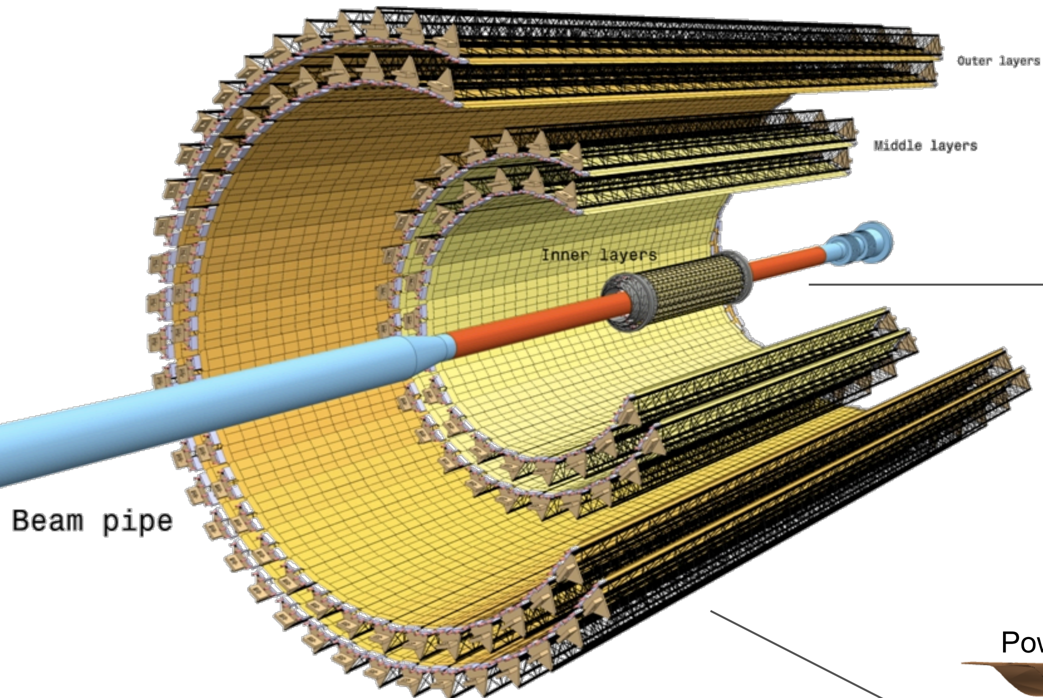


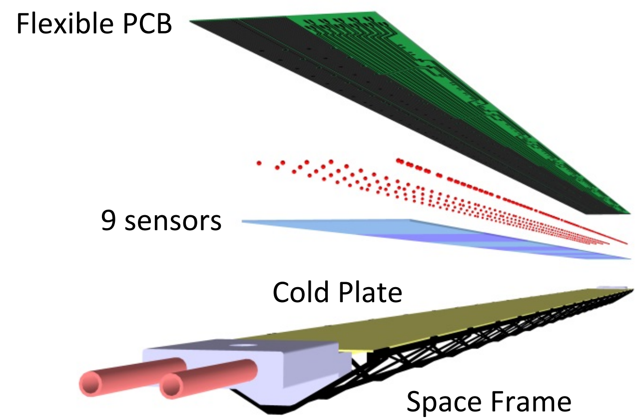


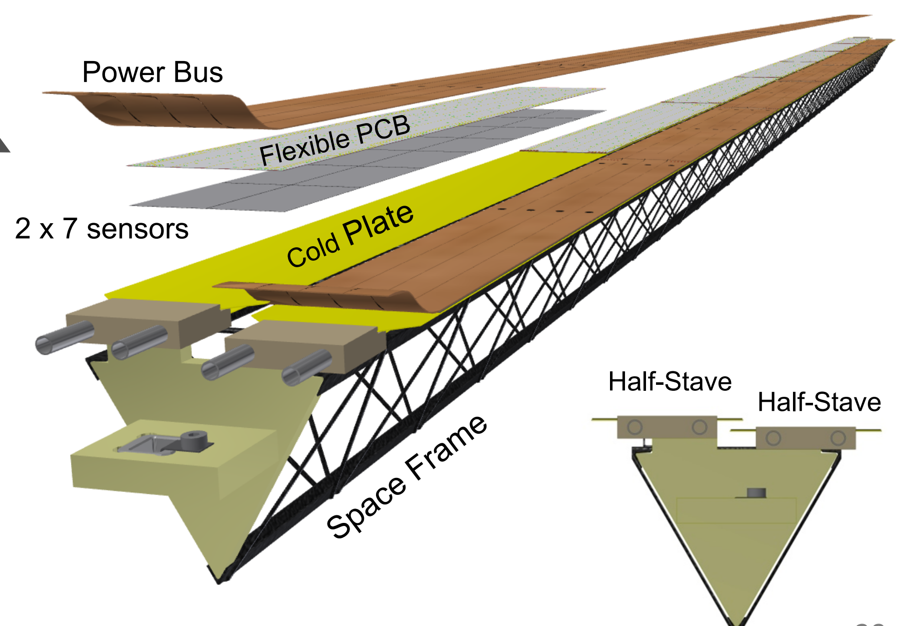
ITS layers are (azimuthally) segmented in staves, which are mechanically independent

Radial coverage 23mm÷405mm

New ITS Staves



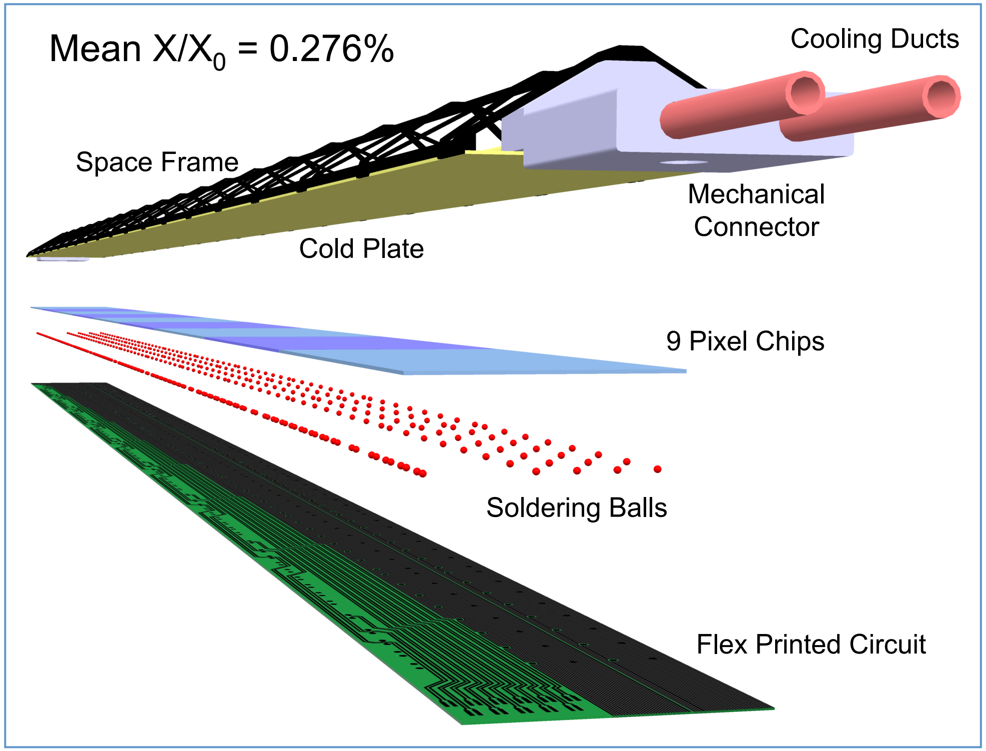


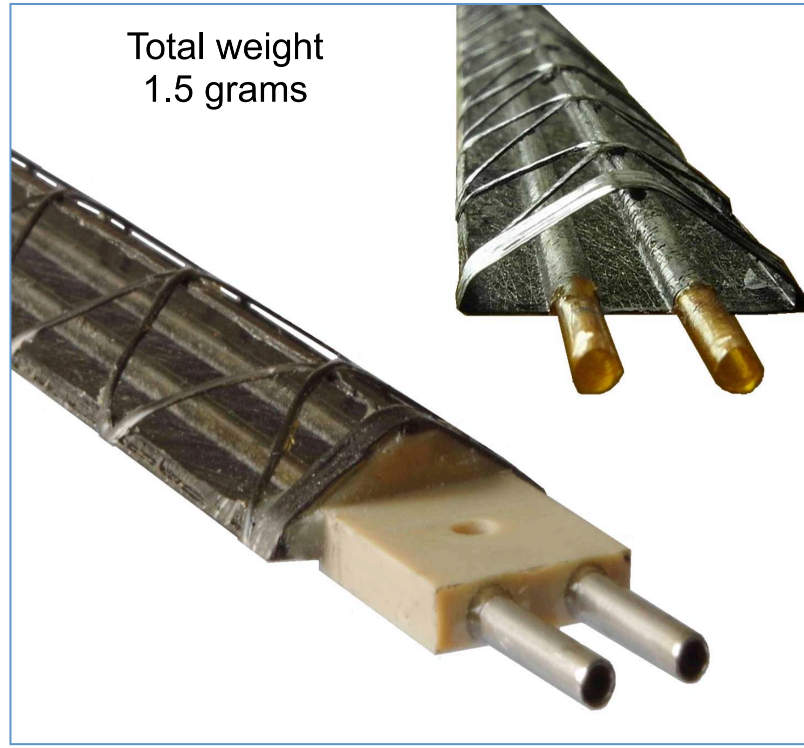


ITS staves length

Inner Layers	290mm
Middle Layers	900mm
Outer Layers	1500mm

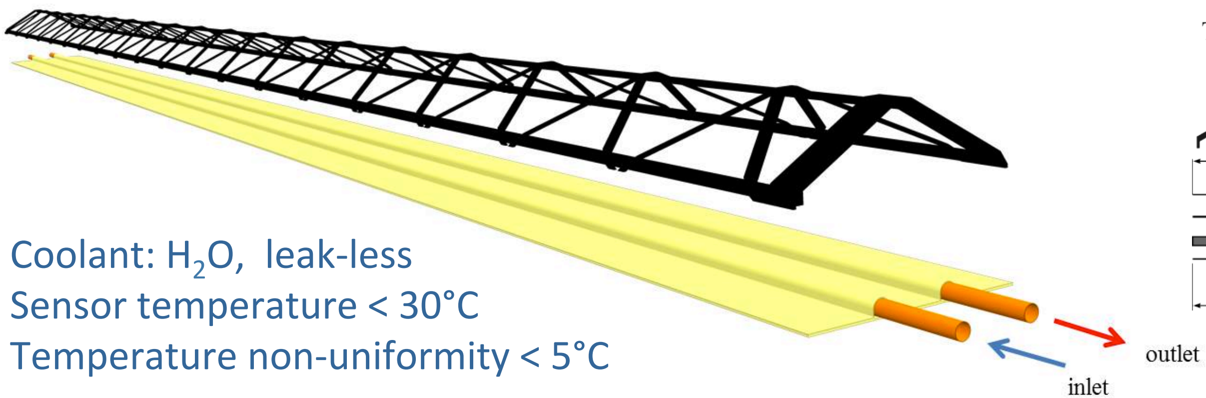
New ITS Layout - Inner Barrel Stave



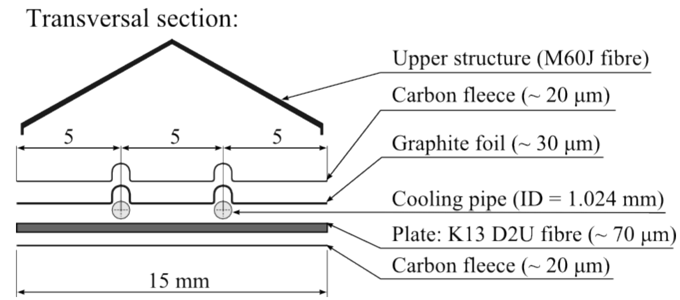


<Radius> (mm): 23,31,39	Length in z (mm): 290
Nr. of staves: 12, 16, 20	Nr. of chips/stave: 9
Nr. of chips/layer: 108, 144, 180	Material thickness: ~ 0.3% X_0
Power density: < 100 mW/cm^2	Throughput (@100kHz): < 80 $Mb/s \times cm^{-2}$

Inner Barrel – Geometry and material budget



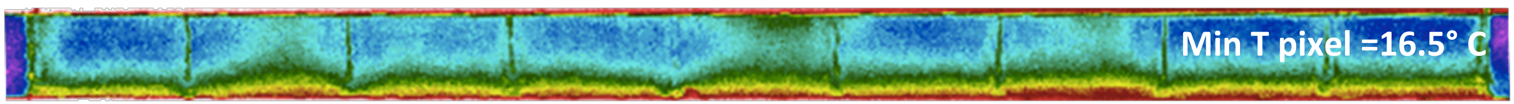
Coolant: H_2O, leak-less
Sensor temperature < 30°C
Temperature non-uniformity < 5°C



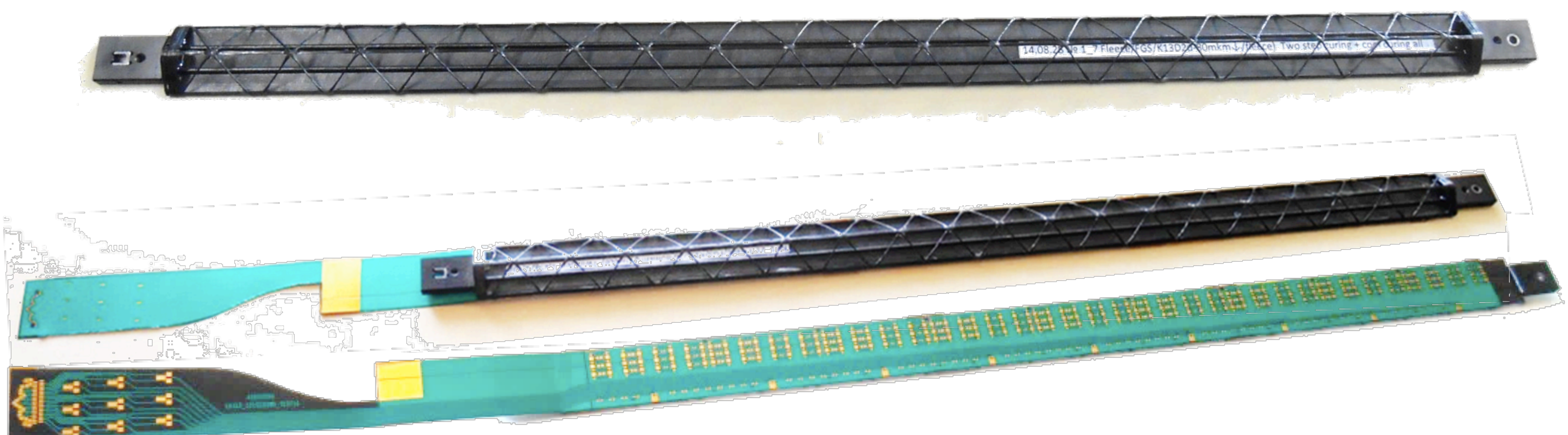
290mm length, 1.5gram weight

Tin=15.8° C

Tout=16.6 °C

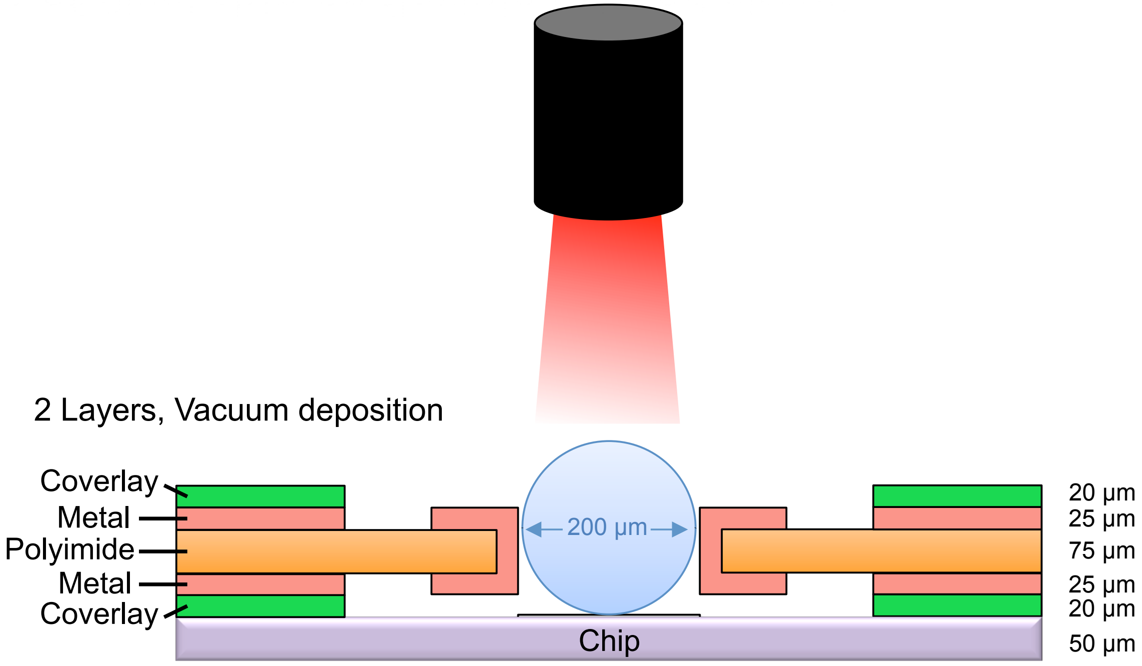


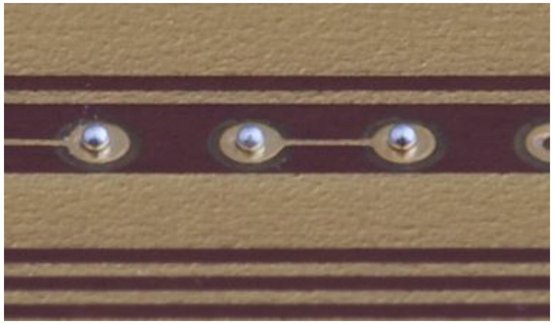
Max T periph=18.5° C

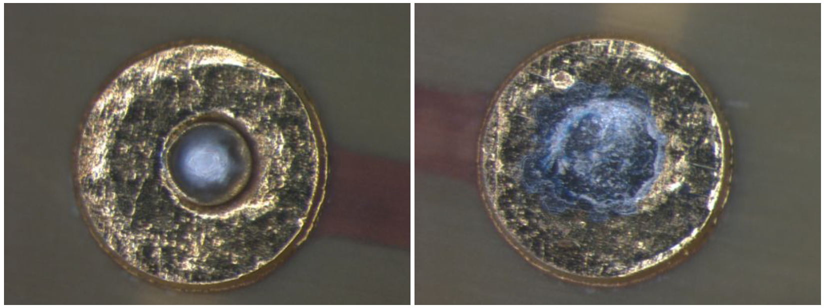


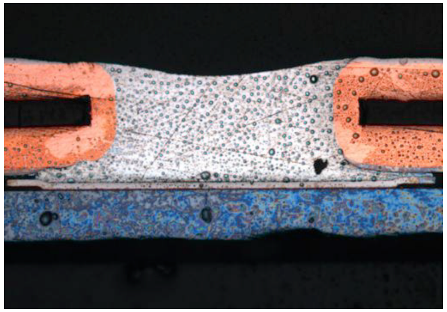
Interconnection of pixel chip to flex PCB

Laser soldering: Interconnection of Pixel chip on flexible printed circuit





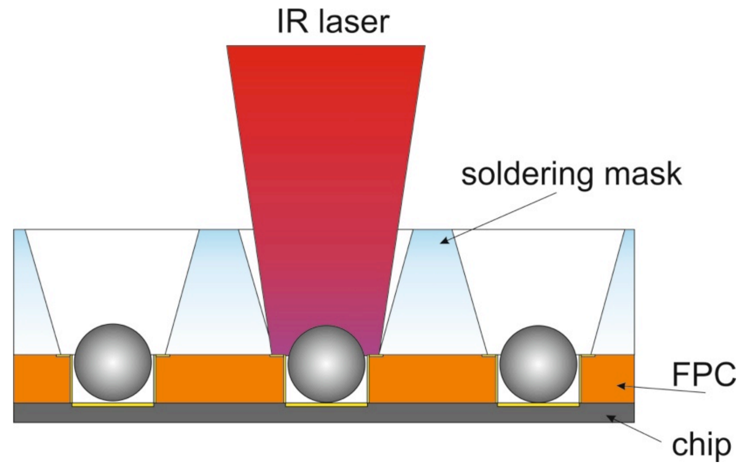


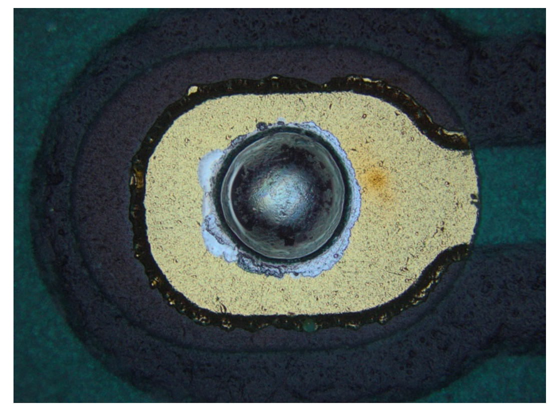


Interconnection of pixel chip to flex PCB

Laser Soldering

- Flux-less soldering of 200 μm diameter Sn/Ag(96.5/3.5) balls (227 ^{o}C melting T) in vacuum ($\leq 10^{-1}$ mbar)
- IR diode laser, 976 nm, 25 W, 50 mm focal length, 250 μm beam spot size
- Laser power modulated by pyrometer, programmable T profile ensures precise limitation of heating
- Soldering mask (in Macor® or Rubalit ®) used to press FPC on chip and guide soldering balls inside FPC vias
- Solder provides electrical and mechanical connection → no glue



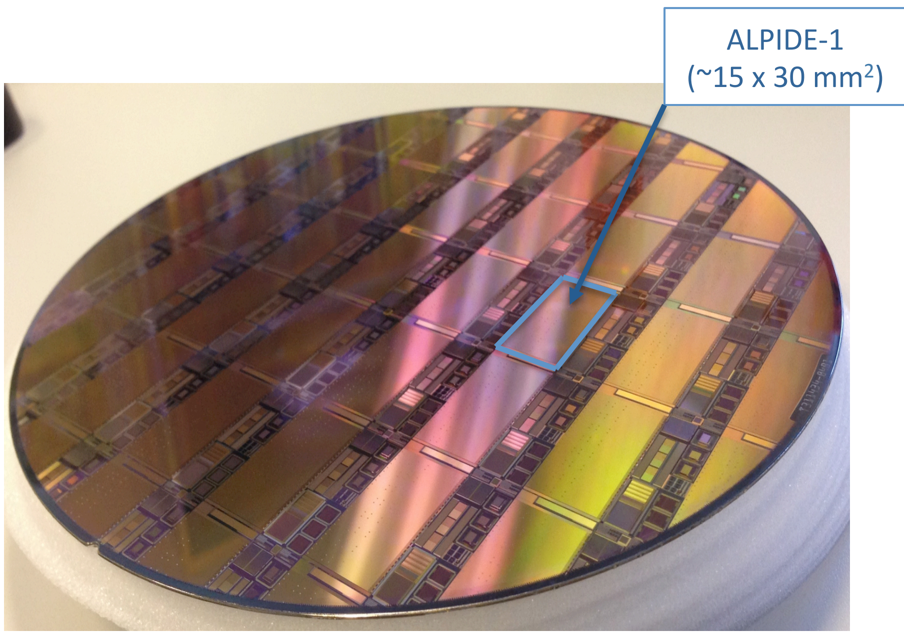


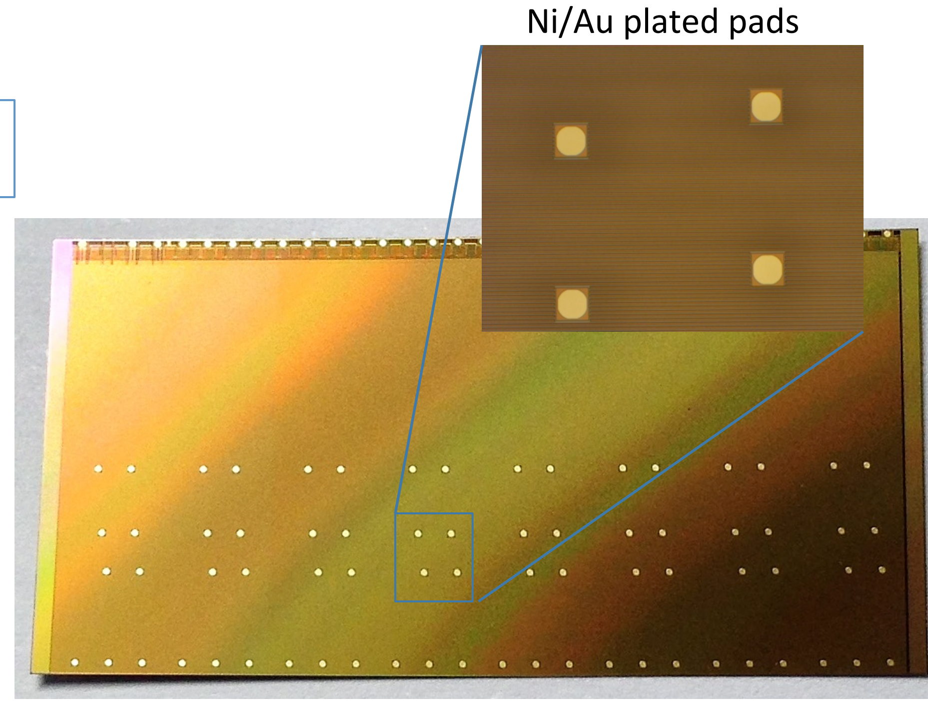
Interconnection of pixel chip to flex PCB

Solder Pads

In order to solder the chip on the flexible printed circuit (FPC), the chip Al pads need to be covered with Ni-Au (wet-able surface)

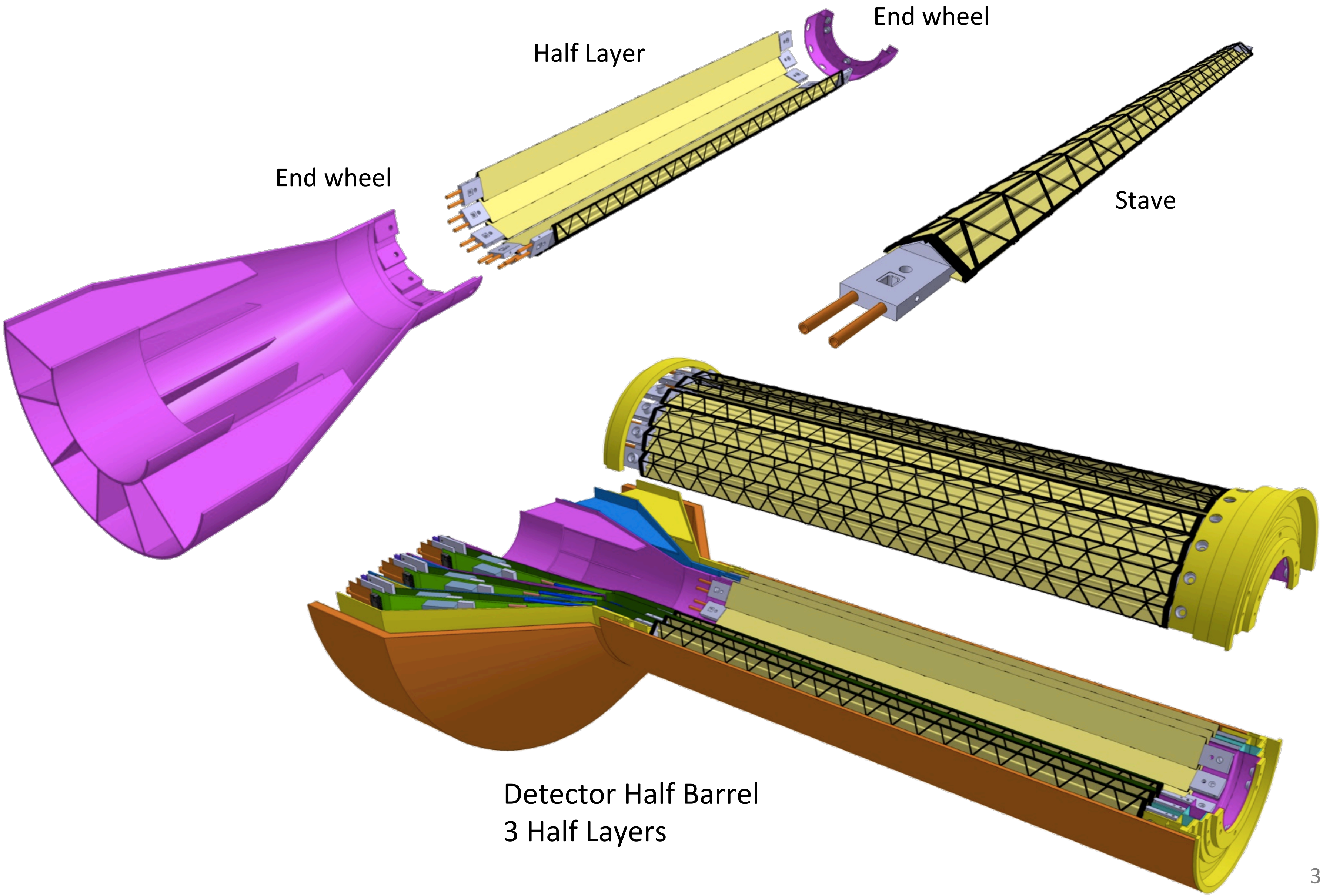
Plating is done on wafers level using electroless Ni-Au plating, prior to thinning and dicing



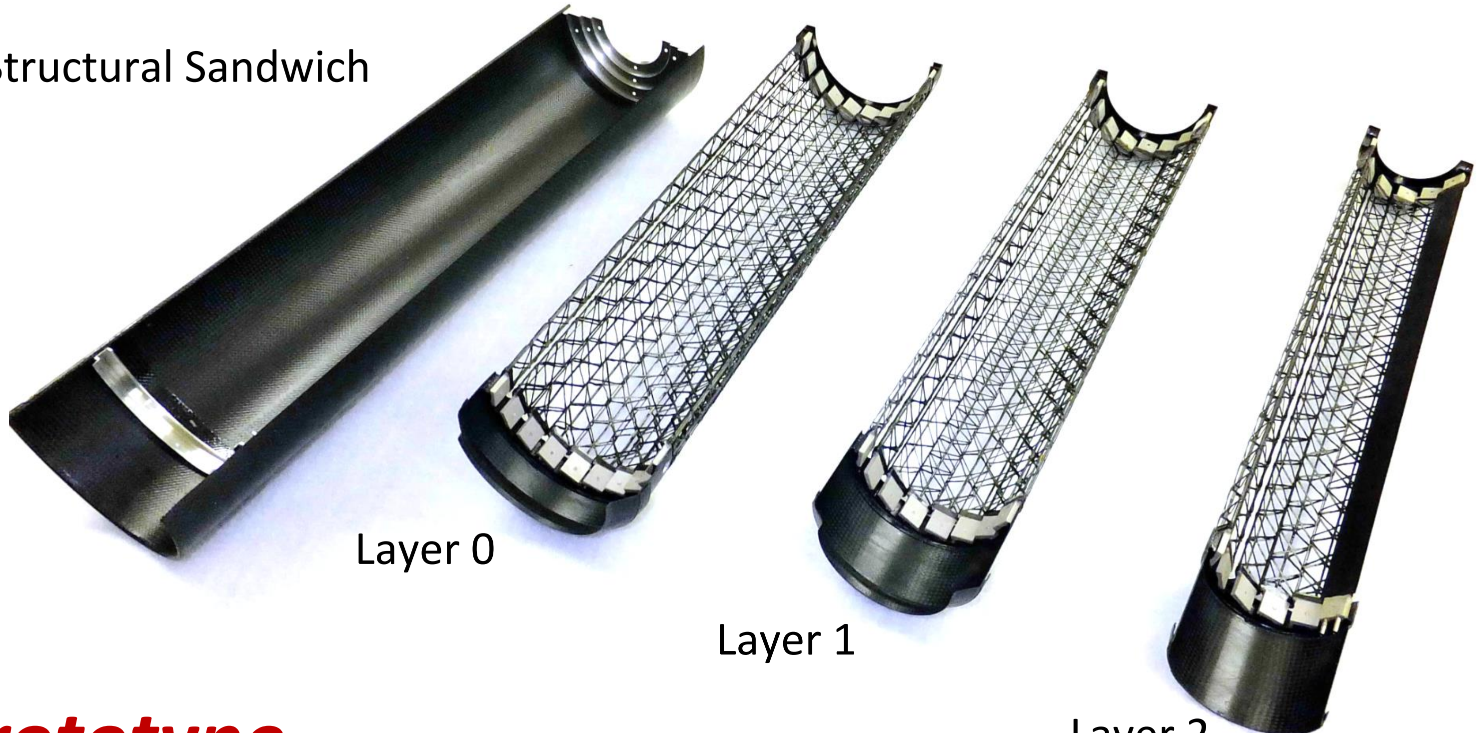


Contact pads are distributed over the matrix (custom designed)

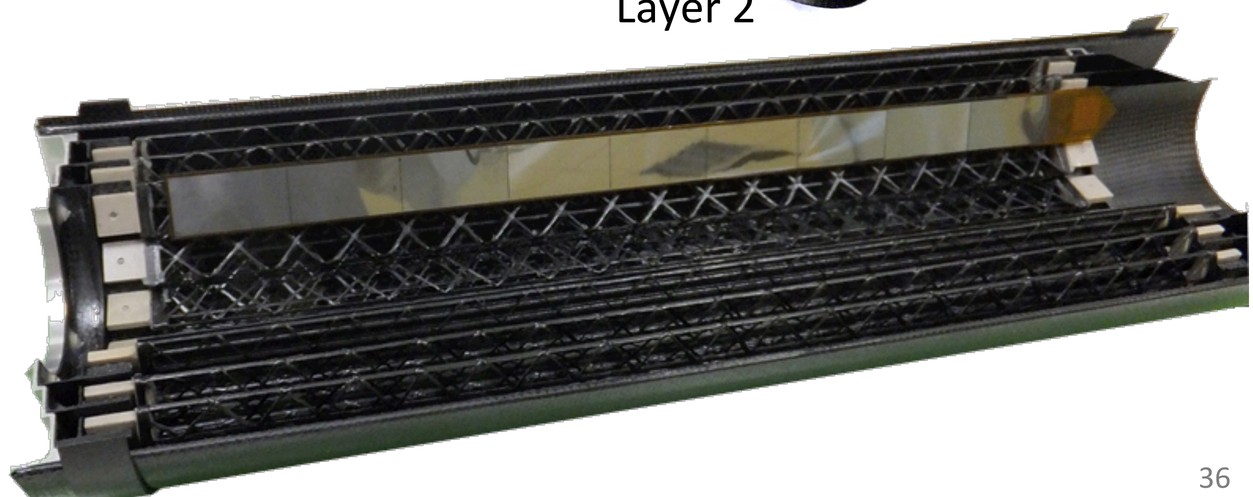
Inner Barrel



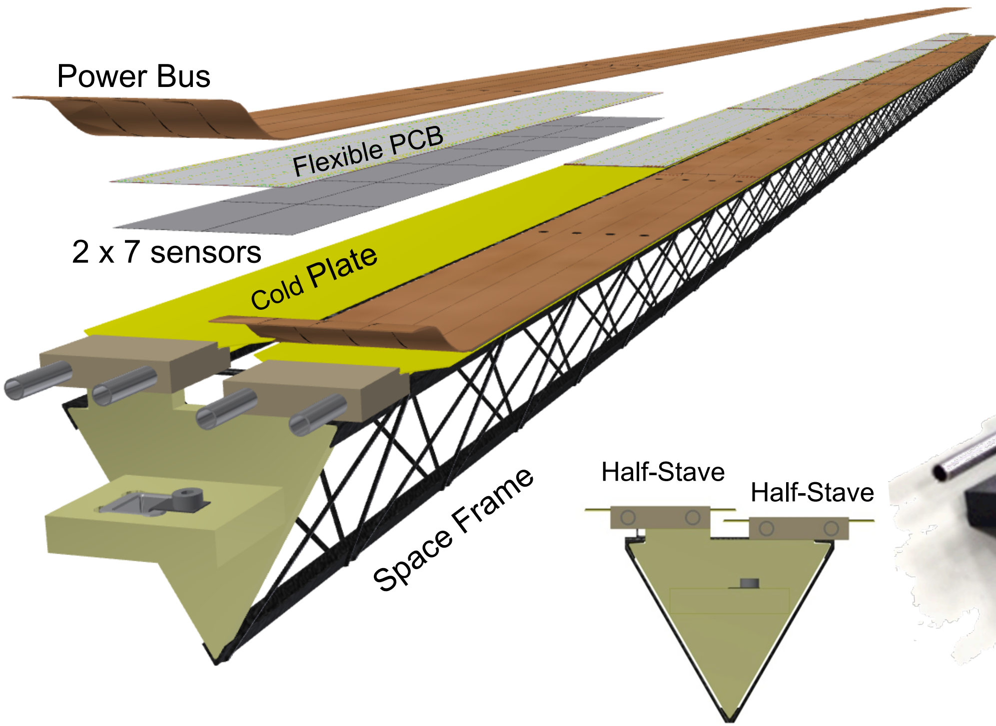
Inner Barrel – full-scale prototype



Prototype



ITS Outer Barrel



Outer Barrel (OB)

<radius> (mm): 194, 247, 353, 405

Nr. staves: 24, 30, 42, 48

Nr. Chips/layer: 6048 (ML), 17740(OL)

Power density < 100 mW / cm^2

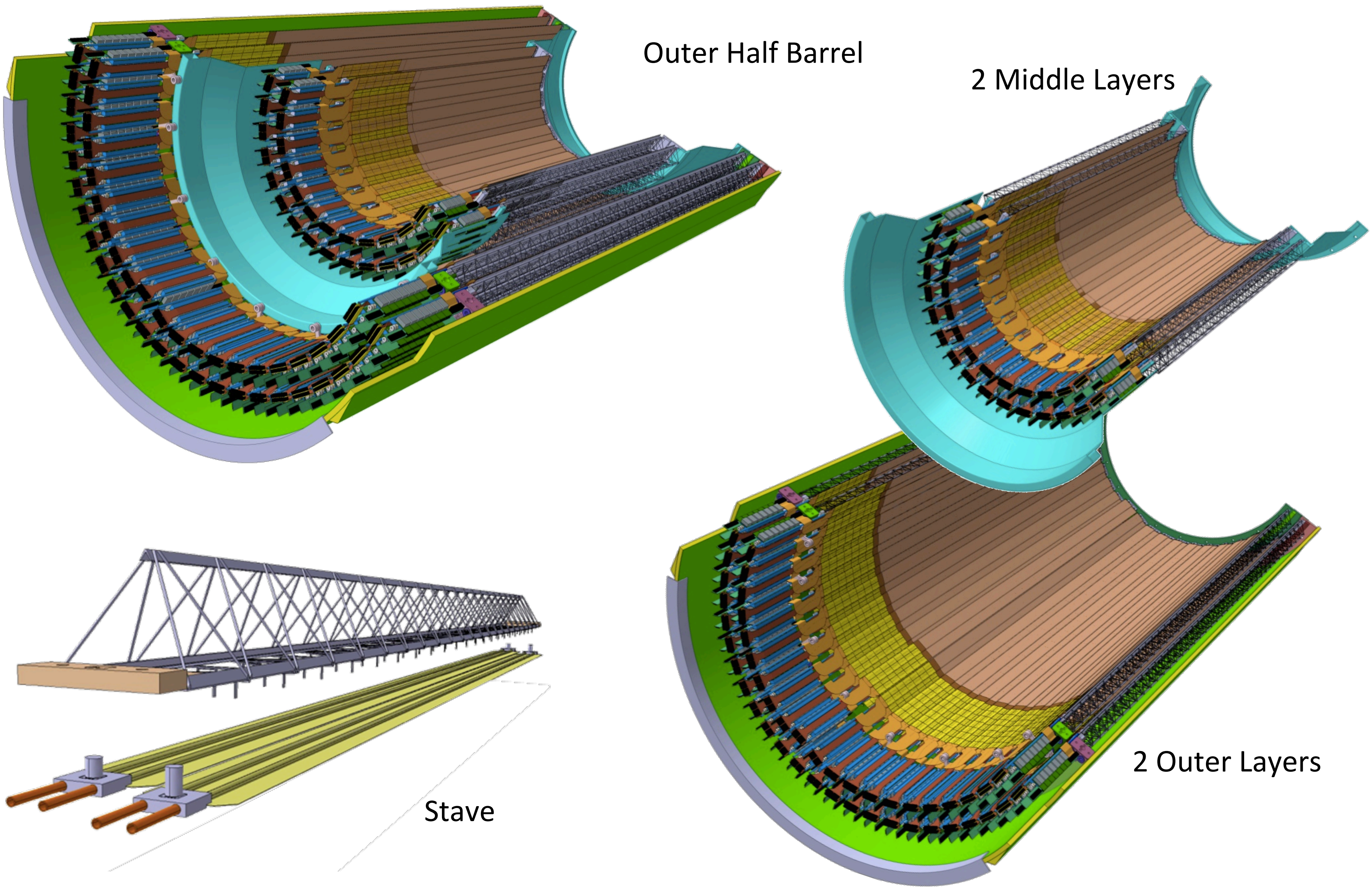
Length (mm): 900 (ML), 1500 (OL)

Nr. modules/stave: 4 (ML), 7 (OL)

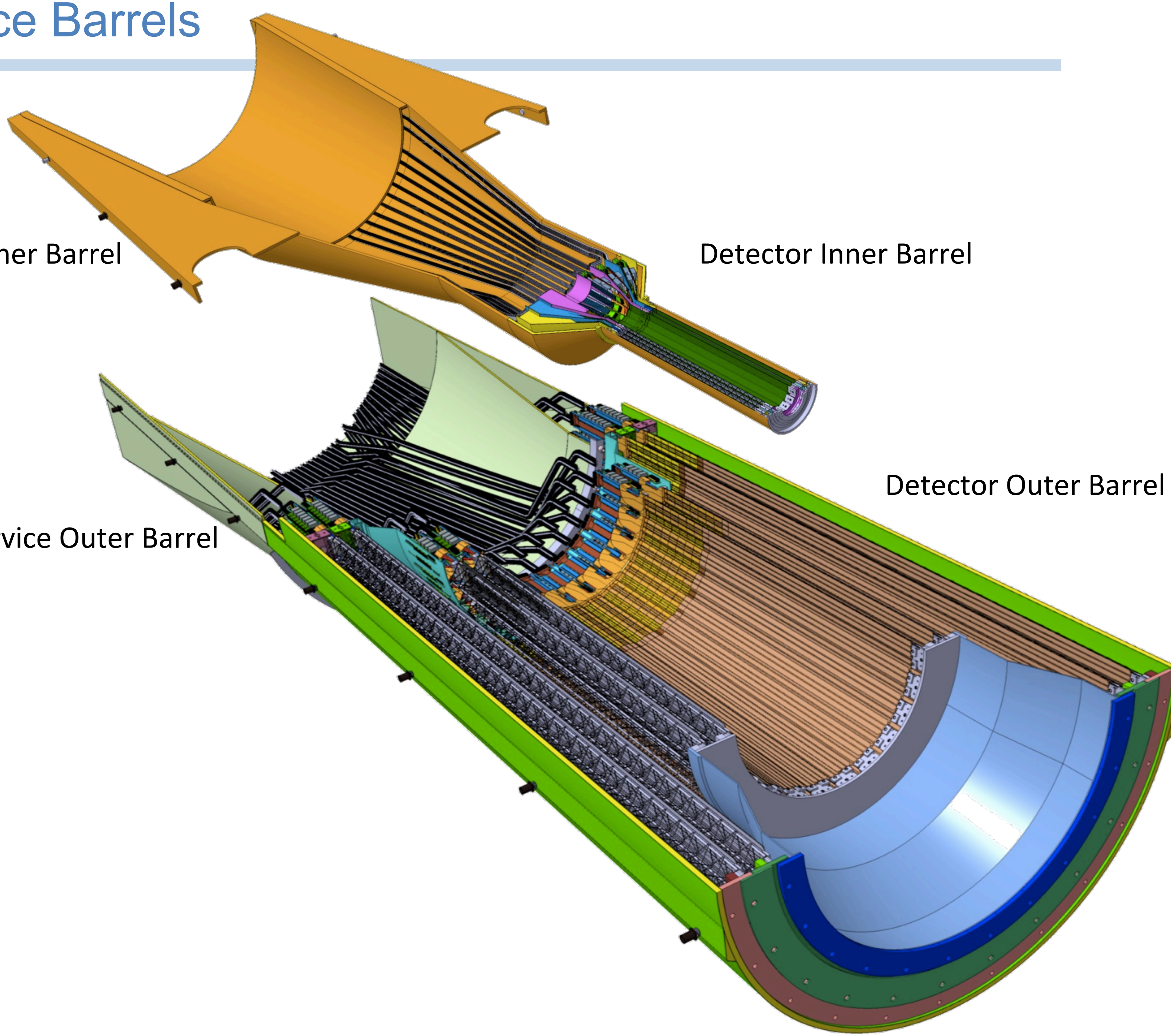
Material thickness: ~ 1% X_0

Throughput (@100kHz): < 3Mb/s × cm^{-2}

ITS Outer Detector Barrel

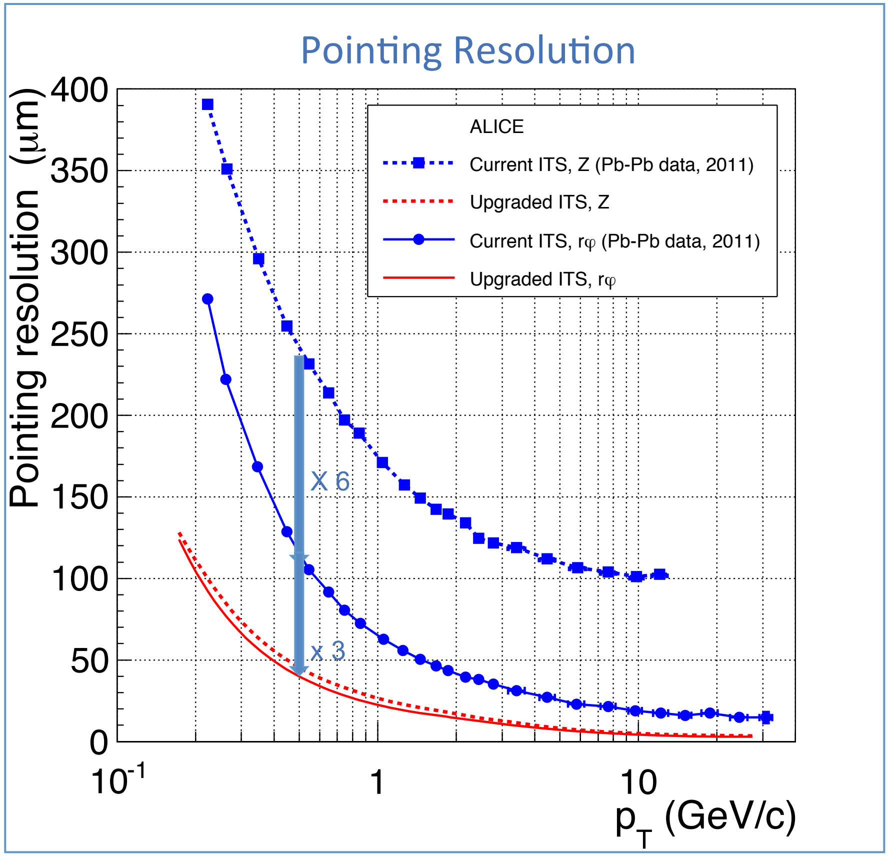


Service Barrels

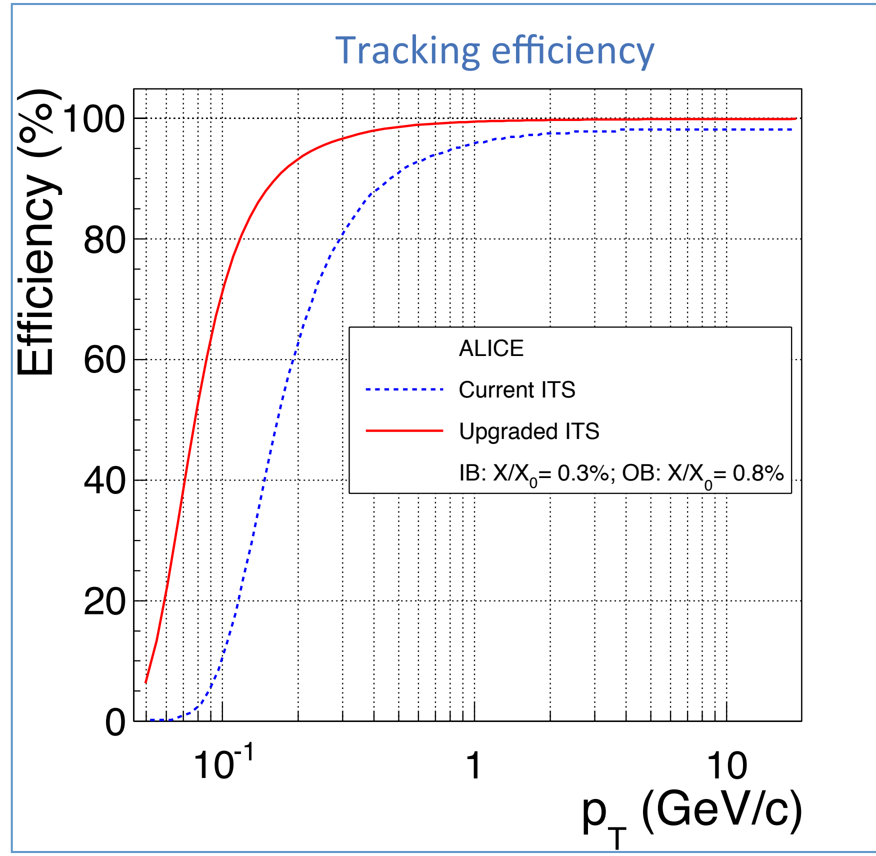


Performance of new ITS (MC simulations)

Impact parameter resolution



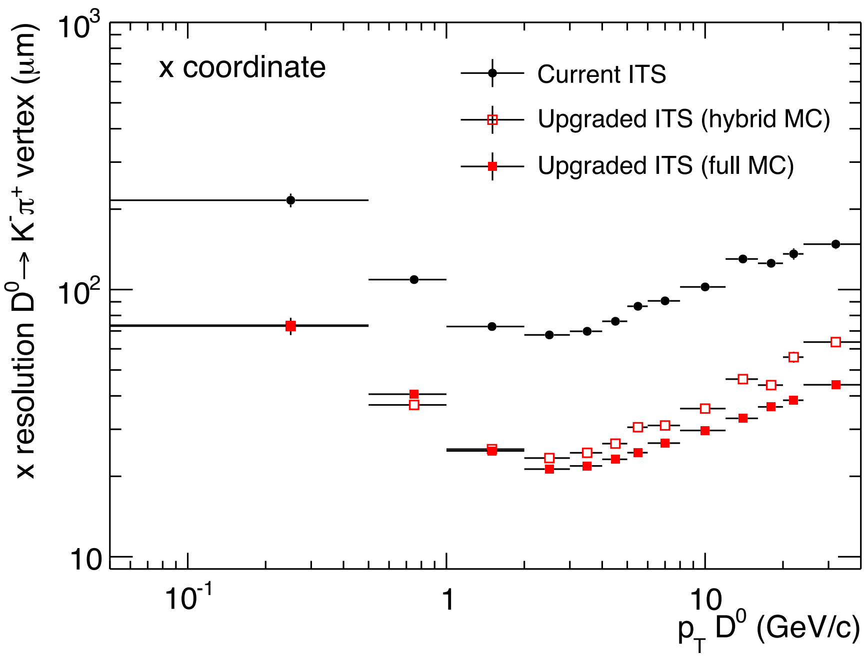
Tracking efficiency (ITS standalone)

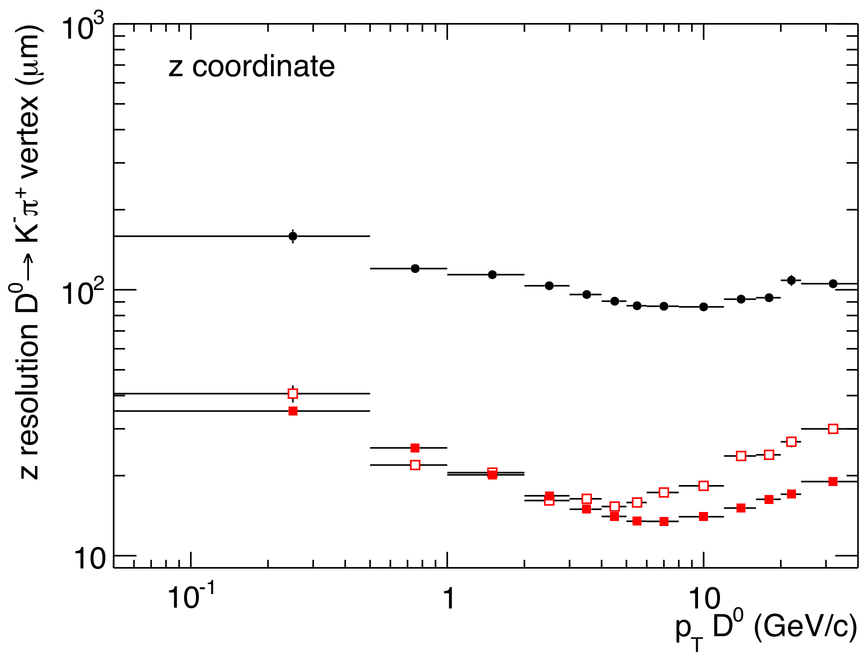


~40 μm at p_T = 500 MeV/c

Performance of new ITS (MC simulation)

$D^0 \rightarrow K^-\pi^+$ secondary vertex position resolution





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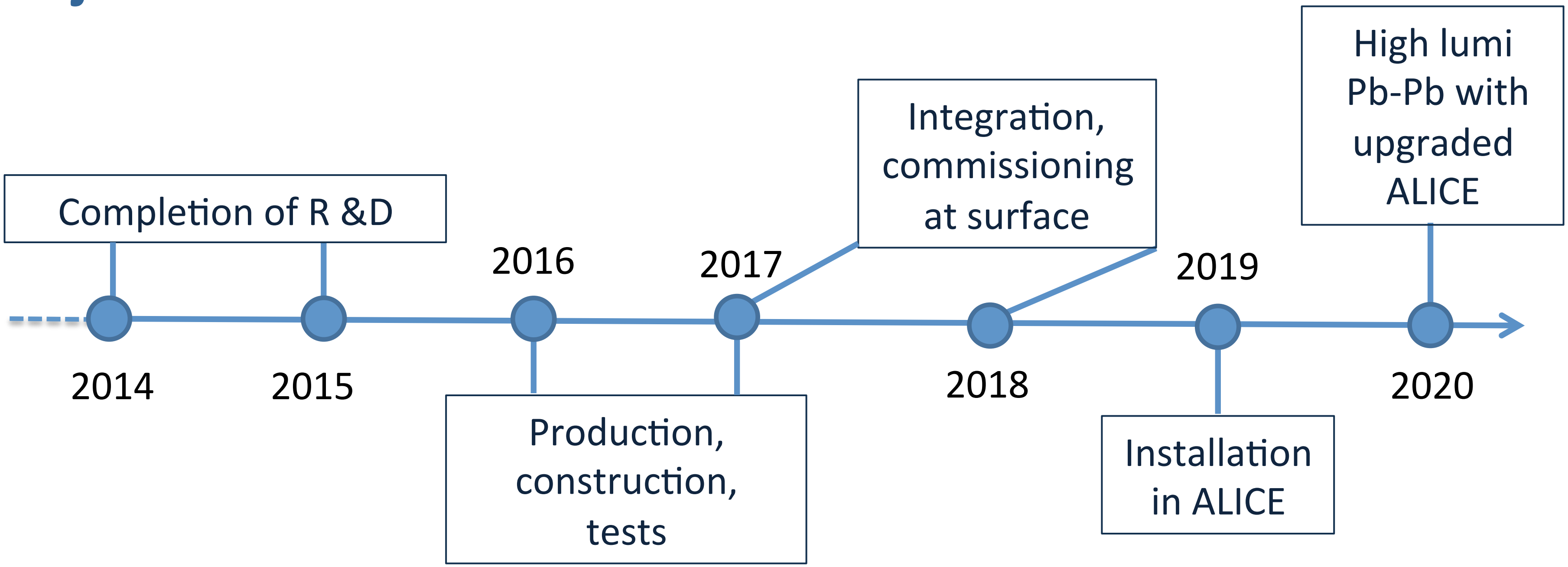
Project Timeline and Collaboration



ALICE ITS Collaboration

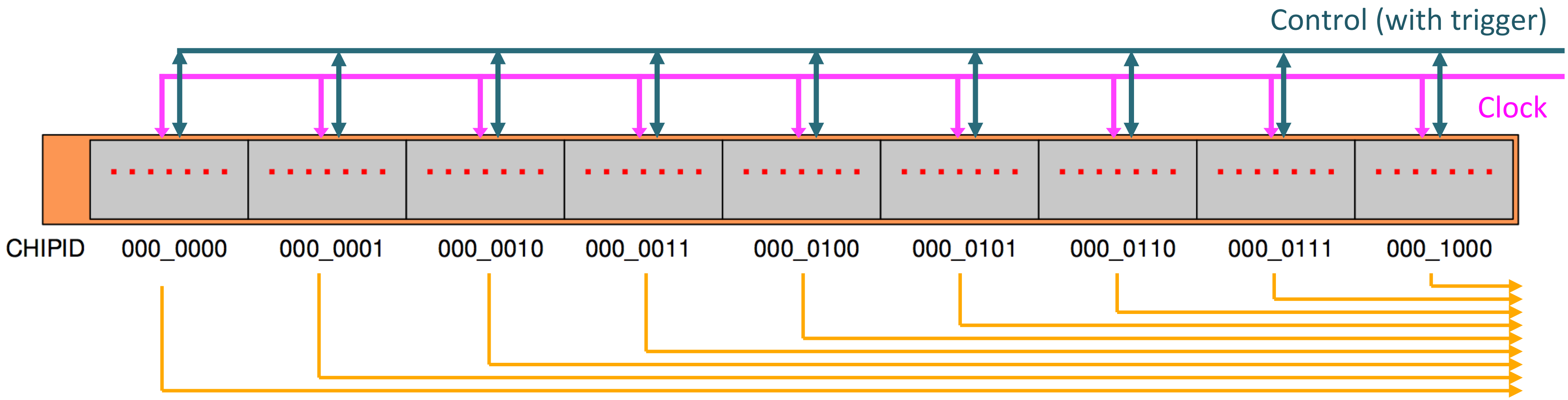
CERN, China (Wuhan), Check Republic (Prague), France (Grenoble, Strasbourg), Italy (Aless., Bari, Cagliari, Catania, Frascati, Padova, Roma, Trieste, Torino), Indonesia (LIPI), Korea (Pusan, Inha, Yonsei), Netherlands (Nikhef, Utrecht), Pakistan (CIIT-Islamabad), Russia (St. Petersburg), Slovakia (Kosice), Thailand (Suranaree, SLRI, TMEC), UK (Daresbury, Liverpool, RAL), Ukraine (Kharkov), USA (Austin, Berkeley)

Institute = participated in current ITS

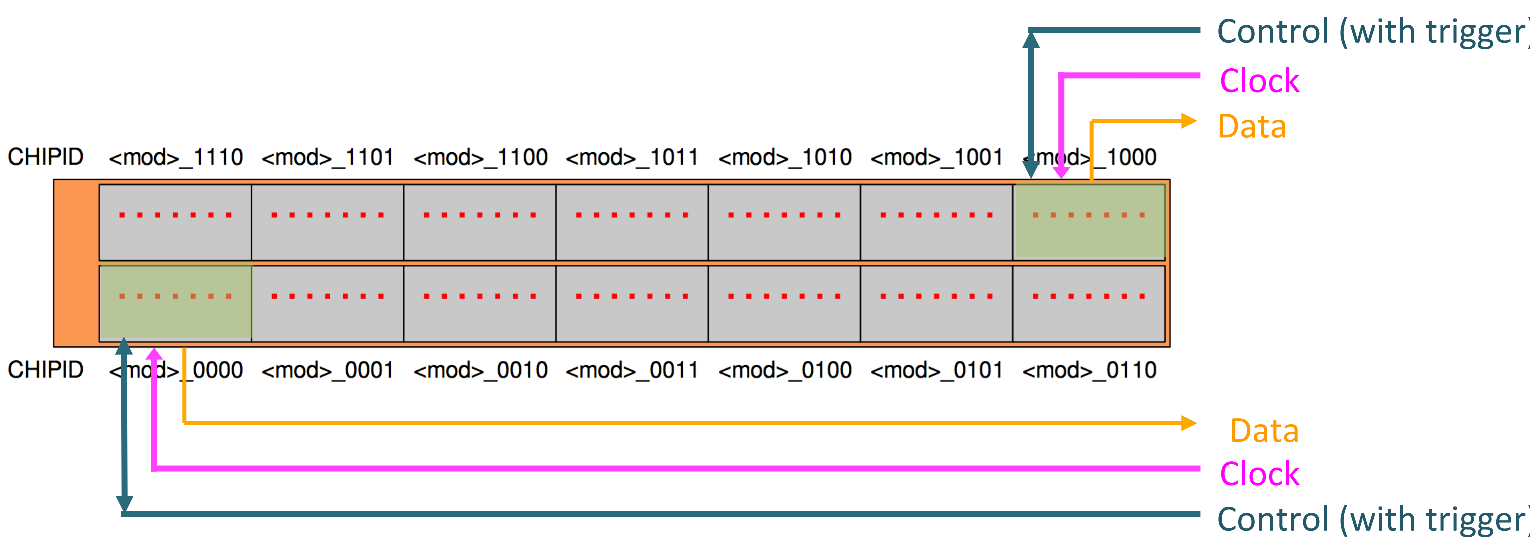
SPARES

Readout – Inner and Middle/Outer Layers connections

Inner layers stave, 9 independent sensors (each read/drives its own data lines)

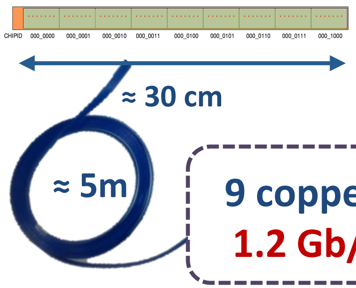


Mid/Outer layers module: 2 symmetric group of 1 master and 6 slave chips. Only the master accesses the data/control lines toward/from the outer world.



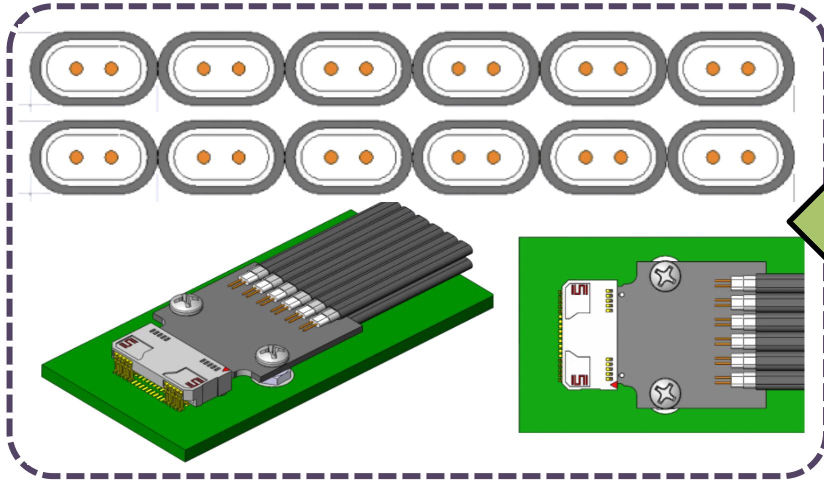
Readout – copper links and available bandwidth

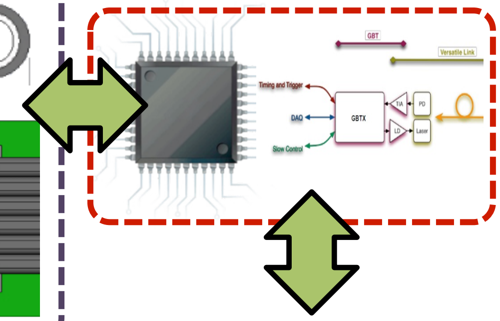
Inner layers (0, 1, 2) staves:
9 masters for each stave



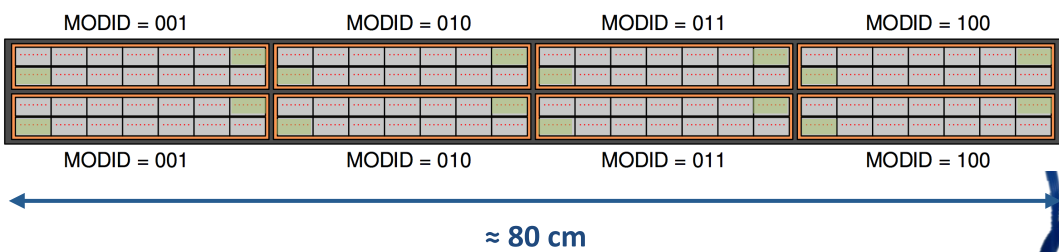
9 copper pairs,
1.2 Gb/s each

12 pairs Twinax copper assembly



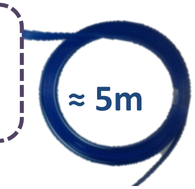


Mid layers (3, 4) staves: 8 modules per stave, 2 master each

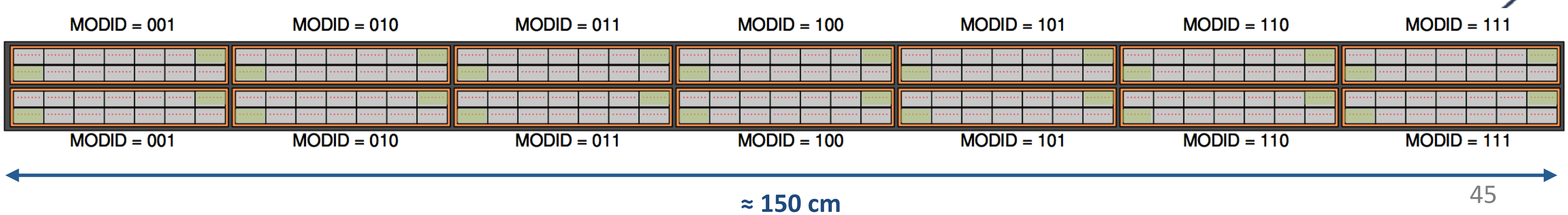


16 copper pairs,
400 Mb/s each

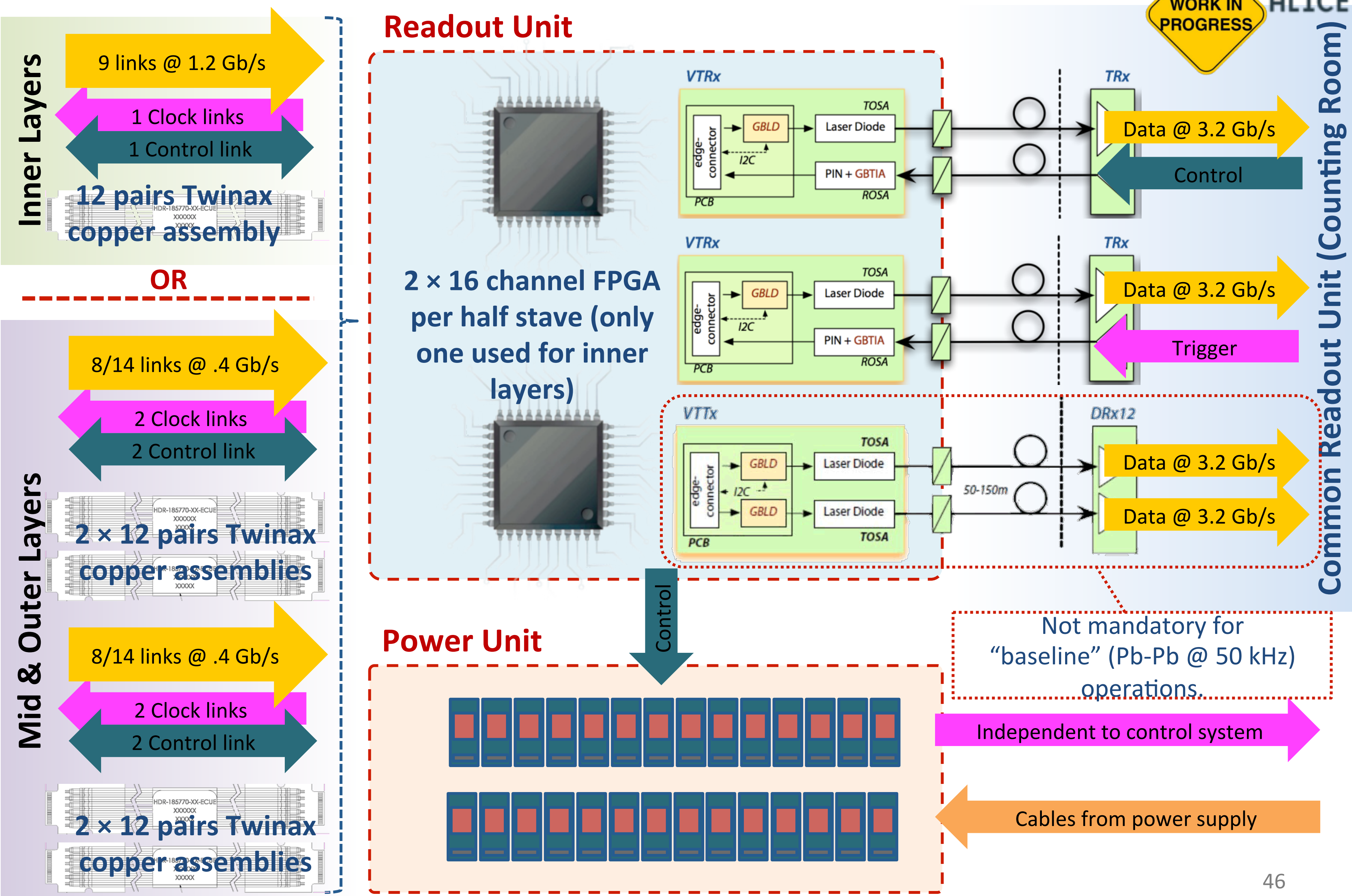
28 copper pairs,
400 Mb/s each



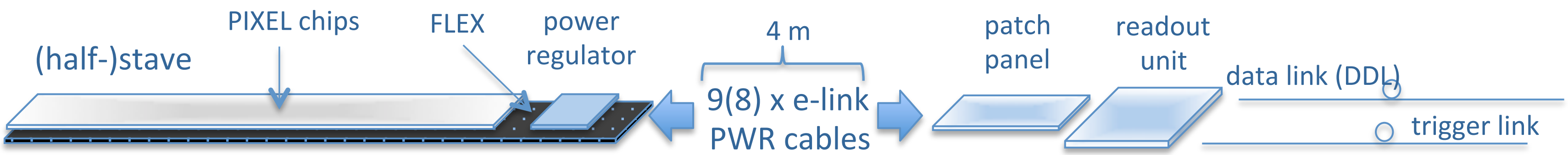
Outer layers (5, 6) staves: 14 modules per stave, 2 master each



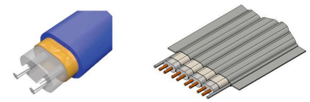
Readout – copper links and available bandwidth



Readout – general scheme and data throughput

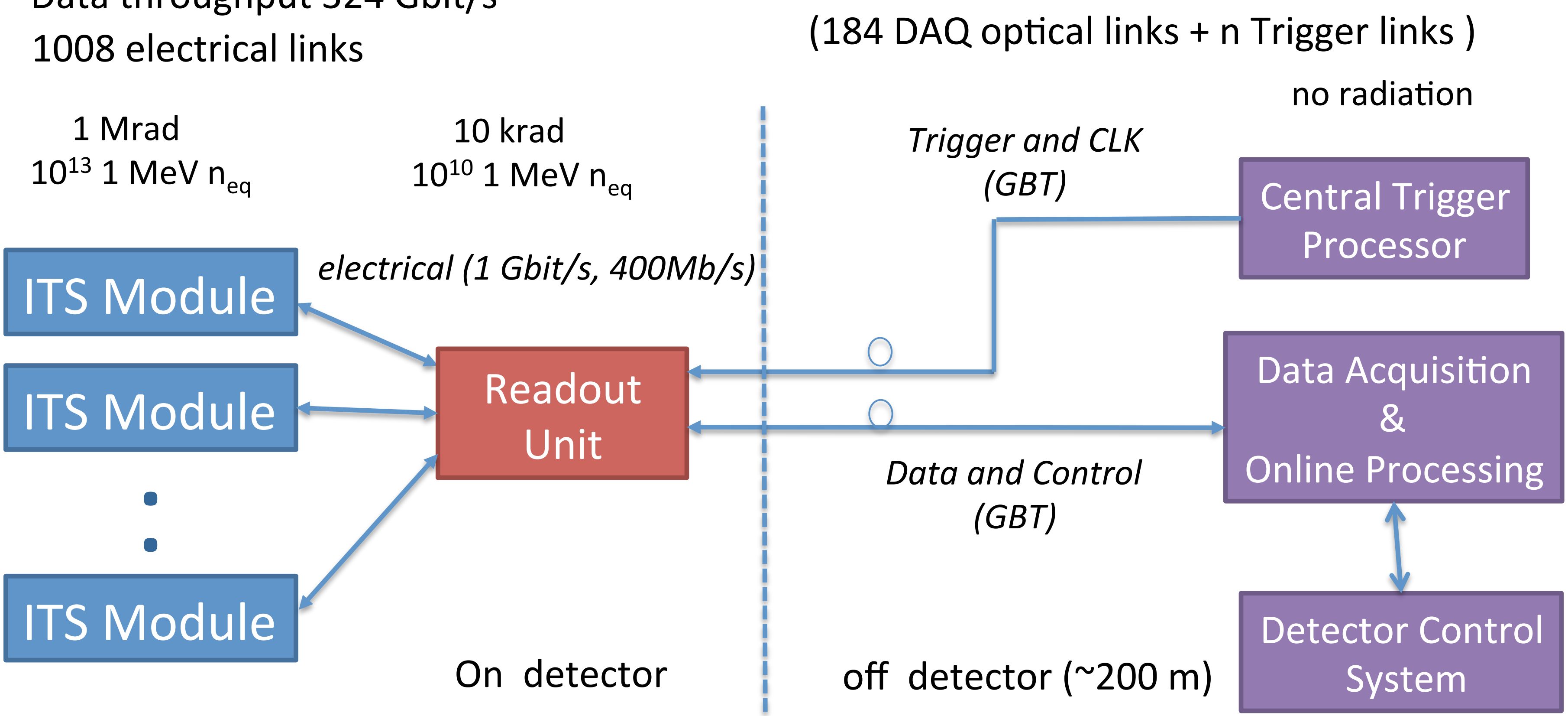


Schematic representation of the readout path

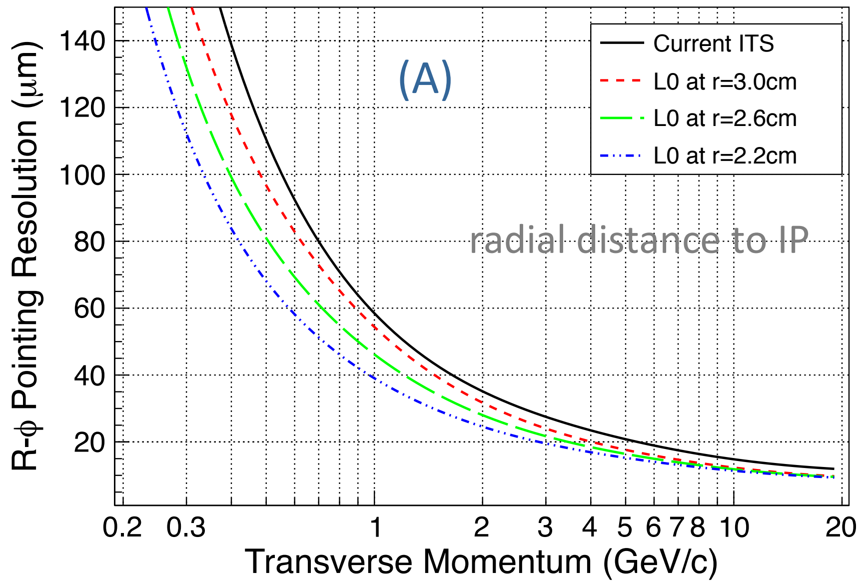


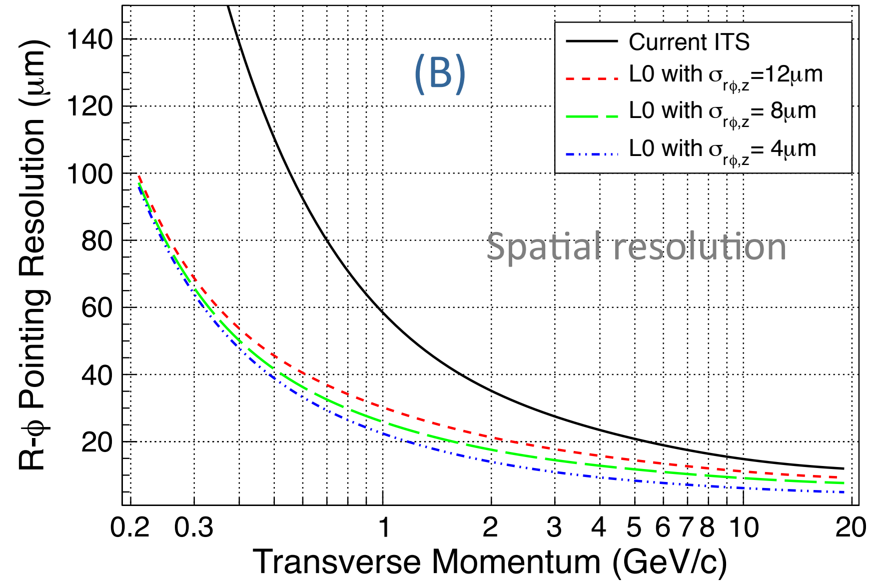
SAMTEC twinax "Firefly"

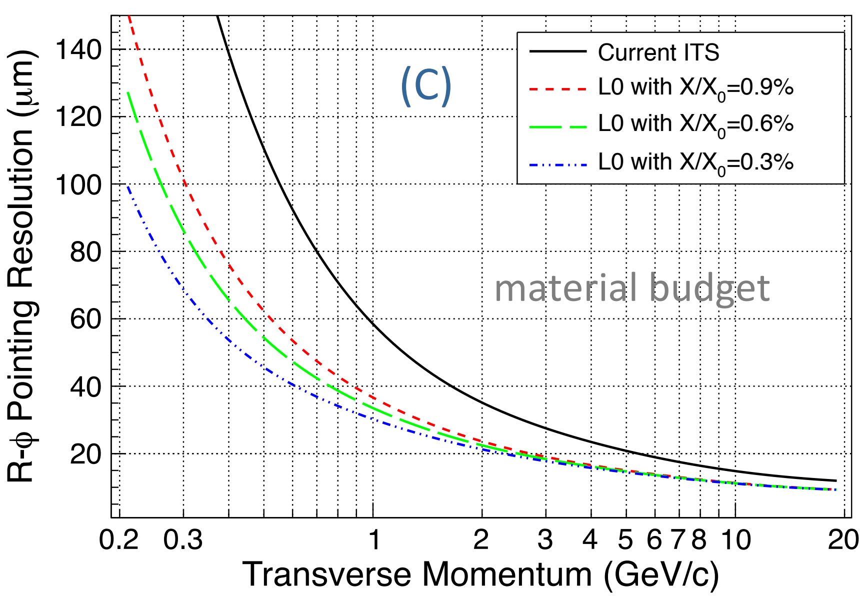
Data throughput 324 Gbit/s
1008 electrical links



Impact parameter studies (ALICE ITS Upgrade)





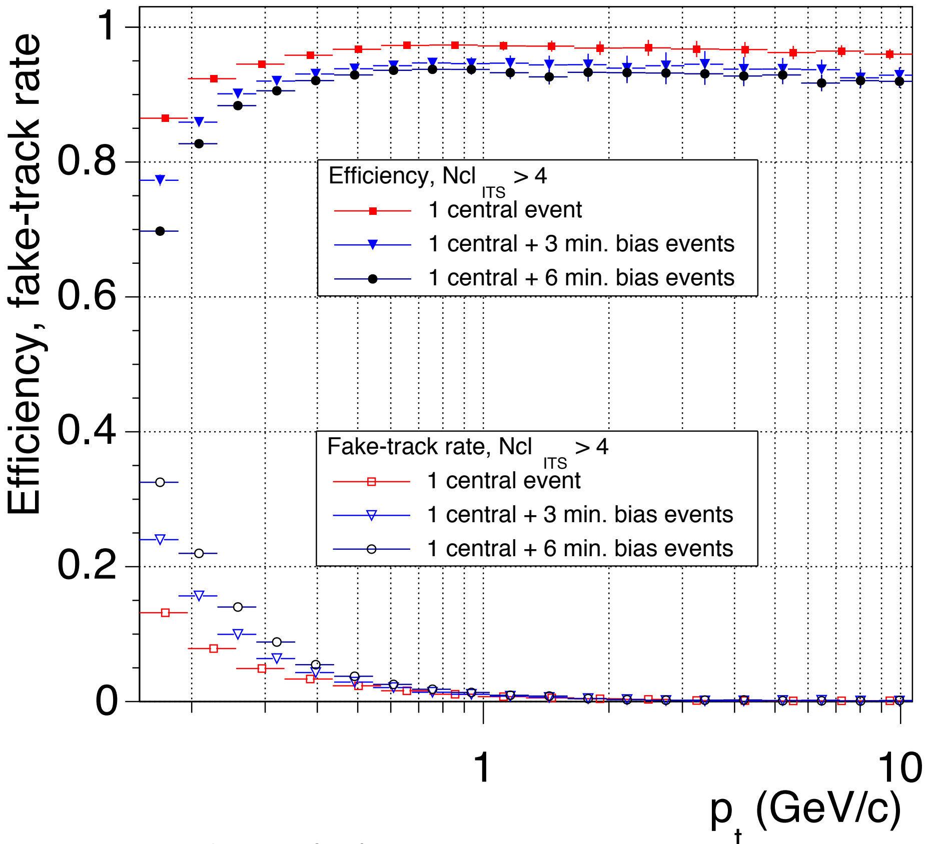


- Current ALICE ITS
  - ✧ radial position of first layer: 39mm
  - ✧ x/X_0: 1.14% per layer
  - ✧ spatial resolution (r-phi): 12 μm
- A) current ITS + L0: x/X0 = 0.3%, res.=4μm;
- B) current ITS + L0: r = 22mm, x/X_0 = 0.3%;
- C) current ITS + L0: r = 22mm, x/X_0 = 0.3%;

ALICE ITS Upgrade CDR, CERN-LHCC-2012-12

Performance of new ITS (MC simulations)

Matching efficiency between the tracks reconstructed in the upgraded ITS and TPC for different values of event pile-up



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The average event pile-up depends on the interaction rate and detector integration time

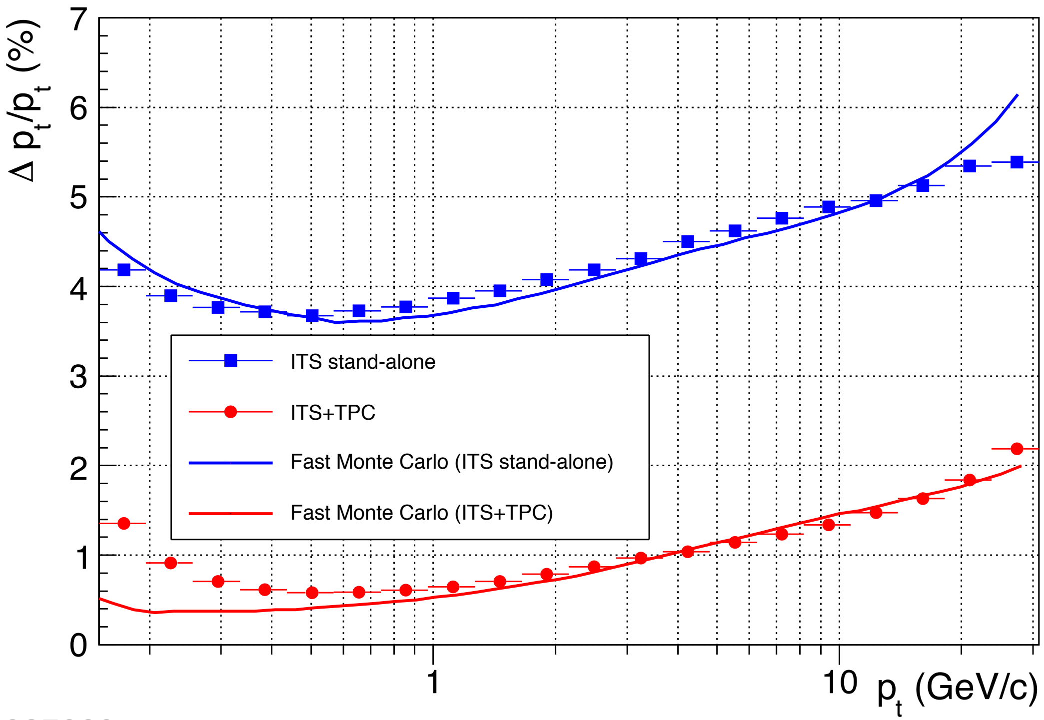
interaction rate 50 kHz
integration time: 4 – 30 μs

For 30 μs integration time (worst case design):

<pile-up> = 1 central + 1.5 min. bias

Performance of new ITS (MC simulations)

MOMENTUM RESOLUTION



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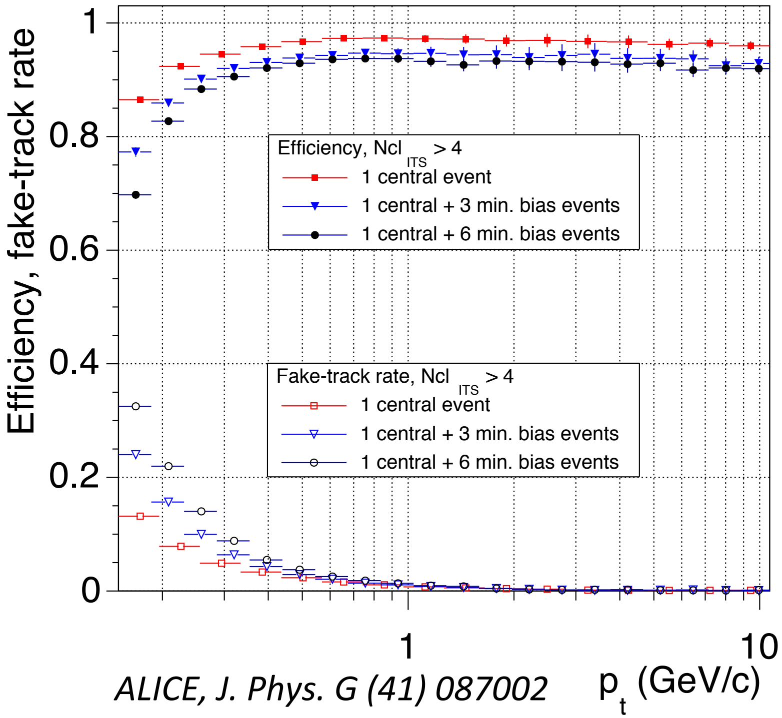
Transverse momentum resolution as function of p_T for primary charged pions for the upgraded ITS and current ITS. The results are shown for ITS standalone and ITS-TPC combined tracking.

How integration time and pile-up affect performance

ALICE ITS Upgrade



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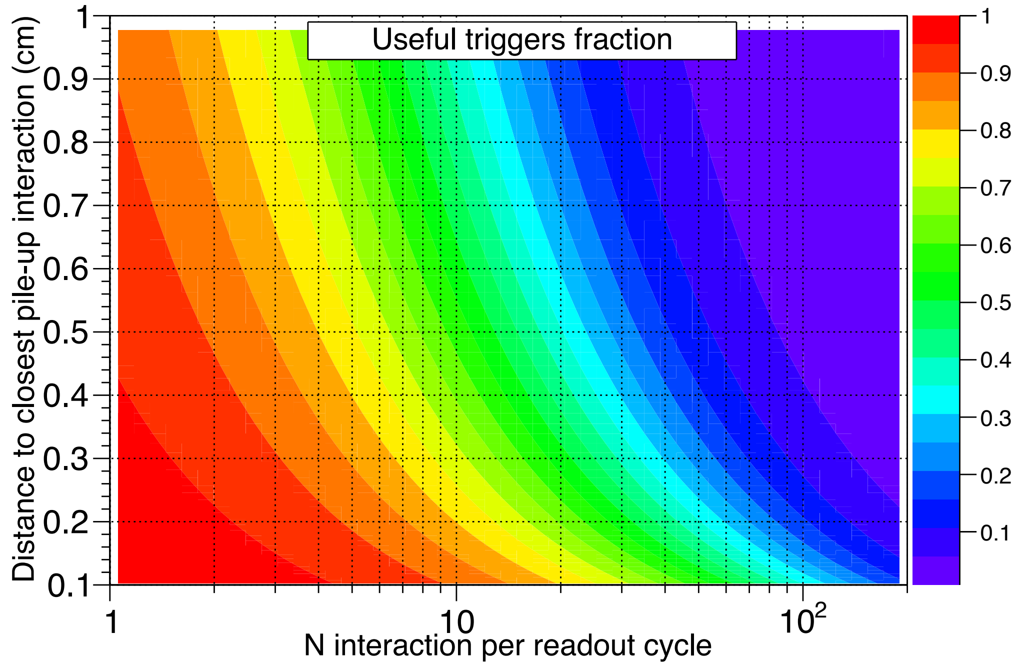
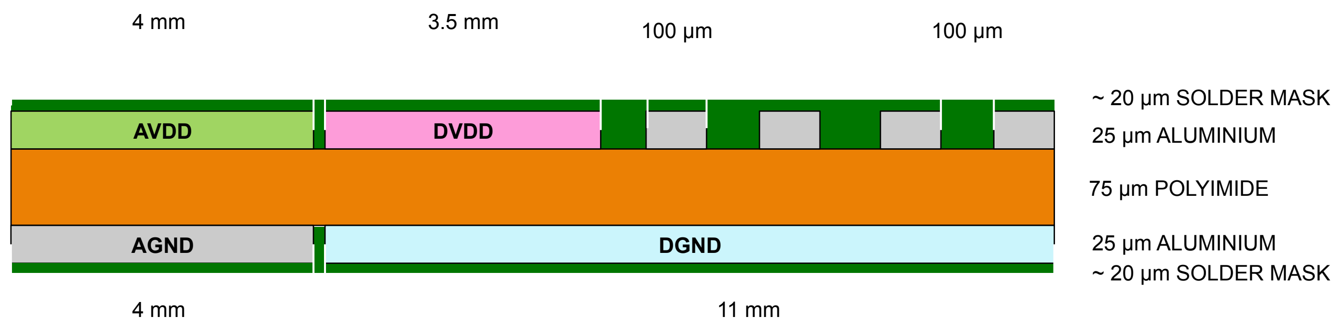


At 50 kHz Pb-Pb interaction rate
<pile-up> @ 20 μs integration time: 1 central + 1 minimum bias

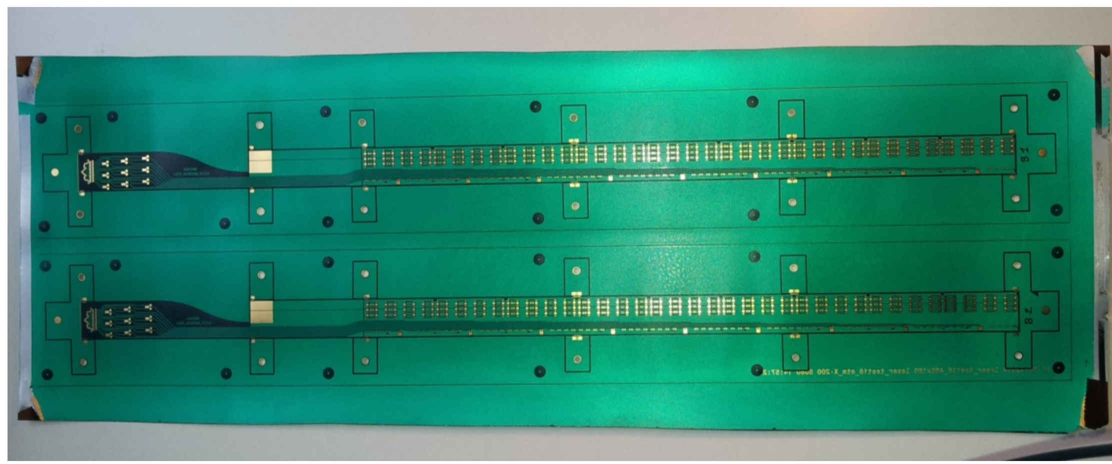
At 200 kHz pp interaction rate
<pile-up> @ 20 μs integration time: 5 interaction

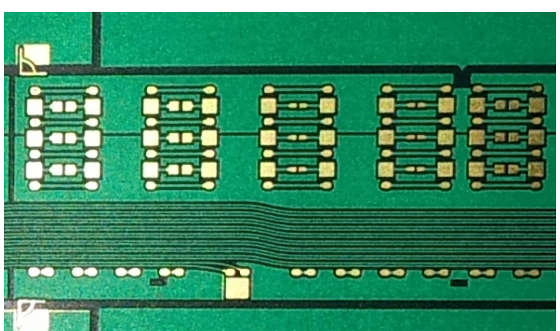
FPC main characteristics

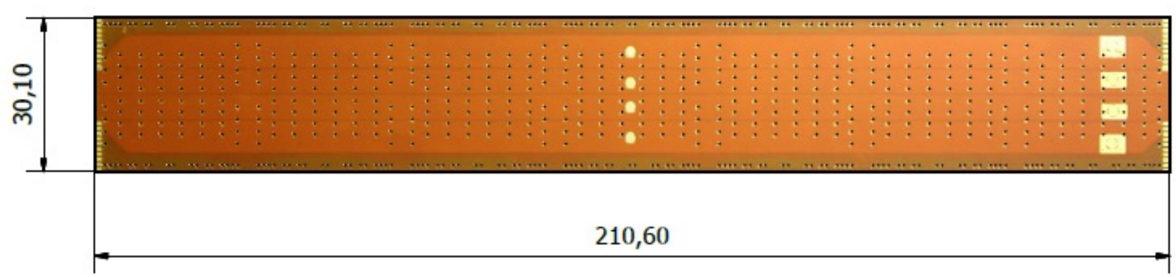
Flexible Printed Circuit



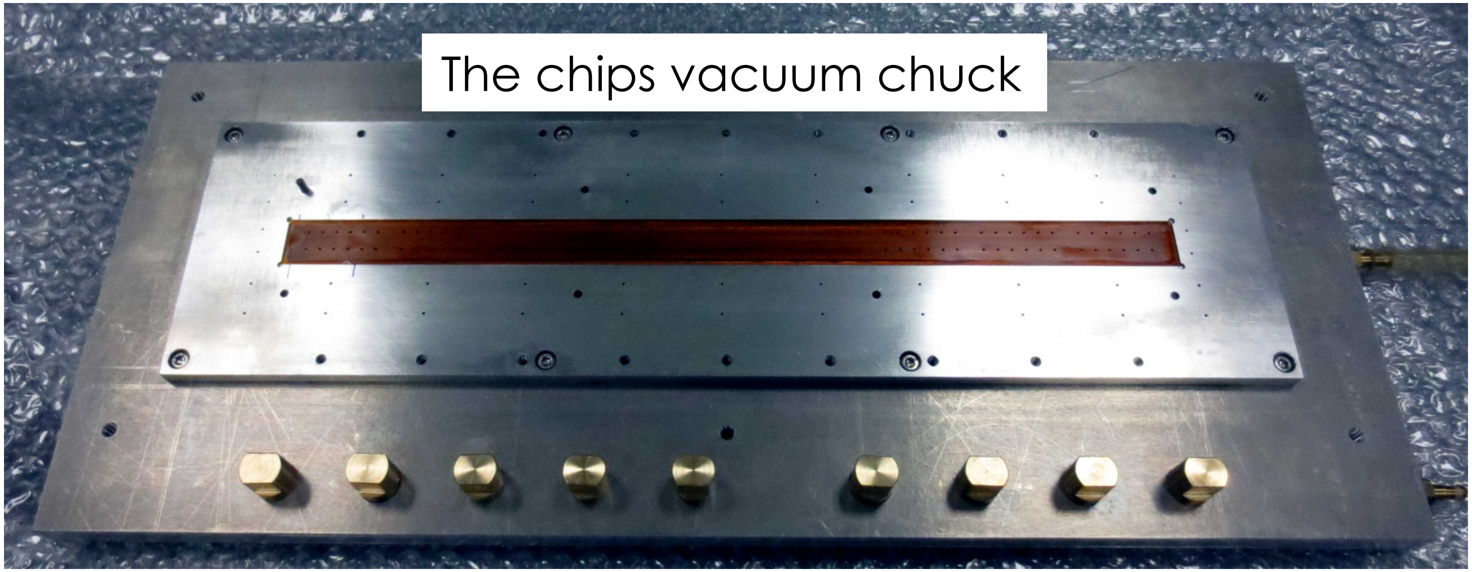
- 2 layouts:
  - IB: 1x9 chips, Al
  - OB: 2x7 chips, Cu
- Metallised vias of 220 mm diameter
- Two openings of 1x1 and 1x0.4 mm^2, respectively, to “see” chip targets

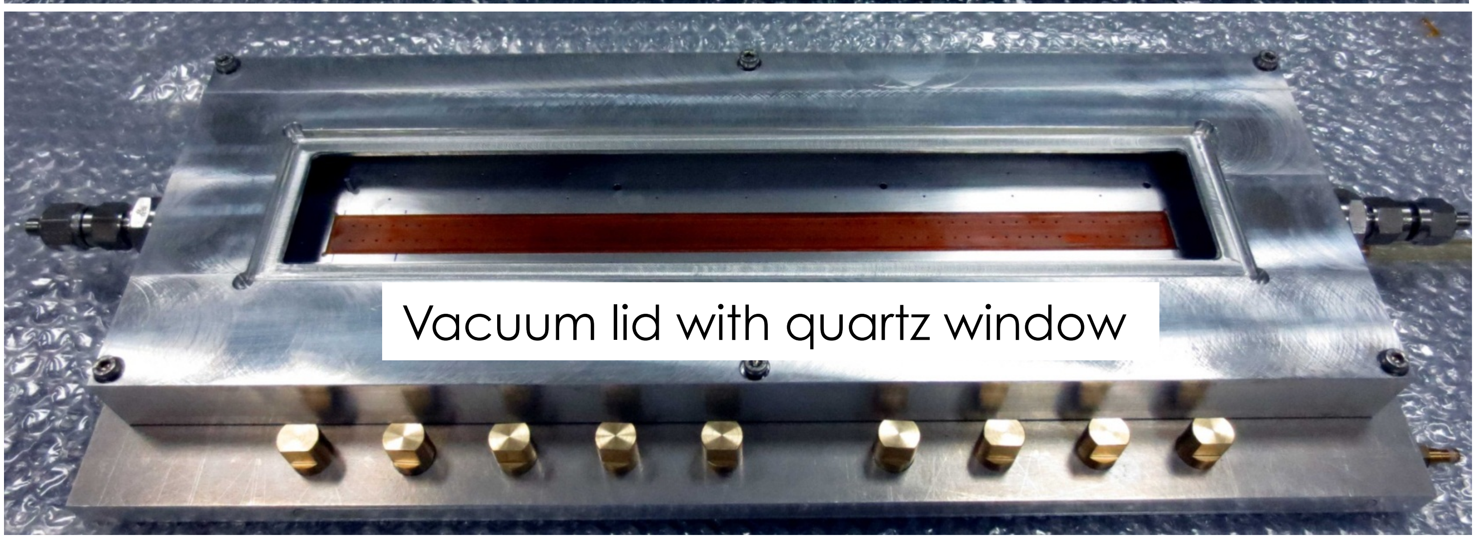




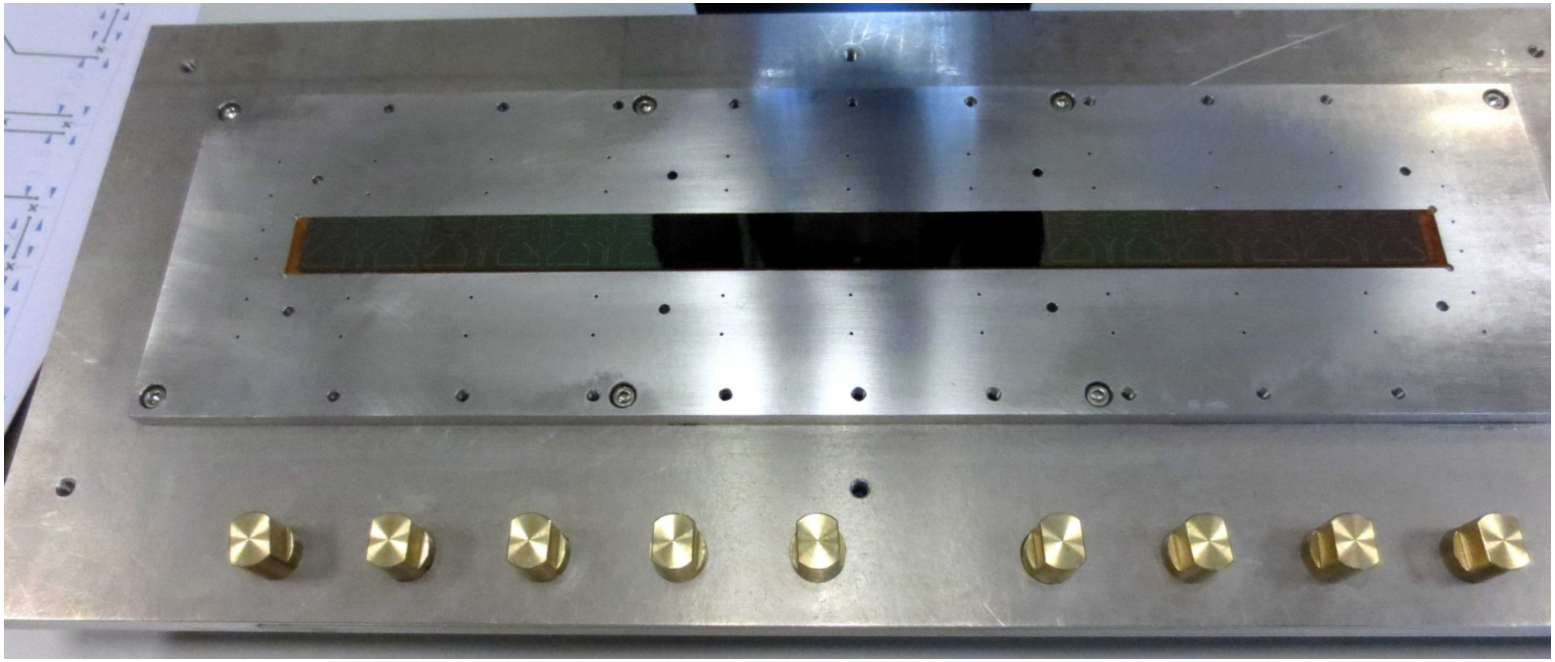


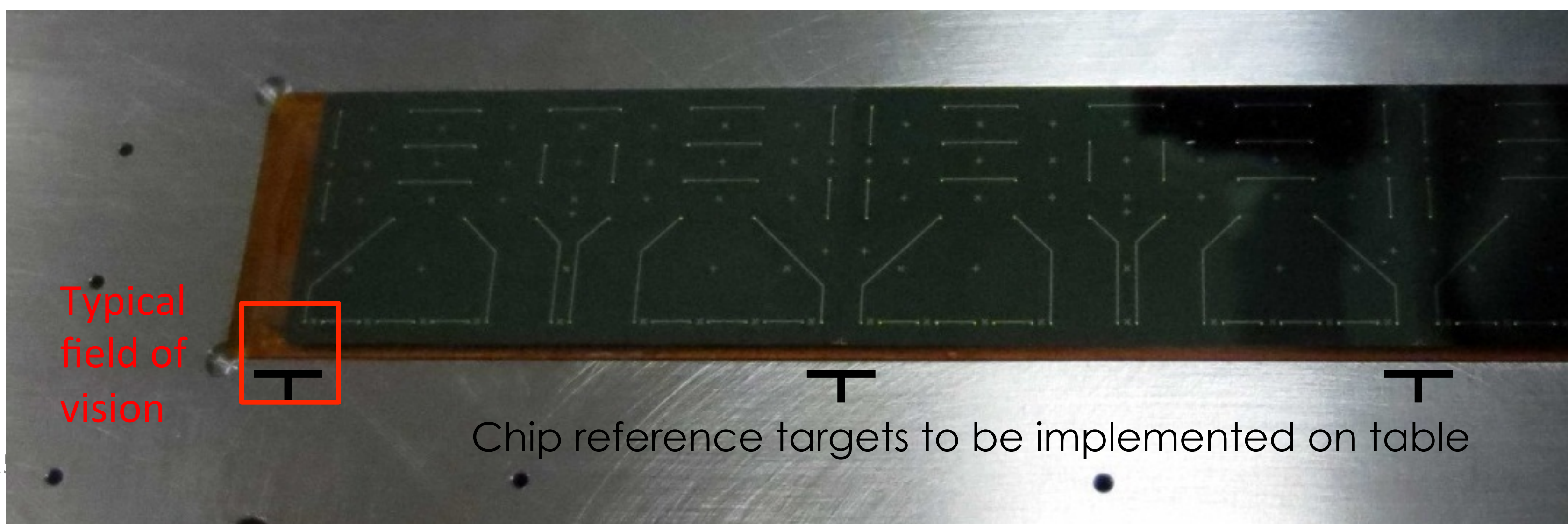
HIC assembly - the IB work table



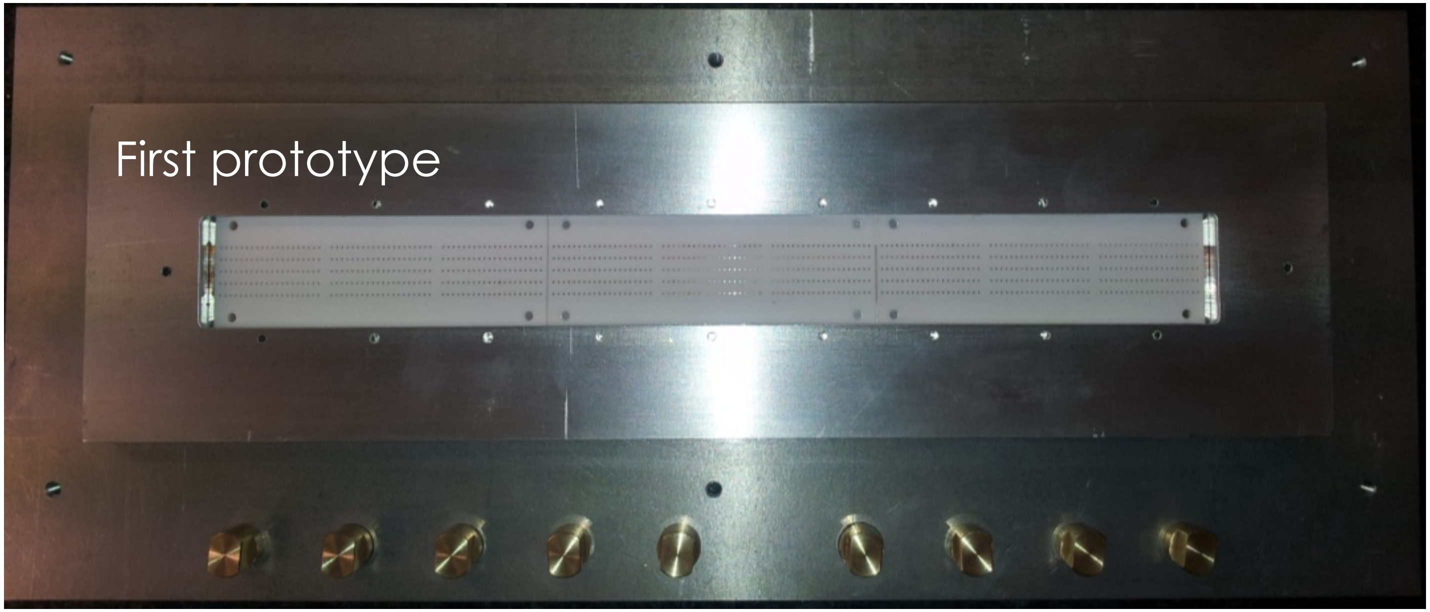


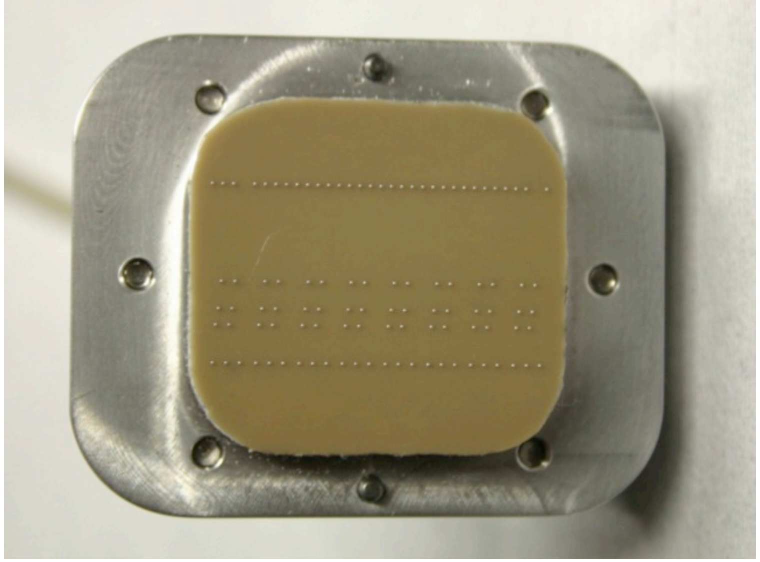
HIC assembly - aligned pad chips



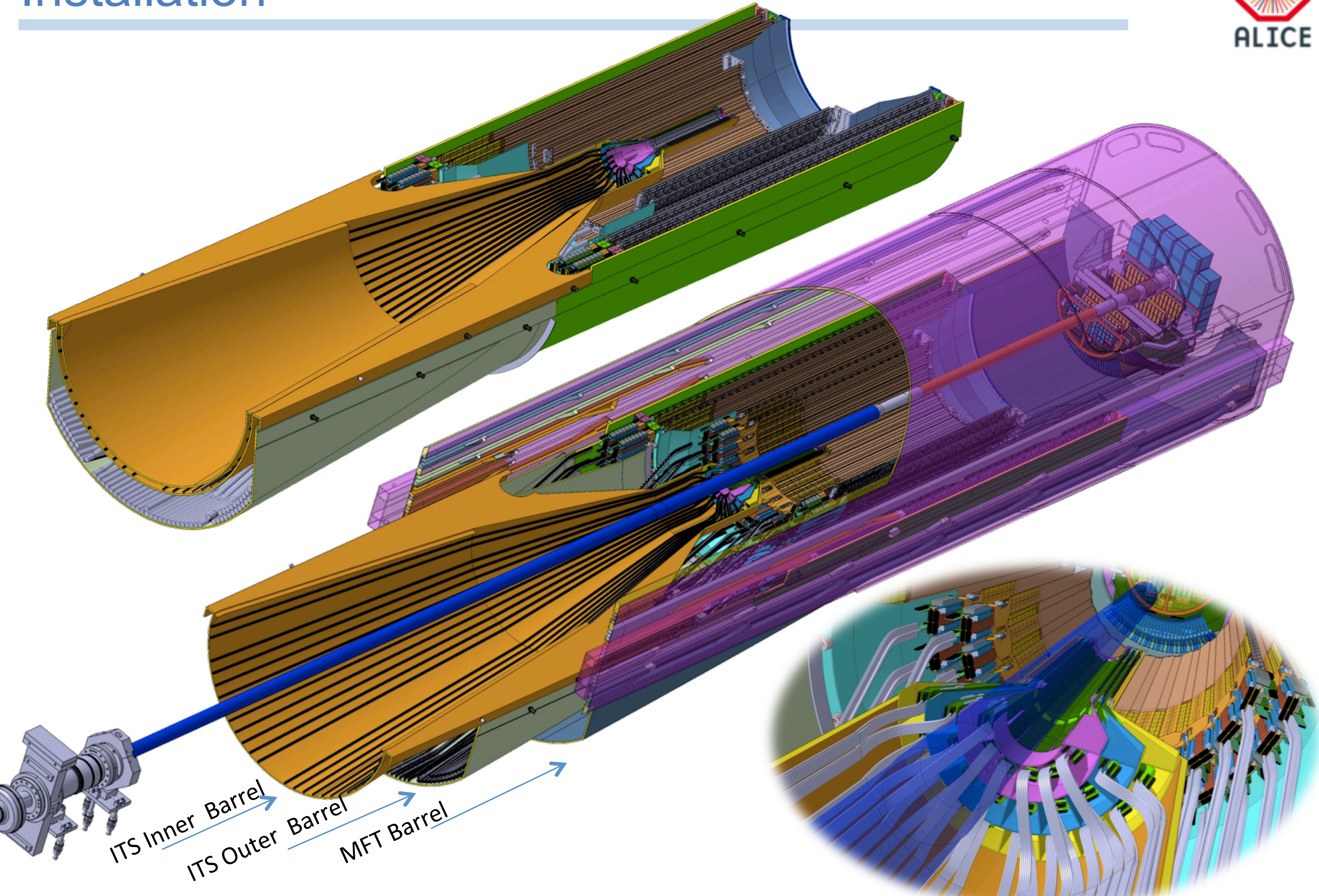


The soldering mask and ball transfer tool



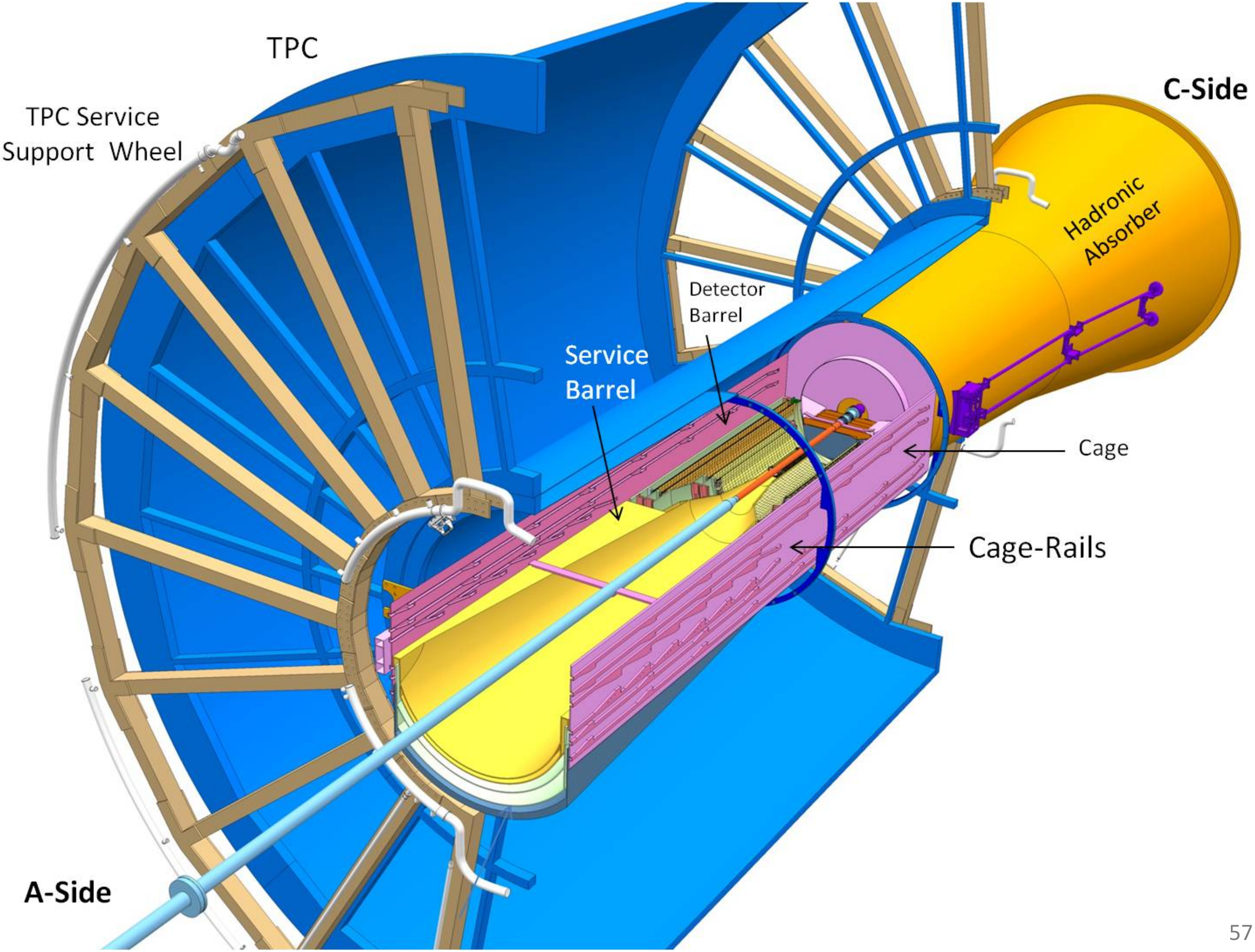


Installation



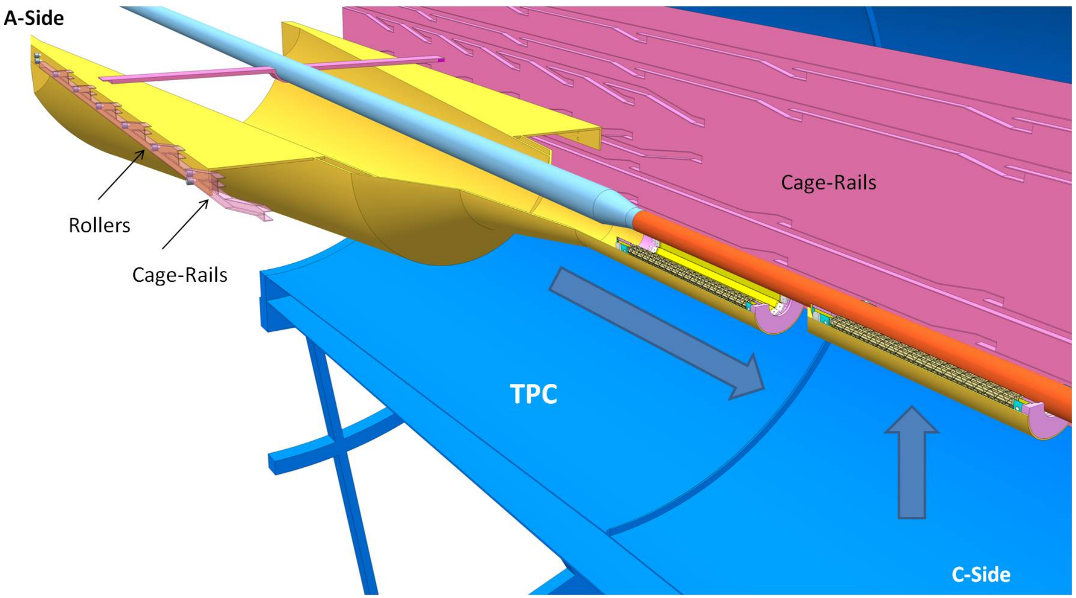
Independent insertion of the ITS Inner and Outer half barrels along the beampipe

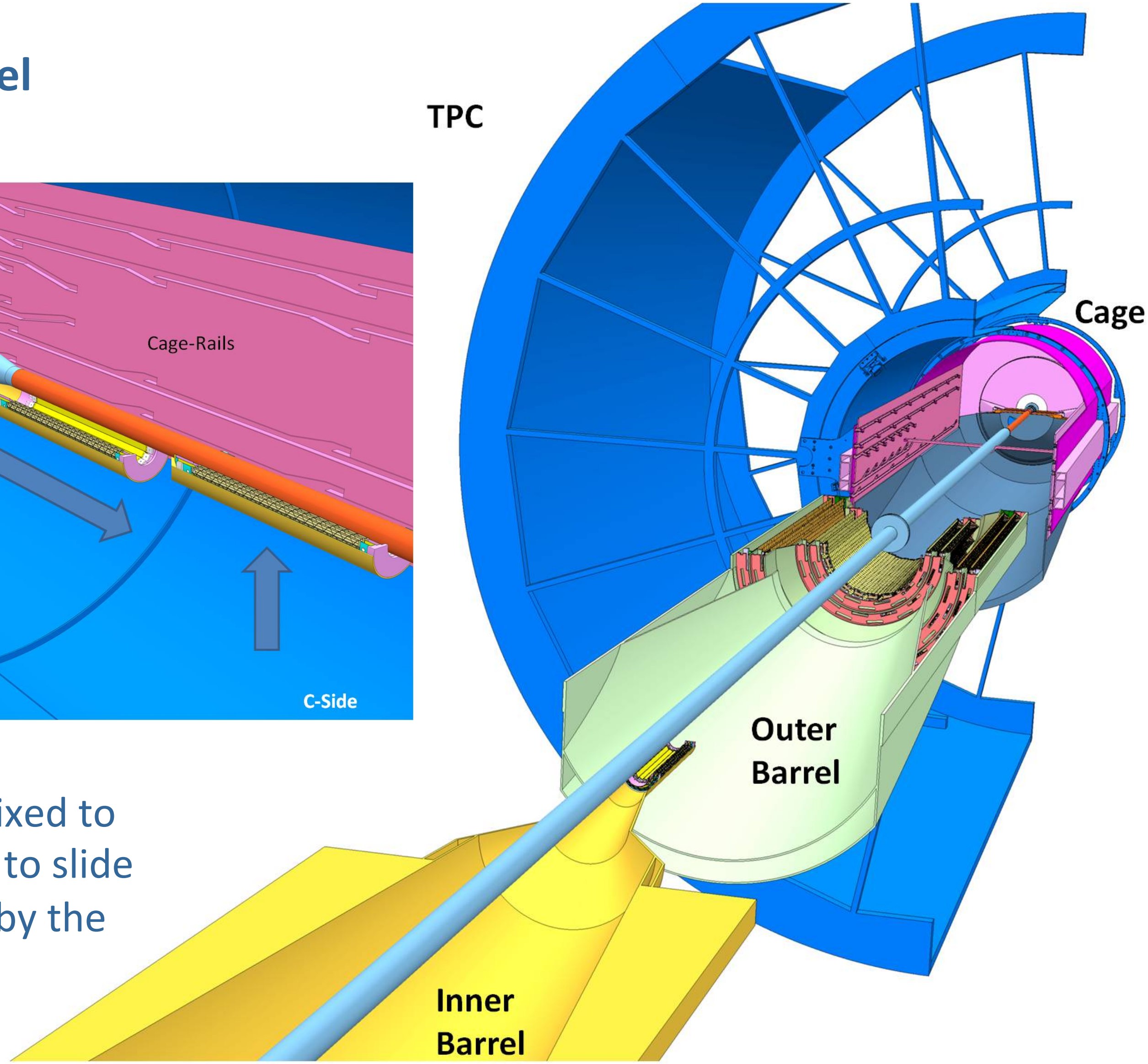
Mechanical Integration



Mechanical Integration

Installation of IB half-barrel





half-barrel are utilizes rollers fixed to the Cylindrical Structural Shell to slide along a rail system supported by the cage

Mechanical Integration