Hyper-K Latest updates (Activities in Japan)

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- 1. Recent news (in Japan)
- 2. Slight update of the timetable
- 3. Update of the sensitivity
 - ~ Accelerator based long baseline experiment ~
- 4. Status of the photo sensor R&D in Japan
- 5. Status of the DAQ R&D (in Japan)

1. Recent news

• Selected one of the **27** 'top projects' out of 192

in 'Japanese master plan for large scale research projects' by Science Council of Japan

Report (In Japanese) : <u>http://www.scj.go.jp/ja/info/kohyo/pdf/kohyo-22-t188-1.pdf</u>

Excerpts (summary translated in English)

No.	Scien- tific Field No.	Project Name	Project Summar	Scientific Significance	Social Value	Project Duration	Financial Requirement (1billion yen)	Implementing Institution, or Affiliation of Proposer
85		Nucleon decay and neutrino oscillation experiment with an advanced large detector	one million ton- scale water Cherenkov detector, Hyper- Kamiokande, to succeed Super- Kamiokande and to perform world-leading neutrino and nucleon decay research in	explore CP violation (matter- antimatter asymmetry) in neutrinos in order to help understand the evolution of the universe. Additionally, with the world's best nucleon decay	Addressing profound questions concerning the elementary structure and evolution of the universe appeals directly to the inherent intellectual curiosity mankind harbors for comprehension of its origins and future. Additionally, dramatic advances in neutrino research with a world- leading project in Japan represent society's dreams for a rich program in basic science.	2015 to 2038	Construction of Hyper- Kamiokande 800, Operating cost of Hyper- Kamiokande 450, Operating cost of J-PARC 600,	Research Organization.

• We had MEXT review (interview) in March.

2. Current status in Japan

Budget for the R&D was approved

1) Grant-in-Aid for Scientific Research on Innovative Area. (5 years from 2013 to 2017) Includes both Hyper-K R&D and T2K/J-PARC improvements. Build a test (small) detector to test the new equipment and components to be used in the HK detector and to confirm the detector stably works as a `system'. Surface of the tank (water shielding liners), water system, photo sensors, signal read out system and calibration system have to be confirmed to work.

2. Current status in Japan

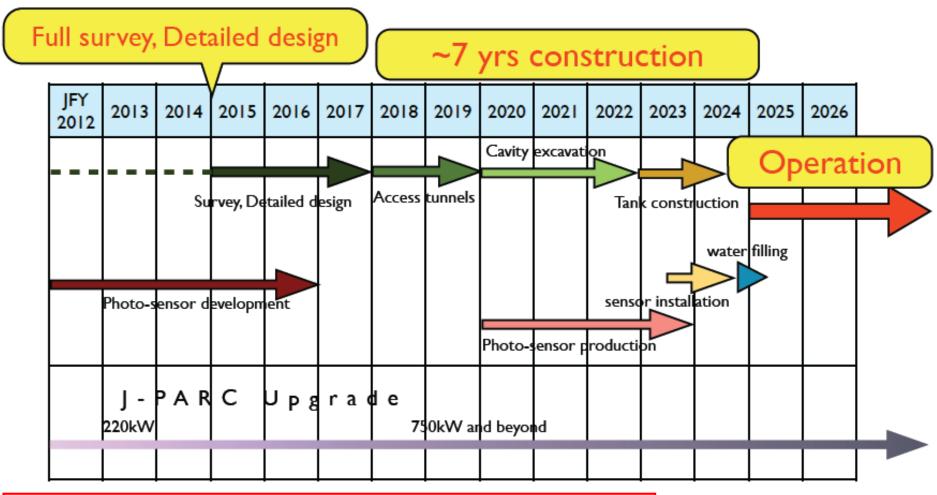
Budget for the R&D was approved

2) Japan/US Cooperation Program in the Field of High Energy Physics.

> For various R&D for the new neutrino detectors (both near and far detectors) and J-PARC accelerator / T2K beamline improvements. Example : R&D of the FPGA-based TDC for

Example : R&D of the FPGA-based TDC for QTC-TDC based front-end electronics is (just) started as a project in 2014.

3. Timeline (slight update)



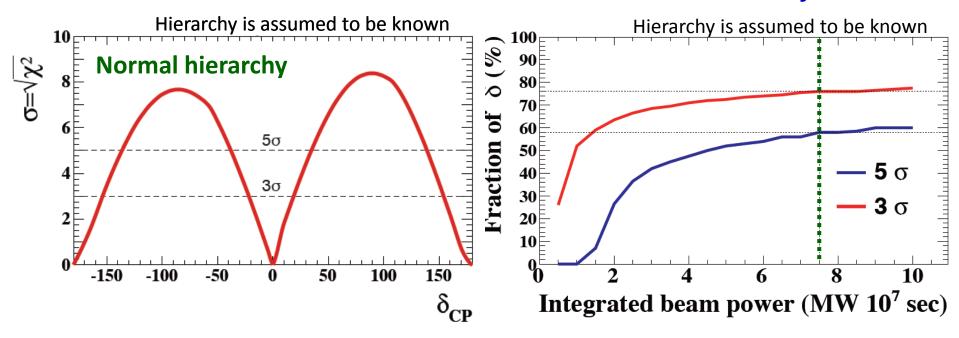
- -2015 Full survey, Detailed design (3 years)
- -2018 Excavation start (7 years)
- -2025 Start operation

4. Updated sensitivity ~ LBL J-PARC & HK ~

Revised systematic errors ~ Determination of CP δ

Sensitivity ~ Exclusion of $\sin \delta = 0$ (7.5 x 10⁷ MW·sec)

Fraction of δ ~ Exclusion of $\sin \delta = 0$



Exclusion of $\sin \delta = 0$ **76%** of δ at **3** σ level and **58%** of δ at **5** σ level with realistic systematic error estimations.

 \sim For better performance and reduction of cost \sim

1) higher QE (from 22% to ~30%)

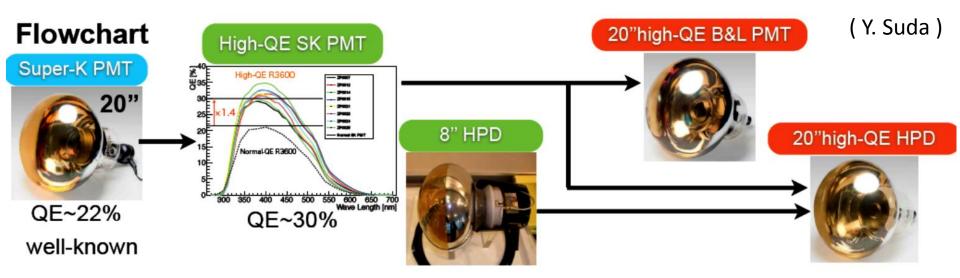
Reduction of # of sensors ~ reduction of cost

2) Better timing response

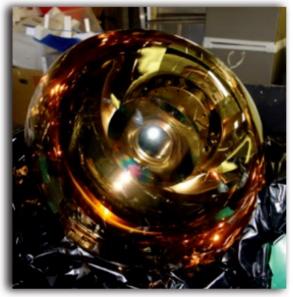
Improvements in the accuracy of the vertex reconstruction

We are testing 2 types of new photo sensors, 20" high QE Box-Line PMT and 20" high QE Hybrid Photo Detector.

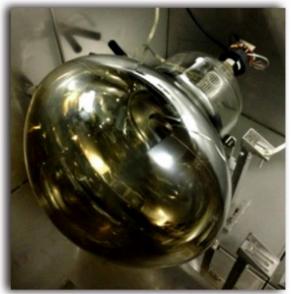
Following 5 pages are from the presentation for TIPP 2014 by Suda-san.



New 20" Prototypes



20" high-QE box&line PMT

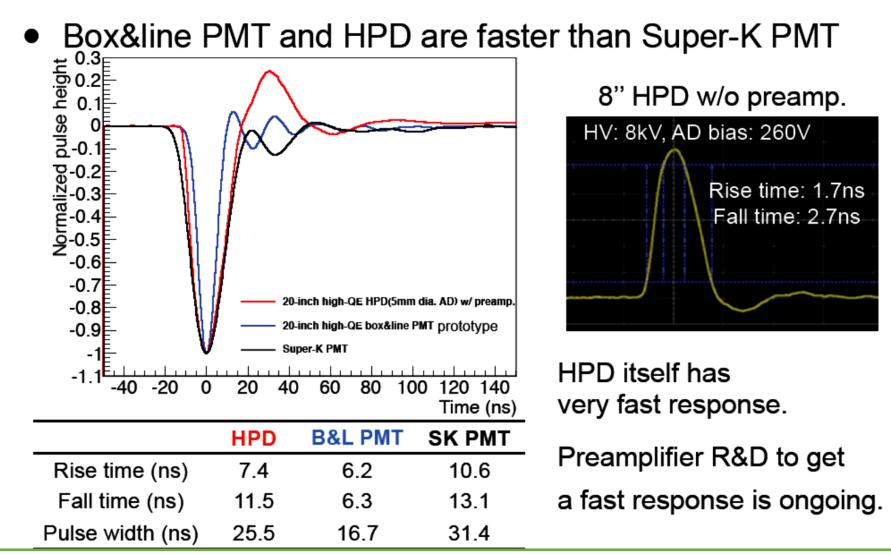


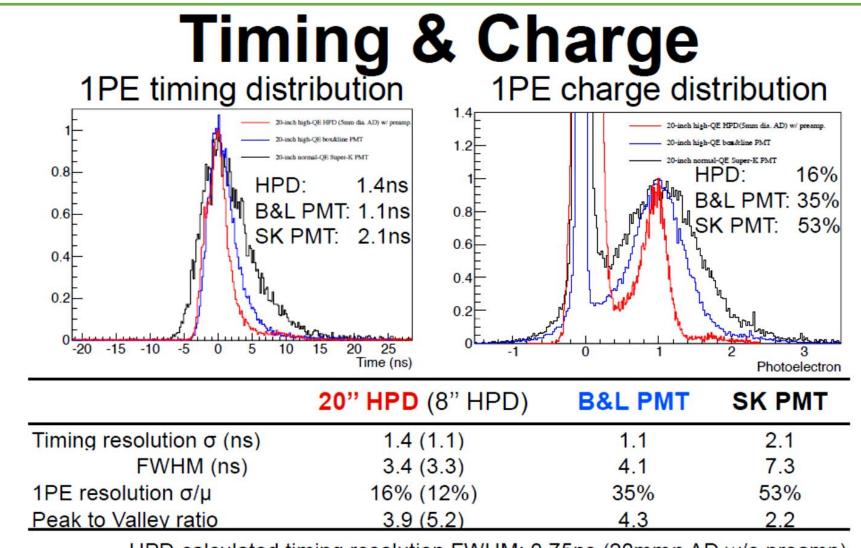
20" high-QE HPD (w/ 5mmΦ AD)

Note

- AD used for the evaluation is smaller size, same as 8" HPD
- 20" HPD w/ 20mmφAD (with good efficiency in final design) will be later measured with coming new preamplifier.

Waveforms





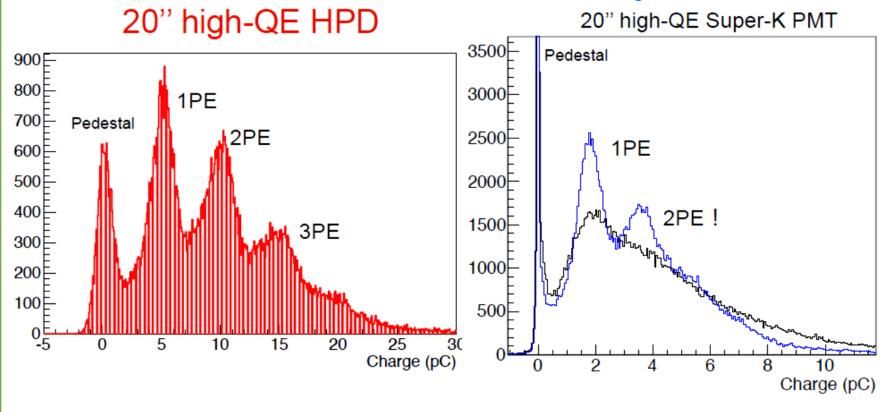
HPD calculated timing resolution FWHM: 0.75ns (20mm AD w/o preamp)

Both box&line PMT and HPD show

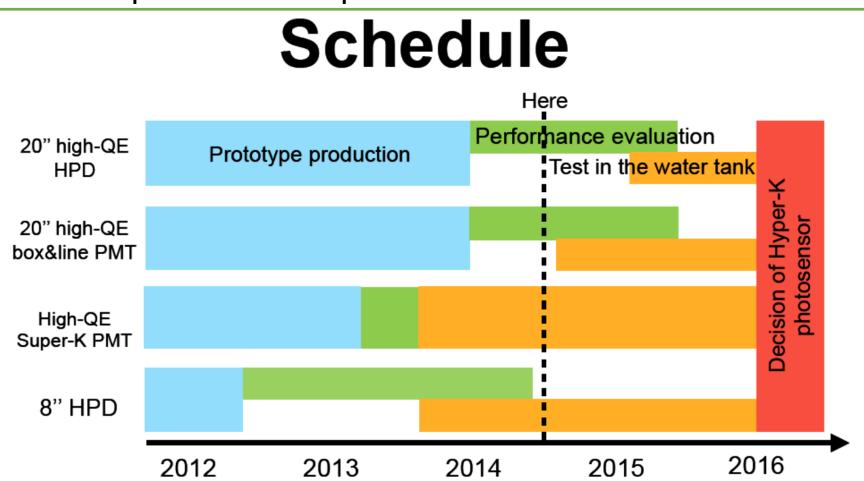
better timing and charge resolution than Super-K PMT

Multi-PE Distribution

20" high-QE Box&line PMT



Multi-photoelectron peaks are clearly seen



- Development of 20" HPD is still ongoing
 - Preamplifier for large AD size, Low capacitance AD
- In this summer, 20" high-QE box&line PMT will be installed in the tank

Baseline design

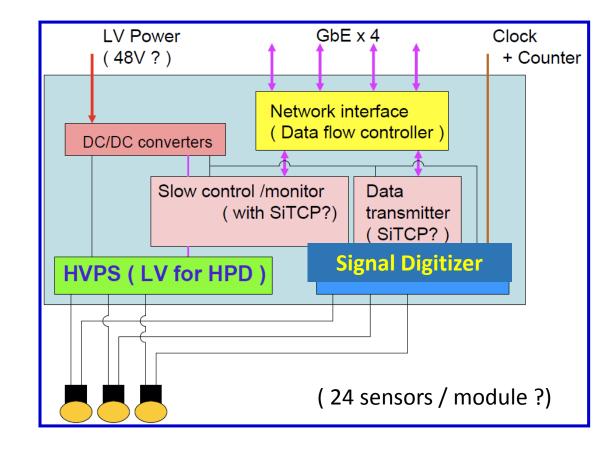
Hardware trigger less DAQ system ~ record all the hits ~ Digitize all the photo sensor signals above threshold (~¼ photo electrons) and read out by a computer.

Key components

- Self triggering
 & dead-time free
 signal digitizers
- HV (LV)

for photo-sensors

- Intelligent network interfaces
- Front-end module in the water



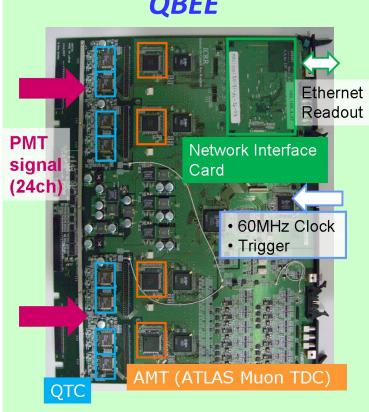
Baseline design

Hardware trigger less DAQ system ~ record all the hits ~ Digitize all the photo sensor signals above threshold (\sim ¼ photo electrons) and read out by a computer.

Possible configurations of the front end module

- QTC (ADC) + TDC Similar to the current SK ~ QBEE
- FADC \bullet Proposed by the Canadian group

In Japan, we have started R&D to develop a test module with QTC & FPGA based TDC.



QBEE

Basic requirements of the front-end module

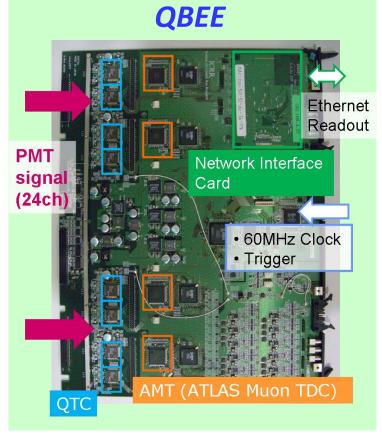
- Built-in Discriminator ¹/₄ p.e. (~0.3 mV)
- Charge integration gate
 - ~ 400 ns
- Processing Speed ~1 usec / hit
- High Sensitivity for single p.e.
- Charge Response Resolution: ~ 0.05p.e. (<25p.e.)
- Wide Charge Dynamic Range (*) 0.1 ~ 1250p.e. (0.2~2500pC)
- Timing Response

0.3ns (1p.e.⇔ -3mV) (RMS)

0.2ns (>5p.e.)

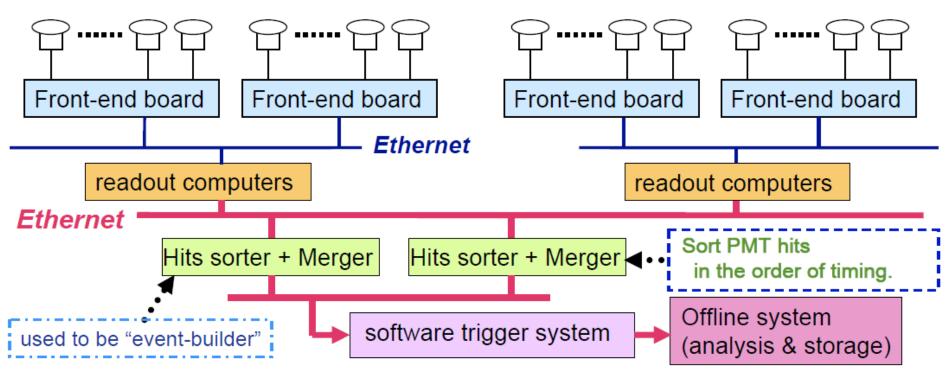
(*) QTC has 3 charge ranges to cover wide dynamic range (1:7:49)

- TDC lowest bit
 - 0.52 ns
- Low power consumption
 - ~< 1W / channel



6. Recent updates of the DAQ R&D R&D of the new front end module 1) Use spare QTC chips for SK (We don't have many but sufficient for the tests.) 2) Use new FPGA based TDC developed in FNAL by Jinyuan-san. AMT3 chip (used in QBEE) has been discontinued. The first buffer of AMT3 was not sufficient and ringing of the PMT signal may fill up the buffer. Data bus throughput is not sufficient to read out all the hits at maximum rate. This TDC is now under development for muon experiment in FNAL. From this summer, evaluation of this TDC will be started. Once this TDC is confirmed to be feasible, we will work on the analog part. Also, we need to prepare new QTC for the real detector. (We are planning to contact "Iwatsu", for possible collaboration.)

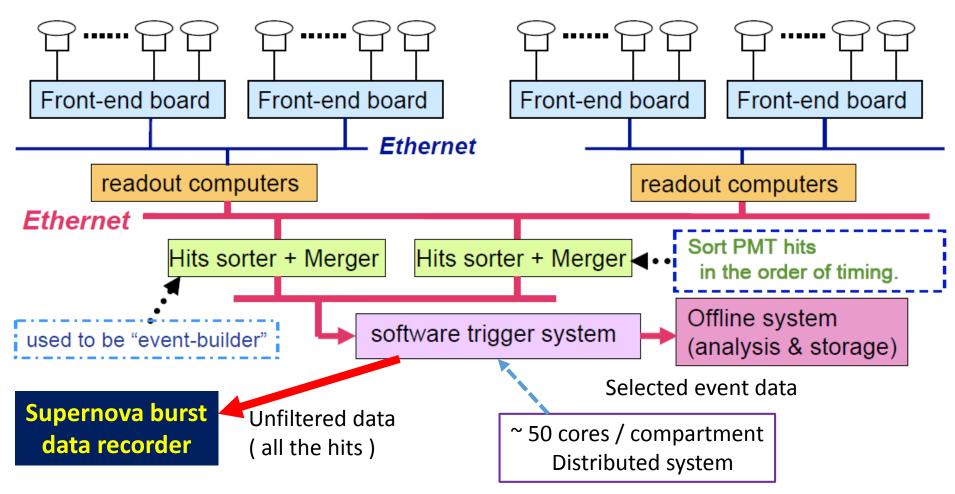
6. Recent updates of the DAQ R&D



 Digitize all the signal (timing and charge) above ~ 1/4 p.e.
 Read out timing and charge with the computers.
 Define events with software and store the event data. Sort the hits in the order of timing and

 a) search for the timing cluster, and
 b) apply reconstruction program for low E_v (recent work / improvements in SK)

6. Recent updates of the DAQ R&D

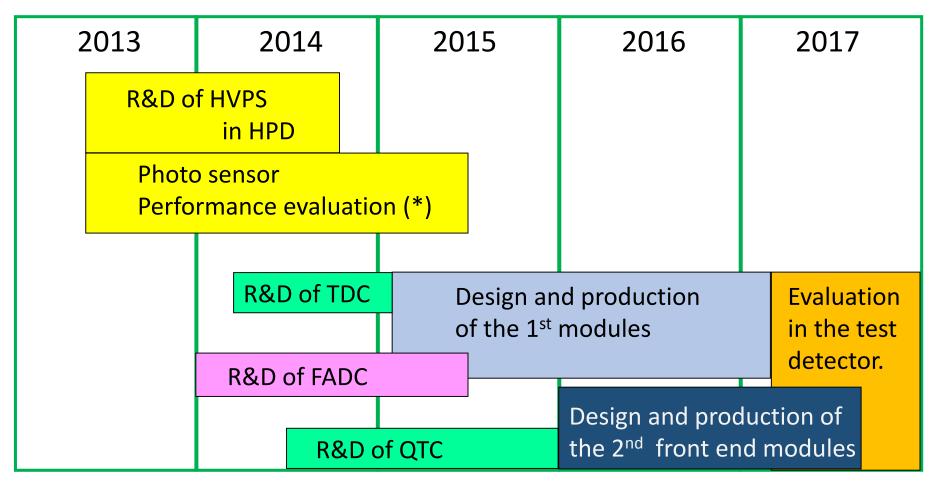


Record all the hit data before and after the supernova for ~ 60 sec.

Transfer all the data to single computer and keep them in the main memory for ~ 60 seconds. Once supernova burst candidate is identified, dump the data to the disk.

This also implemented in SK and now under the test.

Rough timeline of the DAQ system R&D



*) Currently, we are testing the new photo sensors

in the EGADS detector

in collaboration of the EGADS group.

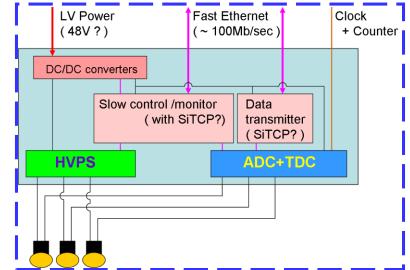
Fin.

Front end electronics + High voltage system

水中用 Front end module の 開発事項

- ケーブルの導入方法
 水中用コネクタ
- ・耐圧防水ケース
 防爆対策も必要か?
- 熱設計

ケースを通して水中に 放熱するしかない



- データおよびタイミング信号を光ファイバーで集約するか?
 耐(水)圧のネットワークケーブルは高いらしい
- こわれにくい HVモジュールの選定(開発?)
- HV制御、電圧モニターの開発
- HVPSとADC部のノイズシールド
- ADC/TDC の開発

などなど

☆ Hybrid PMT で HV や ADC/TDC を PMT に内蔵する場合、 LV供給とデータ集約を行うモジュール Neutrino physics of LBL J-PARC & HK $^{\sim}$ Determination of CP δ

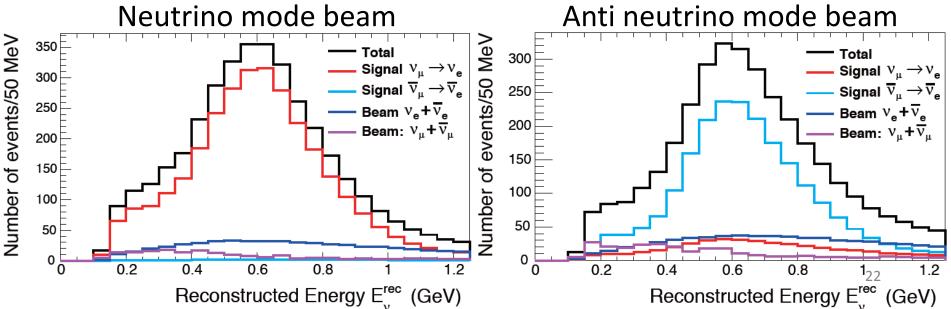
• Expected # of events for $sin^2 2\theta_{13} = 0.1$, $\delta = 0$ and NH

 $(7.5 \times 10^7 \, MW \cdot sec)$

	Signal (vµ→ve CC)	Wrong sign appearance	νμ/νμ CC	beam Ve/Ve contamination	NC
ν	3,016	28		523	172
ν	2,110	396	9	618	265

NC (π^{0}) is not the dominant background already.

Reconstructed energy of neutrino for candidate events



Neutrino physics of LBL J-PARC & HK $^{\sim}$ Determination of CP δ

Systematic error Errors used in the sensitivity studies

~ Realistic estimation of the errors based on the experiences ~

		node	anti-V mode			(T2K 2014)	
	Ve	νμ	Ve	νμ		Ve	νμ
Flux&ND	3.0	2.8	5.6	4.2		2.9	2.7
XSEC model	1.2	1.5	2.0	1.4		4.7	4.9
Far Det. +FSI		1.0	1.7	1.1		3.5	5.6
Total	3.3	3.3	6.2	4.5		6.8	8.1

Reduction of errors in the XSEC models

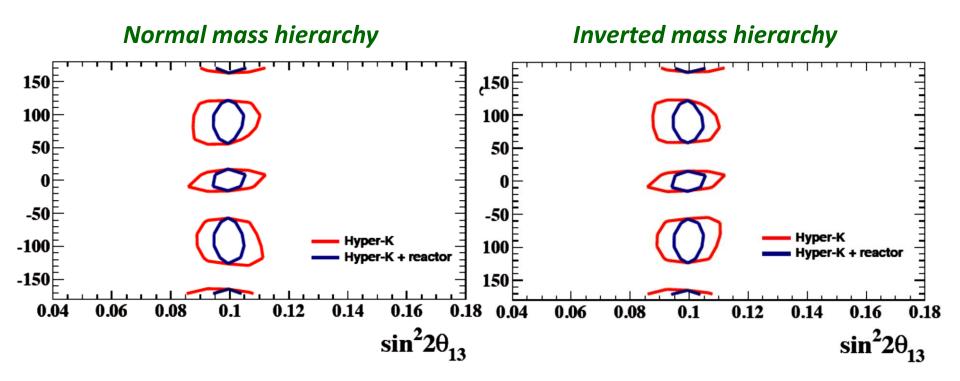
New measurements of neutrino interactions Improved theoretical modeling

Reduction of errors in the far detector + Final state interactions Increased statistics of atmospheric v control sample in HK New near (intermediate) detectors with H₂O target (incl. Water Cherenkov detector) 23 Neutrino physics of LBL J-PARC & HK $^{\sim}$ Determination of CP δ

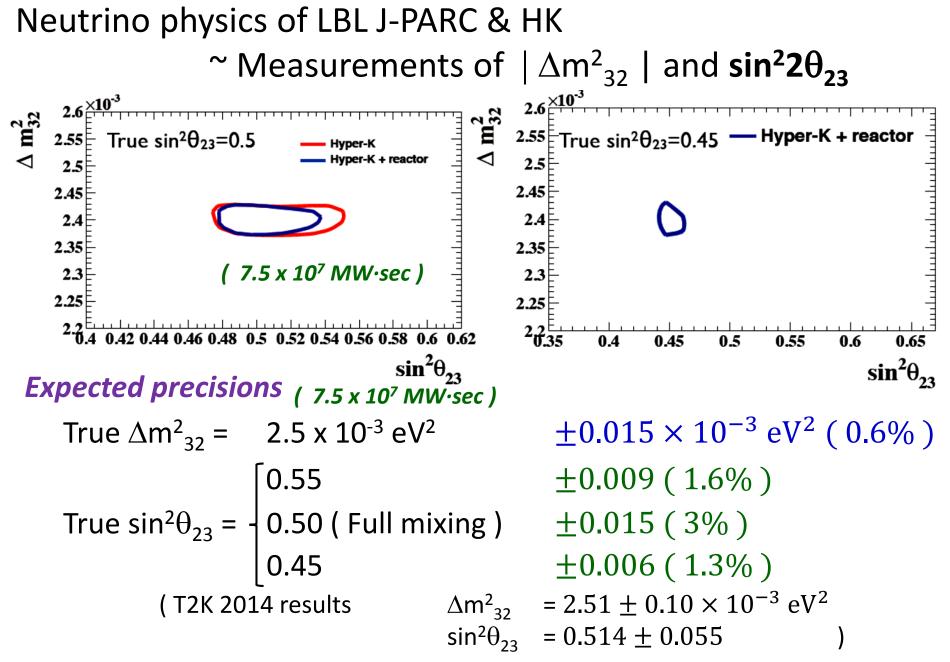
Use both # of observed events

and reconstructed energy spectra of ν and $~\nu.$

 $(@ 7.5 \times 10^7 \text{ MW} \cdot \text{sec}, v: v = 1:3)$

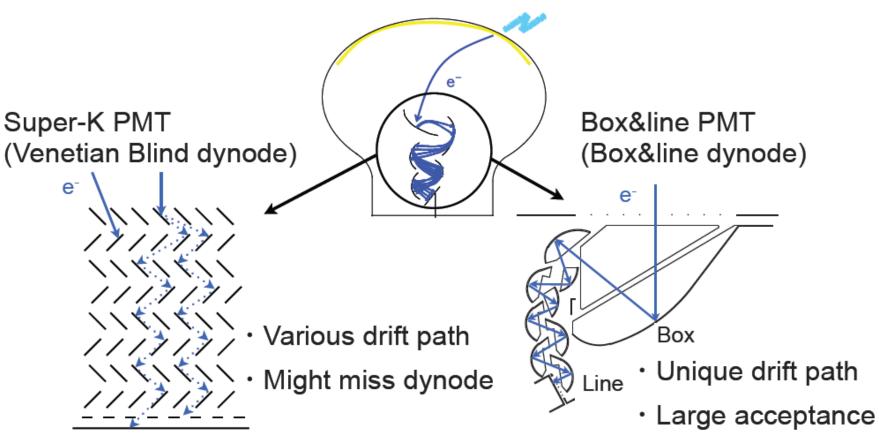


Determination power of CP δ parameter 1σ error of δ is expected to be 8° ~ 19°.



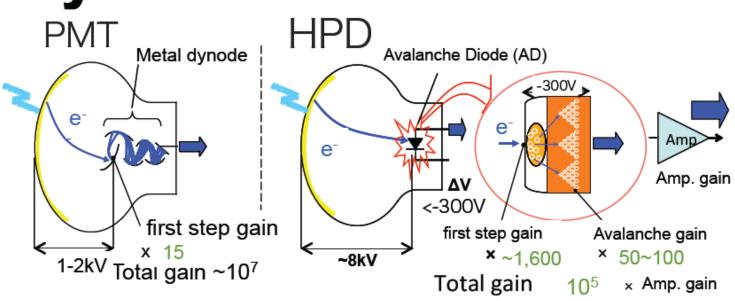
Large improvements & good chance to identify non-maximal mixing.

Box&Line PMT



- Unique drift path \rightarrow Better timing and 1PE resolution
- Large acceptance → Better collection efficiency

Hybrid Photo-Detector



HPD

Advantage

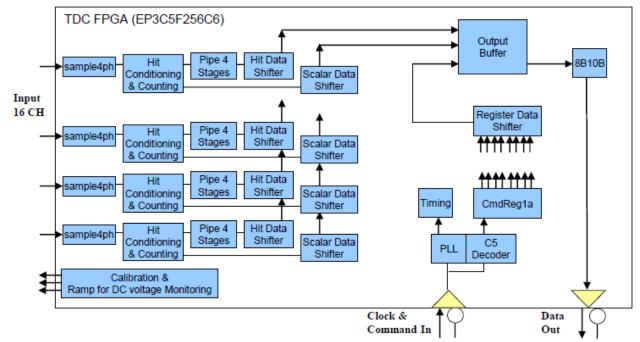
Challenge

- Simple structure \rightarrow Low cost production possibility
- Short drift length → Fast timing response
- High first step gain \rightarrow High single photoelectron resolution

• Difficulty in handling 8kV

No experience to use in a water Cherenkov detector

Block Diagram



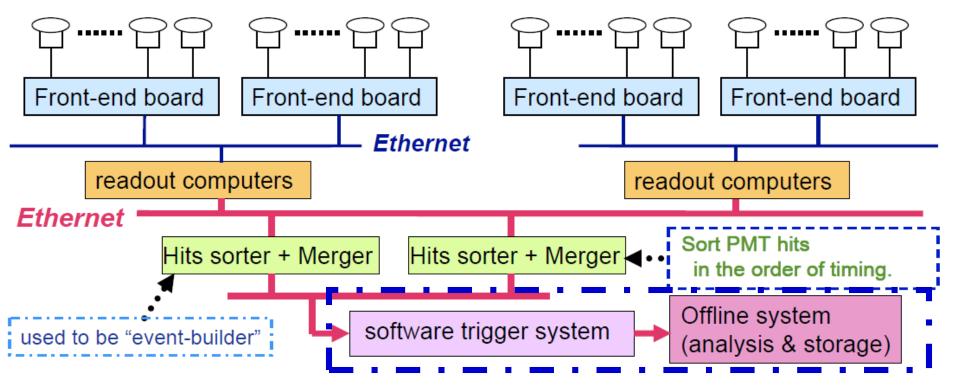
- A 16-channel TDC fits in EP3C5F256C6 with ~50% silicon resource usage.
- Input clock at 10 MHz is multiplied to 200 MHz and two phases of 400 MHz for internal operation.
- Both positive and negative input transitions are digitized with precision LSB 625 ps. (=1/(4*400 MHz))
- Each channel is equipped with a 32-bit scalar which keeps hit count across long period of time.
- For each 10 ms spill, up to 2016 TDC hit data, scalar data, internal register data and an ID header are packed into 2048 32bit words and are output using 8B10B protocol at 25 Mb/s.
- Bursts of up to 4 very rapid hits can be captured. Rapid multiple hits can also be eliminated in the hit conditioning block based on users' setting.
- Only two LVDS pairs, Clock & Command In and Data Out are needed from readout controller to serve the FPGA.
- Calibration hits generation and DC voltage monitoring features are provided.

Apr. 2013, Wu Jinyuan jywu168@fnal.gov

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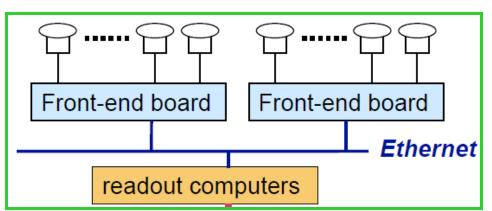
Data rate after the software trigger

~ real-time data processing ~



Assumption 10 compartments (N = 10) 10 kHz dark, 10 k sensors / compartment μ rate = 25 Hz (muon rate * area ~ 12 times larger) ~ 8 MB/sec/compartment after software trigger. ~ 45 % from SLE & 35% from μ

Possible front-end electronics module connections





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2) Connect neighboring boards

- Reduce # of the cables to the top
- Reduce total amount of cables
- Eliminate single point failure
 Usually, data collected by a module
 are transferred to the upper module
 (vertically)

If a module failed,

transfer data to the other module instead of the failed module

(horizontally).

Need to design

the total amount of data < 1Gb/s

~ Design of the data flow

1) Assuming 1Gb Ethernet

- Reliability
- Power consumption

Possible front-end electronics module connections

Amount of data from a module ~ 200 x [dark rate] Bytes/sec (assuming 24 ch / board) Possible configuration for 10 kHz dark rate Dark rate 3905 1) 5kHz N.L Data rate ~ 1 MB/sec/board top ~24 sensors Connect 18 boards / cable 6 front-modules 1 cable from each side side ~48 sensbrs ~ 120 cables from the tank 12 front-modules 2) 10kHz Data rate ~ 2 MB/sec/board Inner Detector bottom ~24 sensors Con Connect 9 boards / cable Linin 6 front-modules 2 cables from each side Bedrock ~ 240 cables from the tank later Tank 24000

of channels per 1 front-end board

of channels per board

High density module will be cost effective.

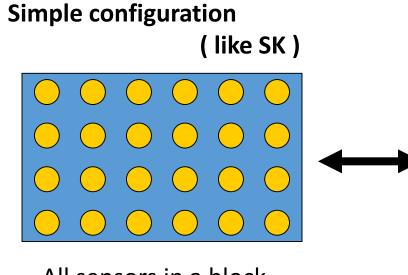
Limitations • Data size per module will be increased

• Larger "dead region" in case of failure

One idea to minimize the effect

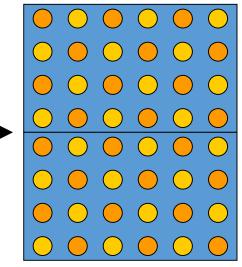


HK detector



All sensors in a block are connected to one font-end board

Possible alternative



Connect neighboring sensors to different front-end boards

