



## LHC Injectors Upgrade

# Beam Loss Monitoring & Observation

Status update on the development, installation and commission plans

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12/06/2014



# Overview

- General
  - Budget
  - Planning
- Installation
  - Crates
  - Detector positions
  - Cables
- Development
  - FPGA
  - FESA Server
  - Expert Application
- Summary



# General





# Budgetary Requirements

- Updated general cost breakdown up until 2019

LIU-PSB	2011	2012	2013	2014	2015	2016	2017	2018	TOTAL LIU (kCHF)
Ring (L2 position)			90						90
Injection & BI Line					52	49			101
Injection (observation)					110	37			147
Ring (L3 position)				50		123			173
Extraction					80	80			160
<b>TOTAL LIU (kCHF)</b>	<b>0</b>	<b>0</b>	<b>90</b>	<b>50</b>	<b>242</b>	<b>289</b>	<b>0</b>	<b>0</b>	<b>671</b>

- Summary of differences on the updated general cost

PSB	original (kCHF)	updated (kCHF)	Diff	Budget Allocation		
				cables	electronics	Detectors
Ring (L2 position)	90	90	0	LIU	CONS	spares
Injection & BI Line	65	101	36	LIU	CONS	spares
Injection (observation)	77	147	70	LIU	LIU	LIU (Diamond)
Ring (L3 position)	40	173	133	LIU	LIU	LIU (Flat IC)
Extraction	0	160	160	LIU	LIU	spares
<b>TOTAL LIU (kCHF)</b>	<b>272</b>	<b>671</b>	<b>399</b>			



# General Planning

Machine/Area		Channels	Documentation	Detectors	Electronics	Installation & Commissioning	Budget	Expected
PSB	Ring (L2 position)	32	Complete	LHC-IC	Pre-series	On-track	Complete	LS1
	Injection & BI Line	18	Complete	LIC	Pre-series	Started	Complete	L4C
	Injection (observ.)	8	Complete	Diamond	OASIS	Started	Complete	L4C
	Ring (L3 position)	32	Complete	FIC	Series	Not started	Complete	LS2
	Extraction	28	Complete	LHC-IC	Series	Not started	Complete	LS2

Plans for **LS1 & LINAC4 Connection** are clear and agreed

- Update of budget (times and amounts) is on-going.
- Will validate pre-series version of electronics with beam
  - Series production to be received towards the end of 2016
- Development of **Firmware and Software** will continue after LS1
  - FESA server, Threshold Management, Logging DB, Controls integration
- Additional **cables and monitors** could be installed during LINAC4 Connection
  - Add electronics in the surface when available.
- Diamond based system's acquisition electronics under study
  - Pursuit more actively after LS1
  - First version will be based on OASIS



# Status of the Installation



# Detector Supports

- **PSB Ring:** design complete
  - Prototype constructed by the CERN workshop
  - Production completed on Dec. 2013
  - Installed and checked for conformity
- **PSB Injection:** started
  - Design started Dec. 2013
  - First versions ready for both LIC and IC detector types
  - Decision/clarification needed which detector type to use



# Detector Support – PSB Ring



- Very tight integration.
- Verified all locations; no interference / obstruction to other systems.





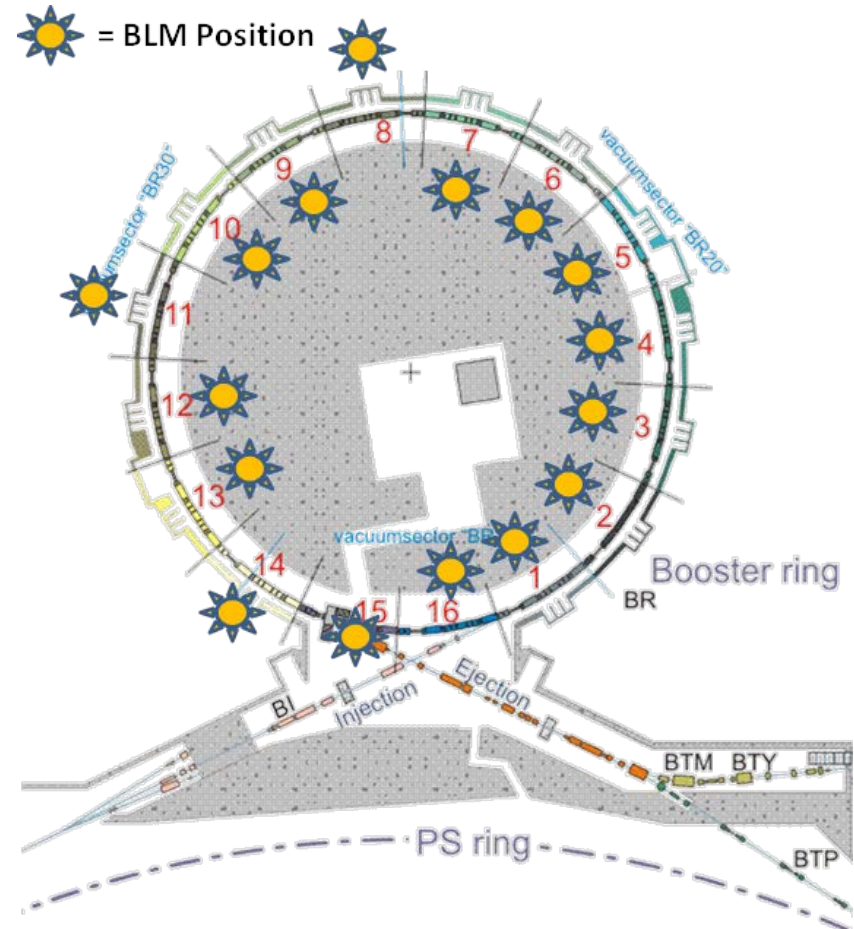


# Position of the detectors

For periods:

- 8, 11 and 14 on the outside,
- 15 between the ring and the ejection line,
- all others on the inside of the ring.

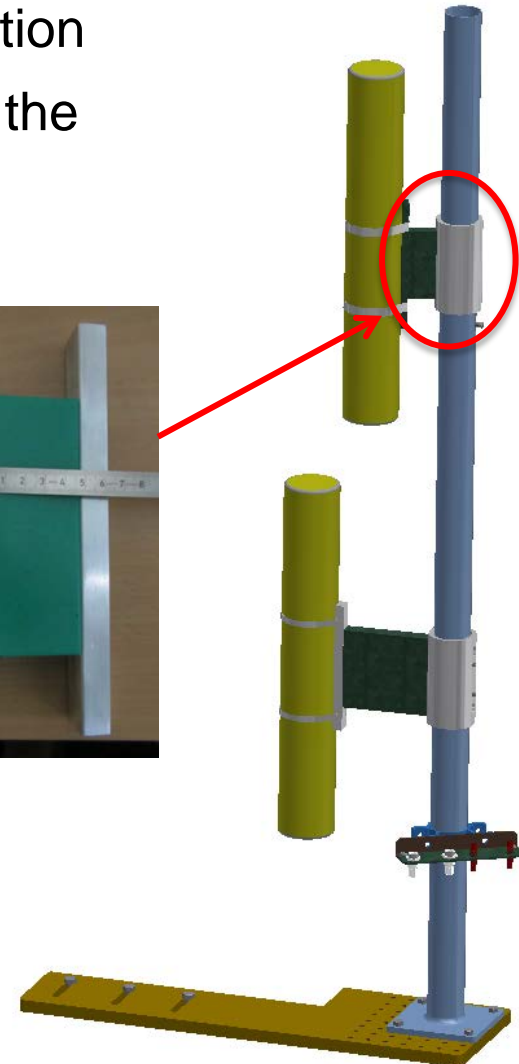
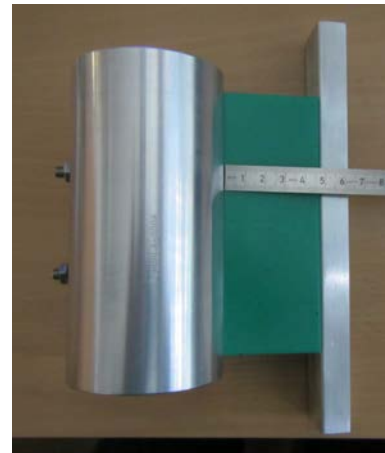
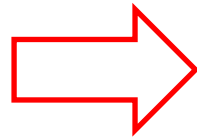
Period	Position	Comment
1	Internal	
2	Internal	
3	Internal	
4	Internal	
5	Internal	
6	Internal	
7	Internal	<i>BPM pickups</i>
8	External	custom support
9	Internal	<i>1230uSv</i>
10	Internal	
11	External	custom support
12	Internal	
13	Internal	<i>RF cavity</i>
14	External	<i>displaced due to ion pump</i>
15	External	Ejection custom support
16	Internal	





# Modification to the supports

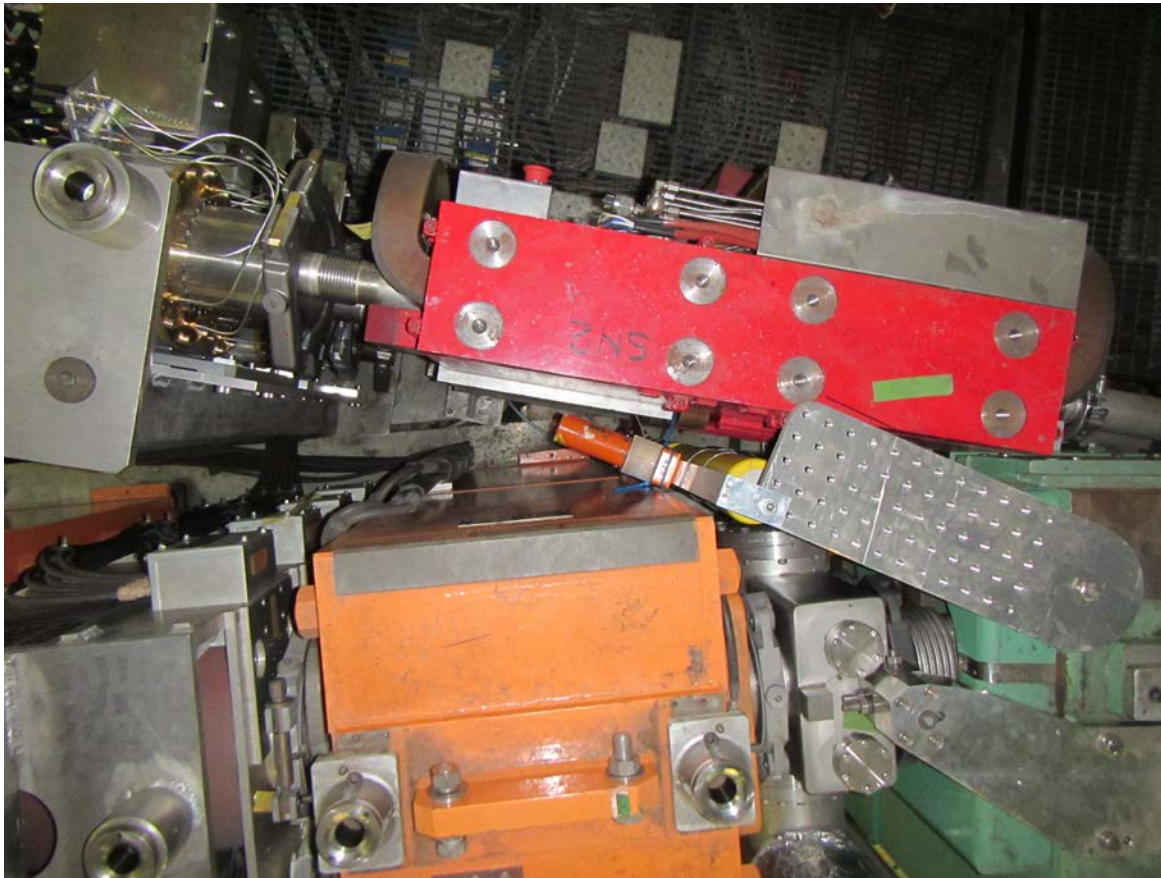
- Ion pumps do not allow standard installation
- Detector is positioned further away from the beam line a few cm.





# Custom support for period 15

- No space to add the detector on the inside of the ring
- ACEMs mounted on the same plate



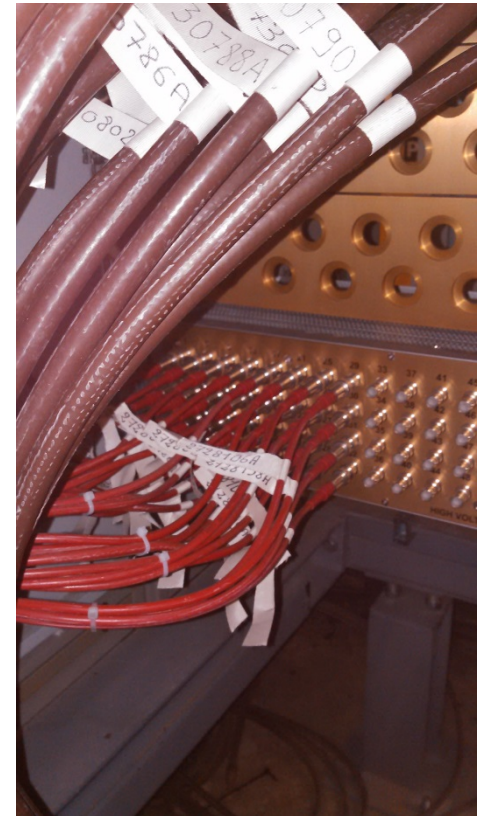


# BLM Cable installation in PSB

- New cable (CKC50) production run on tight schedule:
  - Modification of the CKB50 specs
  - Completed and delivered on-time
- Re-installation in PSB
  - Conformity measured (developed a test-bench)
  - Completed on-time
- Patch-Cords
  - Several types needed (length and connector type)
  - **Completed and tested**



Signal Cables



HV Cables



Signal and HV Patch-Cords

# Rack Installation



Rear View



Front View

- **PSB Ring: completed**
  - Floor supports have been designed and installed
  - Rack installed
- **PSB Injection & Extraction: on-track**
  - Floor supports have been designed and installed
  - Positions defined



Floor Support



# Status of Development



# PCB Development

- All prototypes verified and functional.
- Pre-Series production will need to cover needs till LS2.
- **Tenders for the Acquisition and Mezzanine modules production sent.**

Name	Acronym	Number of Components	2010	2011	2012	2013	2014	2016/7
			Prototype Development			Pre-Series		Series
Acquisition Module	BLEDP	1934	First Prototype (1 piece)	V1.0 (2 pieces)	V2.0 & V2.1 (3 pieces)	-	Production V3.0 (20 pieces)	Production V3.x (60-100 pieces)
Acquisition Backplane	BLEBP	1173	-	V1.0 (2 pieces)	V2.0 (1 piece)	Production V3.0 (7 pieces)	-	Production V3.0 (10-15 pieces)
Processing Mezzanine	BLEPM	210	-	V1.0 (1 piece)	-	-	Production V2.0 (20 pieces)	Production V2.x (60-100 pieces)
Crate Main Panel	BLEMP	52	-	First Prototype (2 pieces)	V1.0 (2 pieces)	Production V2.0 (7 pieces)	-	Production V2.0 (10-15 pieces)
Crate Control Unit	BLECU	180	-	First Prototype (1 piece)	Second Prototype (1 piece)	Production V1.0 (7 pieces)	-	Production V1.0 (10-15 pieces)
Acquisition Crate	BLEAC	200	-	First Prototype (1 piece)	V1.0 (2 pieces)	Production V2.0 (7 pieces)	-	Production V2.0 (10-15 pieces)
Crate Programmer	BLEJP	160	-	-	First Prototype (1 piece)	Production V1.0 (7 pieces)	-	Production V1.0 (10-15 pieces)
High Voltage Distribution	BLEHV	100	-	-	-	Production V1.0 (7 pieces)	-	Production V1.0 (10-15 pieces)



# PCB Production

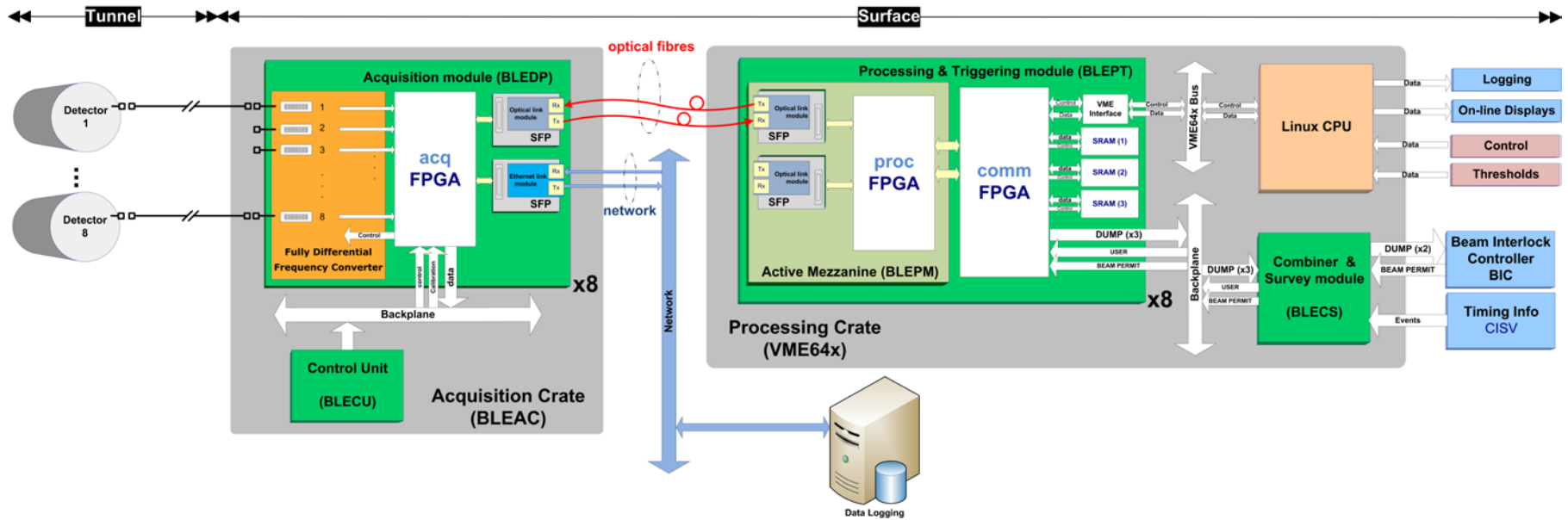
- Production of the **Acquisition** (BLEDP) and **Mezzanine** (BLEPM) modules.
- **Tenders** for the Acquisition and Mezzanine modules production sent.
- Costs: BLEDP: ~60 KCHF, BLEPM: ~30 KCHF

15/04/2014	Send Tenders
4 weeks	
20/05/2014	Deadline for offers
01/06/2014	Send order
(production of pre-series) 9 weeks	
15/08/2014	Reception of pre-series
(verification of production quality) 2 weeks	
01/09/2014	Give OK/FAIL
(production of series) 7 weeks	
01/11/2014	Reception of series



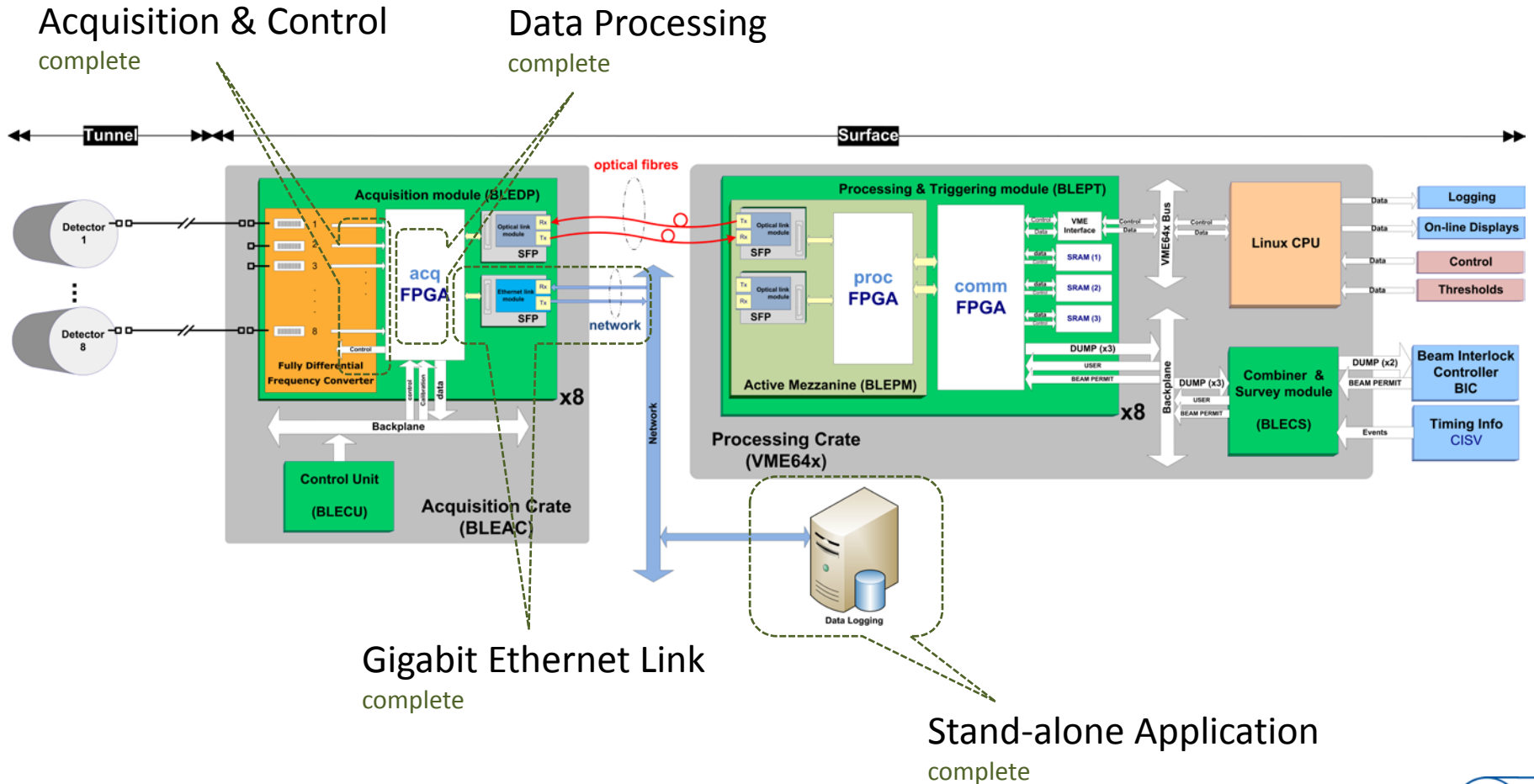


# System Overview



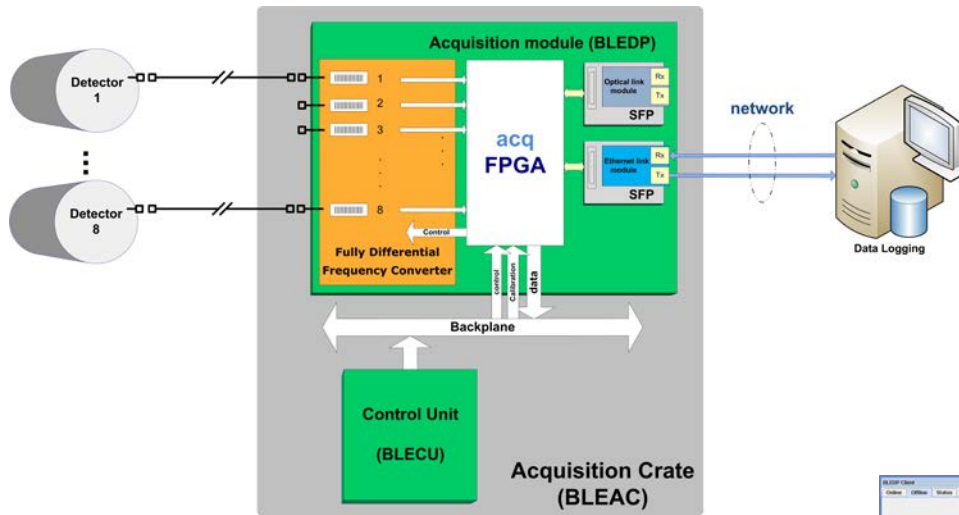


# FPGA Development (1/4)

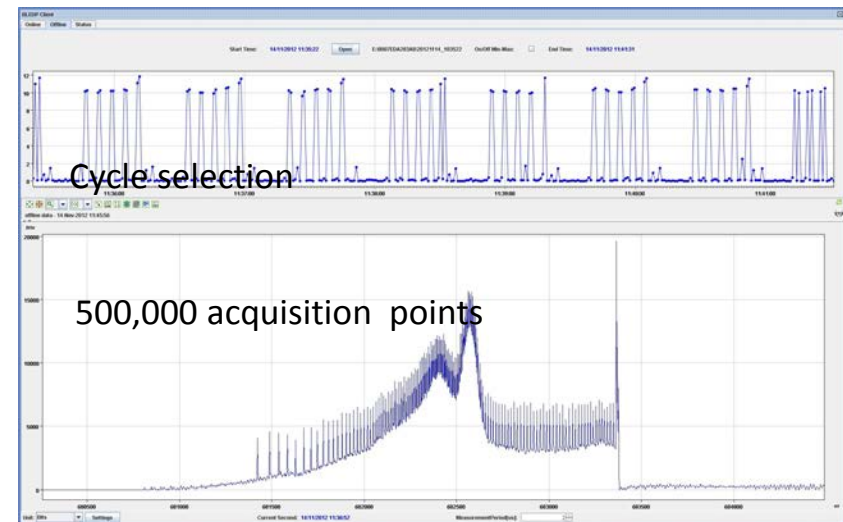




# Stand-alone/Ethernet version

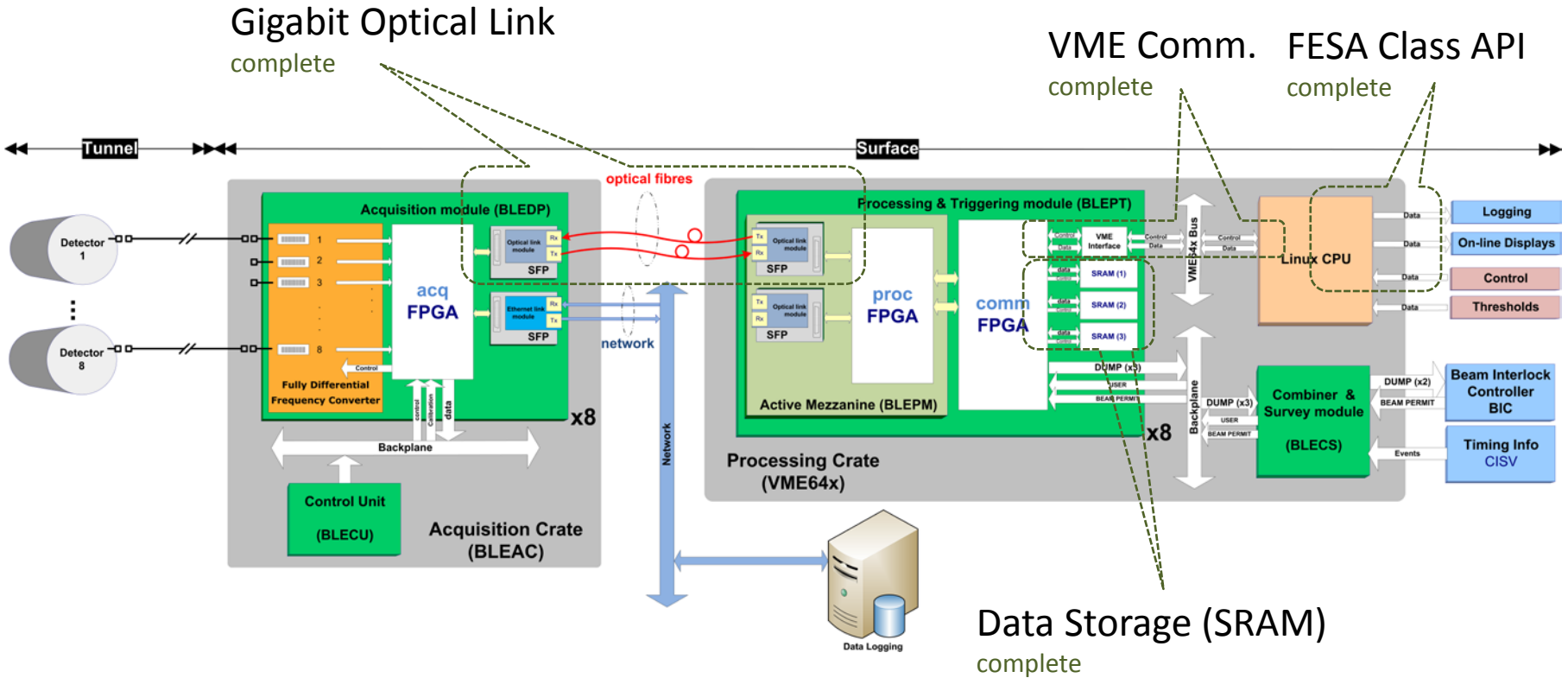


- Ethernet-based version of the system ready
- Very powerful for
  - verification,
  - commissioning and
  - fine observations



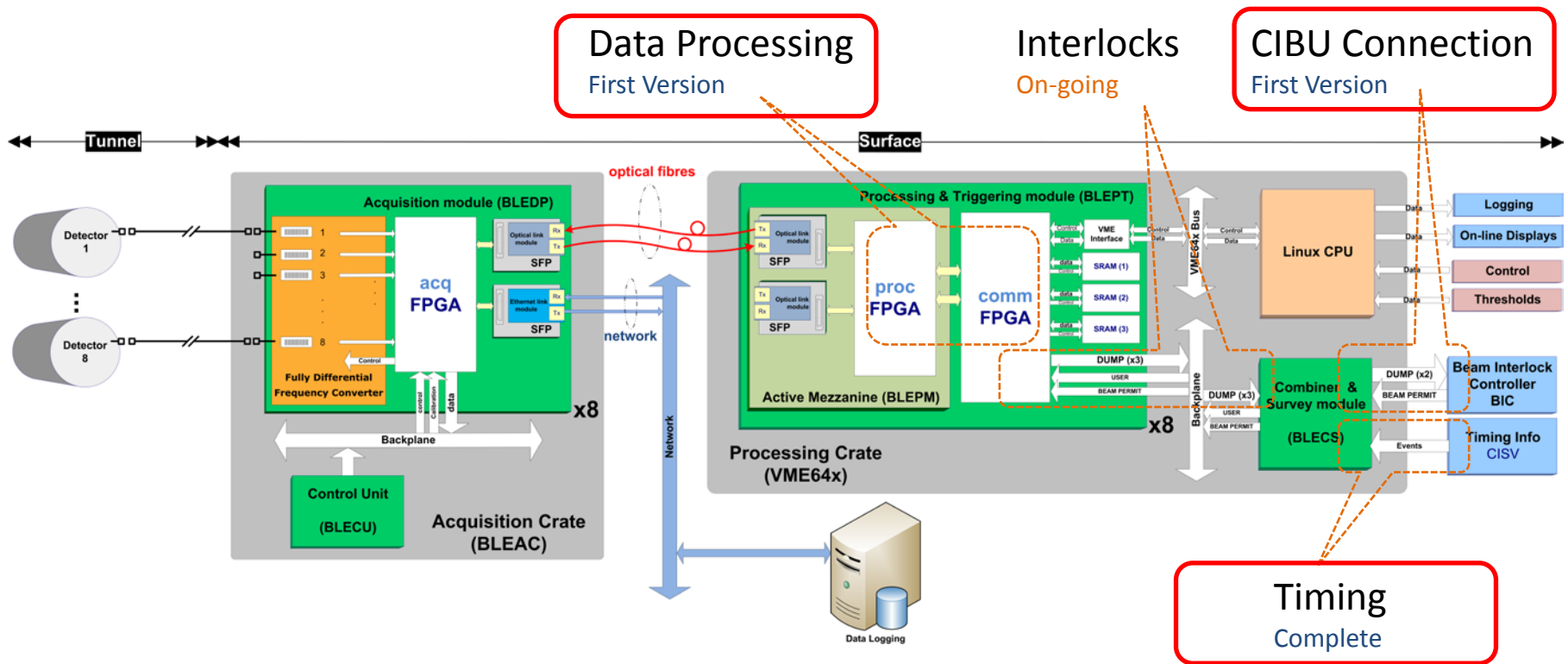


# FPGA Development (2/4)



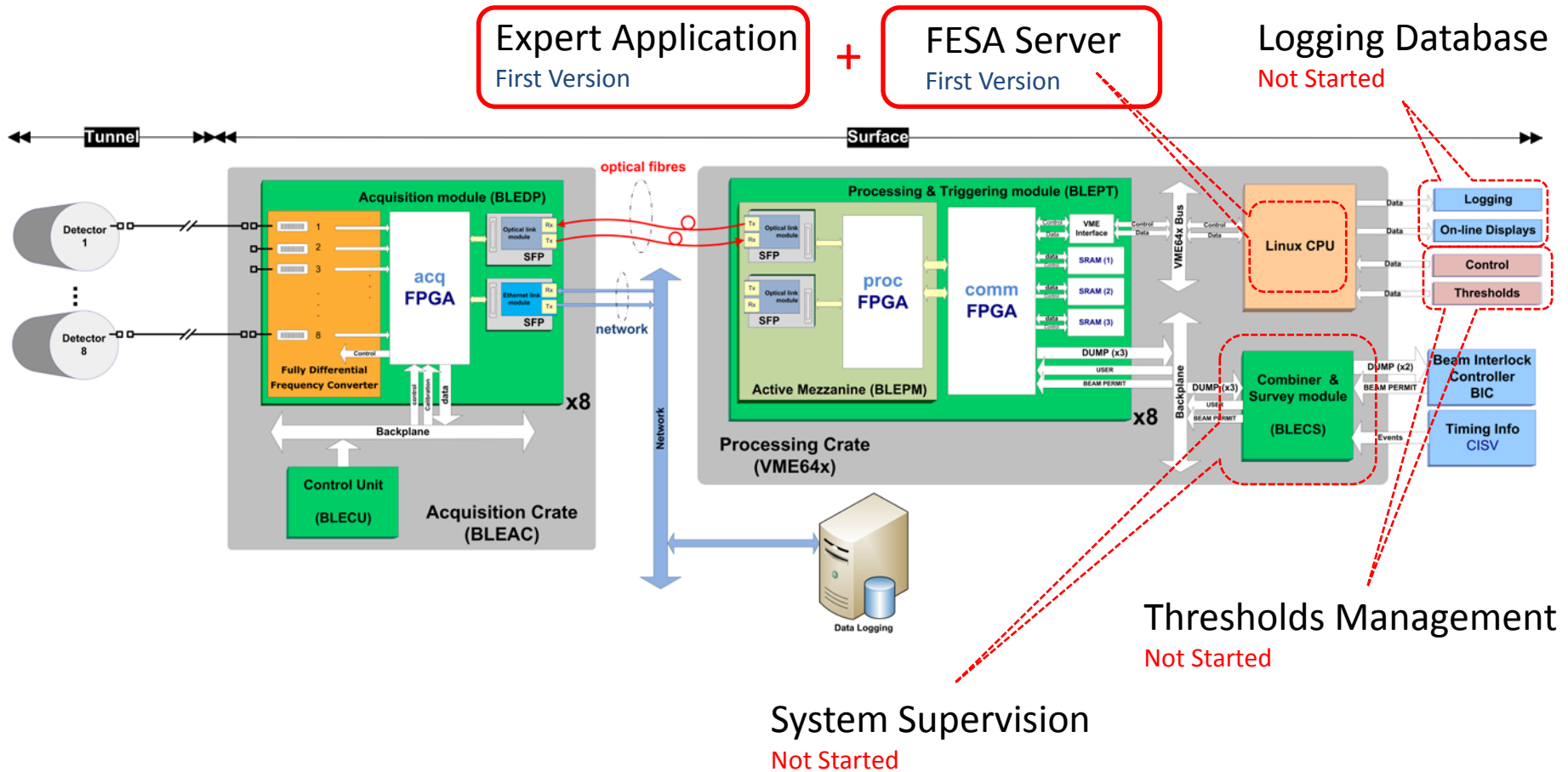


# FPGA Development (3/4)



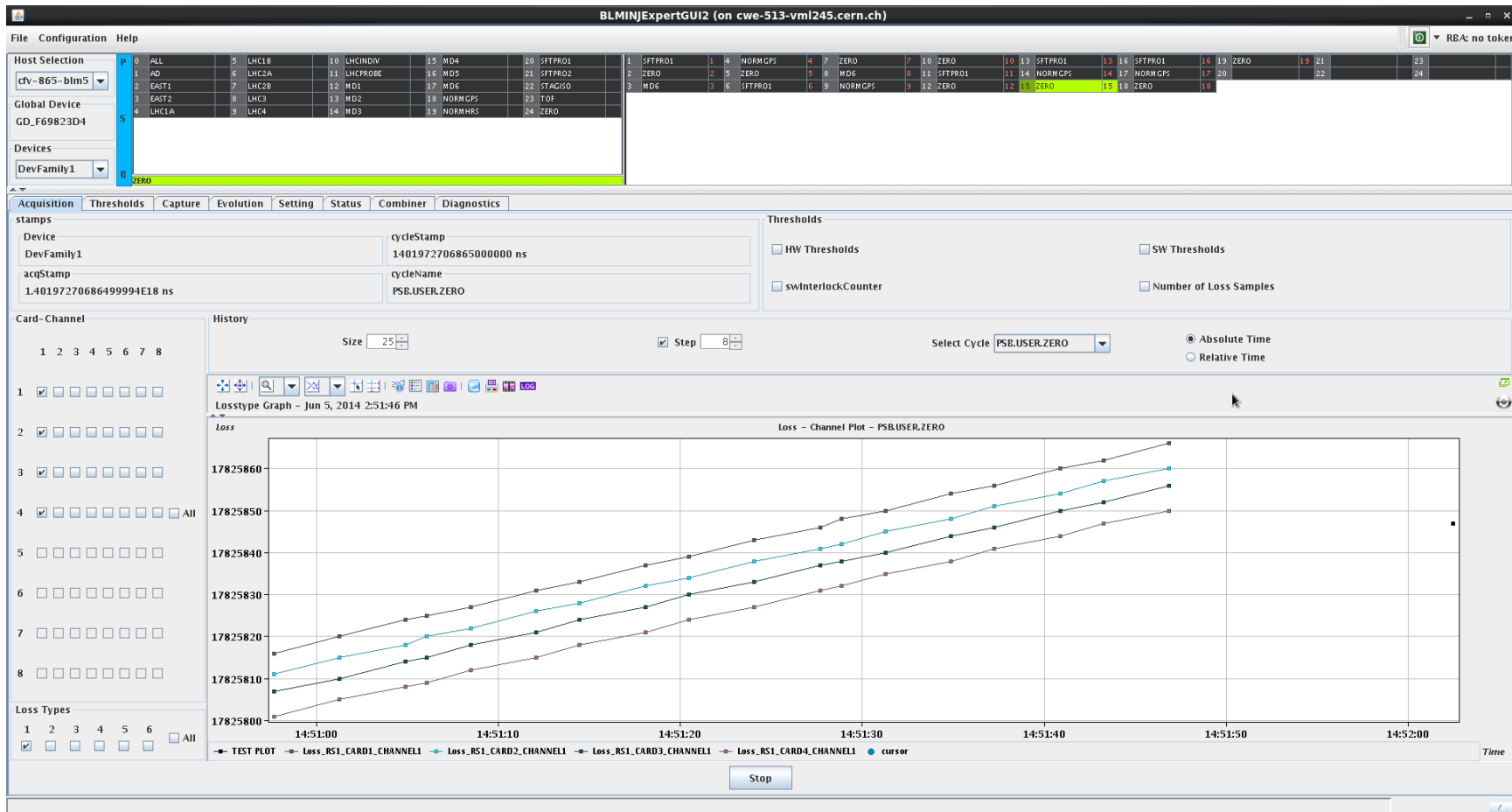


# FPGA Development (4/4)



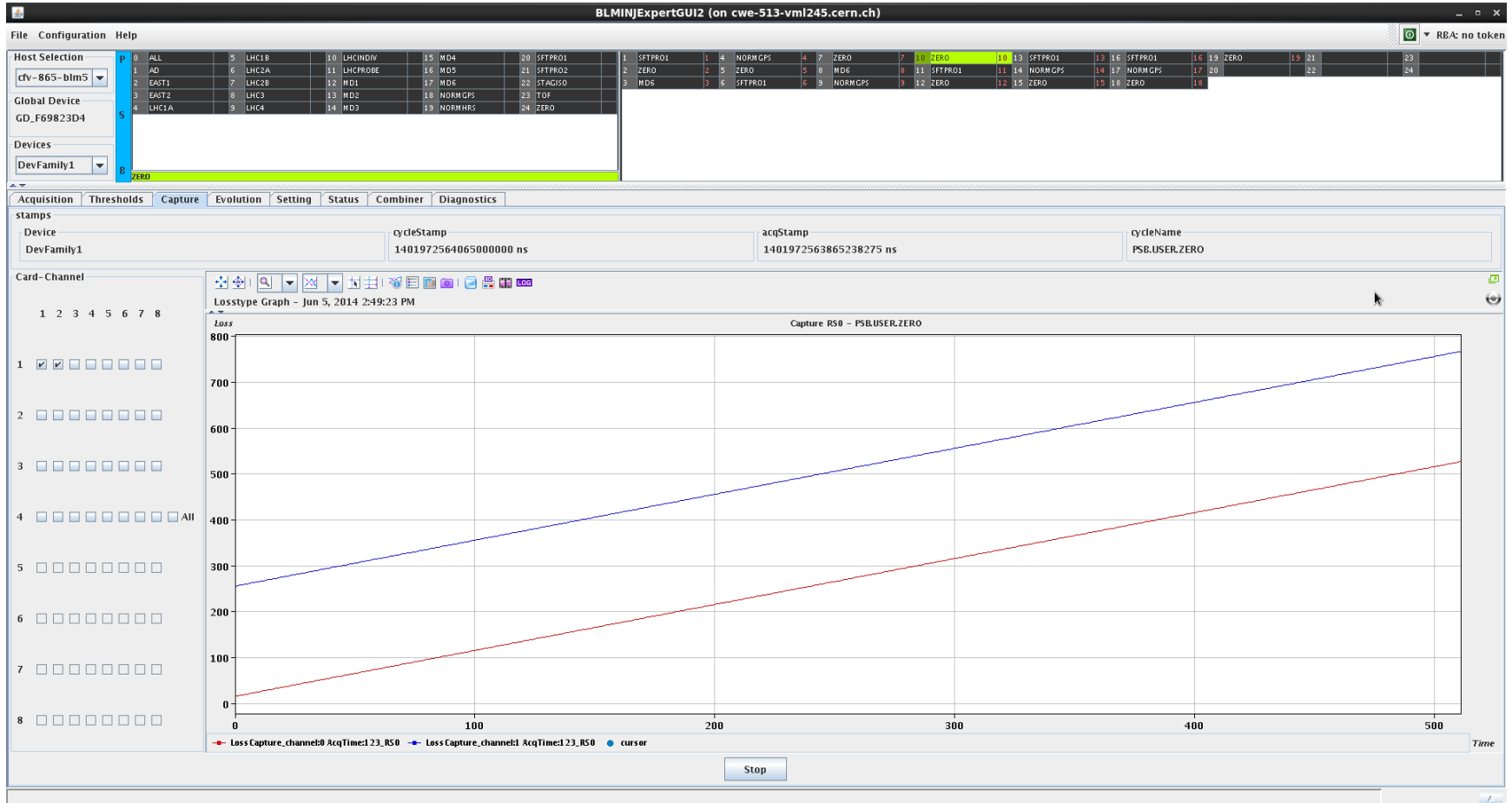


# Expert Application – Integrals





# Expert Application – Capture







# Expert Application – Interlocks

BLMINJExpertGUI2 (on cwe-513-vm1245.cern.ch)

File Configuration Help

Host Selection: cv-865-blm5

Global Device: GD\_F69823D4

Devices: DevFamily1

0	ALL	5	LHC1B	10	LHCINDIV	15	MD4	20	SFTPRO1	1		4		7	ZERO	7	10	ZERO	10	13	SFTPRO1	12	15	SFTPRO1	16	19	ZERO	19	21		23		24
1	AD	6	LHC2A	11	LHCPROBE	16	MDS	21	SFTPRO2	2		5		8	MD6	8	11	SFTPRO1	11	14	NORMGPS	14	17	NORMGPS	17	20							
2	EAST1	7	LHC2B	12	MD1	17	MD6	22	STAGISO	3		6		9	NORMGPS	9	12	ZERO	12	15	ZERO	15	18	ZERO	18								
3	EAST2	8	LHC3	13	MD2	18	NORMGPS	23	TOF																								
4	LHC1A	9	LHC4	14	MD3	19	NORMHRS	24	ZERO																								

Acquisition Thresholds Capture Evolution Setting Status Combiner Diagnostics

Interlocks

CIBU status

Channel 1 Channel 2

Hardware Interlocks

Channel 1 Clear channel 1 Channel 2 Clear channel 2

Software Interlock

FieldName	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	
User played	🟢	🟢	🟢	🟢	🟢	🟢	🟢	🟢	🟢	🟢	🟢	🟢	🟢	🟢	🟢	🟢	🟢	🟢	🟢	🟢	🟢	🟢	🟢	🟢	🟢	🟢	🟢	🟢	🟢	🟢	🟢	🟢	
Channel 1	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴
Channel 2	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴

All Clear channel 1 All Clear channel 2

All Set channel 1 All Set channel 2

Software watchdog

110 Time to interlock (ms)

2400 Watchdog timeout (ms)

Set watchdog timeout (ms)

Stop





# Expert Application – Diagnostics 1/2

BLMINJExpertGUI2 (on cwe-513-vml245.cern.ch)

File Configuration Help

Host Selection: cfw-865-blm5

Global Device: GD\_F69823D4

DevFamily1: SFTPRO1

0	ALL	5	LHC1B	10	LHCINDIV	15	MD4	20	SFTPRO1	1	SFTPRO1	4	NORMCPS	4	7	ZERO	7	10	ZERO	10	13	SFTPRO1	12	16	SFTPRO1	16	19	ZERO	19	21	23	23
1	AD	6	LHC2A	11	LHCPRDRE	16	MD5	21	SFTPRO2	2	ZERO	2	5	ZERO	5	8	MD6	8	11	SFTPRO1	11	14	NORMCPS	14	17	NORMCPS	17	20	22	24	24	
2	EAST1	7	LHC2B	12	MD1	17	MD6	22	STAGISO	3	MD6	3	6	SFTPRO1	6	9	NORMCPS	9	12	ZERO	12	15	ZERO	15	18	ZERO	18					
3	EAST2	8	LHC3	13	MD2	18	NORMCPS	23	TOF																							
4	LHC1A	9	LHC4	14	MD3	19	NORMHRS	24	ZERO																							

Acquisition Thresholds Capture Evolution Setting Status Combiner Diagnostics

General Analog SFPs Graph IL BLEDP IL BLEPT Misc RAW

### BLEDP

FieldName	Card1	Card2	Card3	Card4	Card5	Card6	Card7	Card8
FW Version	0x0214f00a	0x0214f00a	0x0214f00a	0x0214f00a	0x00000000	0x00000000	0x00000000	0x00000000
Chip ID	0xac00001546bbfd01	0xac00001546bbfd01	0xac00001546bbfd01	0xac00001546bbfd01	0x0000000000000000	0x0000000000000000	0x0000000000000000	0x0000000000000000
Geo Address	100	100	100	100	0	0	0	0
Temperature	28.63 °C	28.63 °C	28.63 °C	28.63 °C	0 °C	0 °C	0 °C	0 °C
Humidity	17.79 %	17.79 %	17.79 %	17.79 %	0 %	0 %	0 %	0 %

### BLEPM

FieldName	Card1	Card2	Card3	Card4	Card5	Card6	Card7	Card8
FW Version	0x0214f10a	0x0214f10a	0x0214f10a	0x0214f10a	0x00000000	0x00000000	0x00000000	0x00000000
Chip ID	0xac00001546bbfd01	0xac00001546bbfd01	0xac00001546bbfd01	0xac00001546bbfd01	0x0000000000000000	0x0000000000000000	0x0000000000000000	0x0000000000000000
Temperature	28.64 °C	28.64 °C	28.64 °C	28.64 °C	0 °C	0 °C	0 °C	0 °C
Humidity	18.35 %	18.35 %	18.35 %	18.35 %	0 %	0 %	0 %	0 %

### DAB64x

FieldName	Card1	Card2	Card3	Card4	Card5	Card6	Card7	Card8
FW Version	0x0214f20a	0x0214f20a	0x0214f20a	0x0214f20a	0x00000000	0x00000000	0x00000000	0x00000000
Chip ID	0xac00001546bbfd01	0xac00001546bbfd01	0xac00001546bbfd01	0xac00001546bbfd01	0x0000000000000000	0x0000000000000000	0x0000000000000000	0x0000000000000000
Geo Address	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Temperature	37.5 °C	37.5 °C	37.5 °C	37.5 °C	0 °C	0 °C	0 °C	0 °C

Stop





# Expert Application – Diagnostics 1/2

BLMINJExpertGUI2 (on cwe-513-vml245.cern.ch)

File Configuration Help

Host Selection: cvt-865-blm5

Global Device: GD\_F69823D4

Devices: DevFamily1

0	ALL	5	LHC1B	10	LHCINDIV	15	MD4	20	SFTPRO1	1	SFTPRO1	1	4	NORMCPS	4	7	ZERO	7	10	ZERO	10	13	SFTPRO1	13	16	SFTPRO1	16	19	ZERO	19	21		23
1	AD	6	LHC2A	11	LHCPRDRE	16	MD5	21	SFTPRO2	2	ZERO	2	5	ZERO	5	8	MD5	8	11	SFTPRO1	11	14	NORMCPS	14	17	NORMCPS	17	20		22		24	
2	EAST1	7	LHC2B	12	MD1	17	MD6	22	STAGISO	3	MD6	3	6	SFTPRO1	6	9	NORMCPS	9	12	ZERO	12	15	ZERO	15	18								
3	EAST2	8	LHC3	13	MD2	18	NORMCPS	23	TOF																								
4	LHC1A	9	LHC4	14	MD3	19	NORMHRS	24	ZERO																								

MD6

Acquisition Thresholds Capture Evolution Setting Status Combiner Diagnostics

General Analog SFPs Graph IL BLEDP IL BLEPT Misc RAW

BLEDP SFP1

FieldName	Card1	Card2	Card3	Card4	Card5	Card6	Card7	Card8
Part Number	FT3A05D	FT3A05D	FT3A05D	FT3A05D				
Temperature	10.97	10.97	10.97	10.97	0	0	0	0
VCC	1584	1584	1584	1584	0	0	0	0
TX Power	225.6	225.6	225.6	225.6	0	0	0	0
RX Power	0	0	0	0	0	0	0	0
TX Bias	3040	3040	3040	3040	0	0	0	0
Warnings								

LOSS\_OF\_SIGNAL

BLEDP SFP2

FieldName	Card1	Card2	Card3	Card4	Card5	Card6	Card7	Card8
Serial Number	120512016	120512016	120512016	120512016				
Part Number	FT3401G	FT3401G	FT3401G	FT3401G				
Temperature	0	0	0	0	0	0	0	0
VCC	0	0	0	0	0	0	0	0
TX Power	0	0	0	0	0	0	0	0
RX Power	0	0	0	0	0	0	0	0
TX Bias	0	0	0	0	0	0	0	0

BLEPM SFP1

FieldName	Card1	Card2	Card3	Card4	Card5	Card6	Card7	Card8
Serial Number	130601016	130601016	130601016	130601016				
Part Number	FT3A05D	FT3A05D	FT3A05D	FT3A05D				
Temperature	10.97	10.97	10.97	10.97	0	0	0	0
VCC	1584	1584	1584	1584	0	0	0	0
TX Power	225.6	225.6	225.6	225.6	0	0	0	0
RX Power	0	0	0	0	0	0	0	0
TX Bias	3040	3040	3040	3040	0	0	0	0

BLEPM SFP2

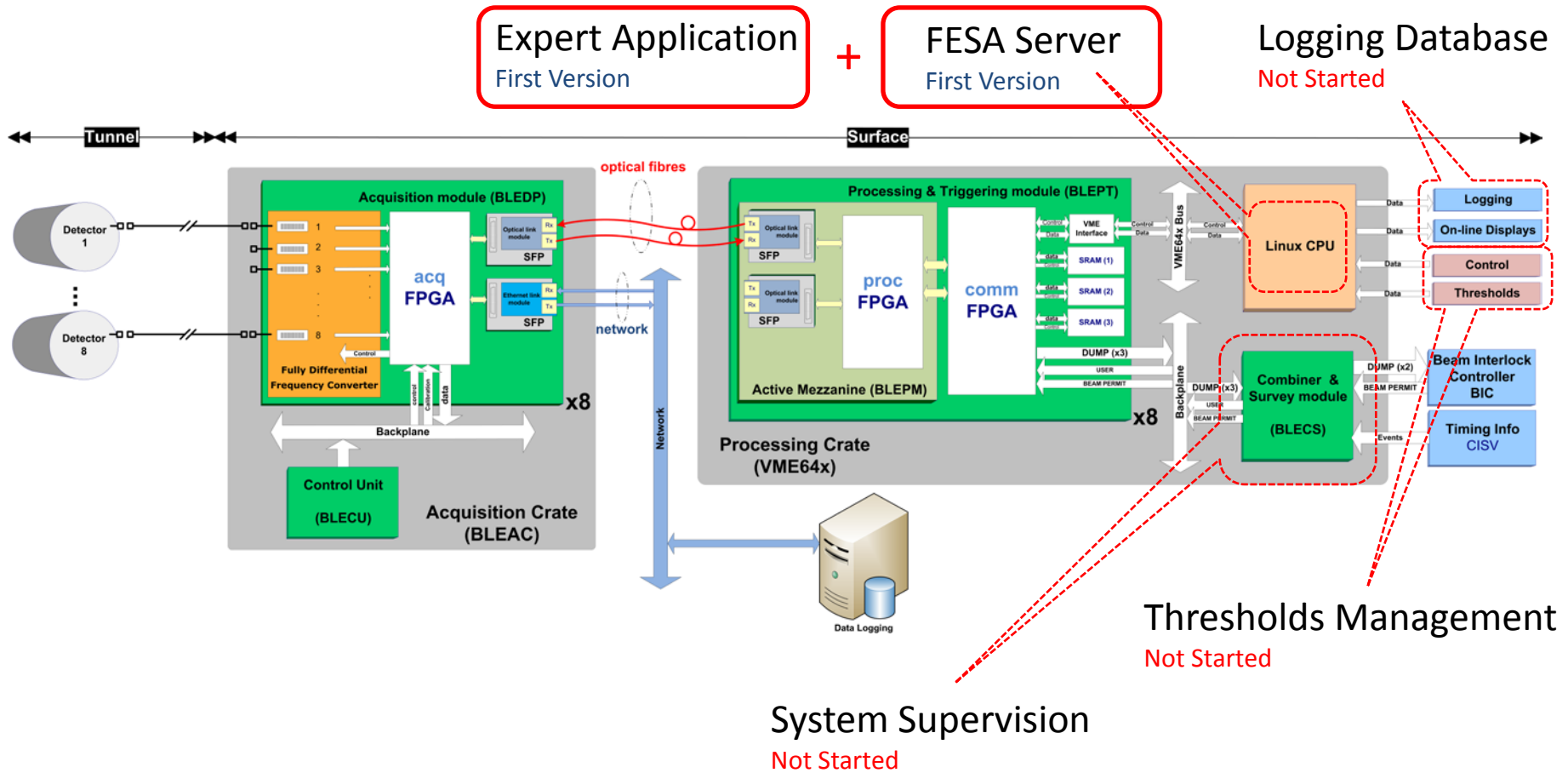
FieldName	Card1	Card2	Card3	Card4	Card5	Card6	Card7	Card8
Serial Number	130512016	130512016	130512016	130512016				
Part Number	FT3401G	FT3401G	FT3401G	FT3401G				
Temperature	0	0	0	0	0	0	0	0
VCC	0	0	0	0	0	0	0	0
TX Power	0	0	0	0	0	0	0	0
RX Power	0	0	0	0	0	0	0	0
TX Bias	0	0	0	0	0	0	0	0

Stop





# FPGA Development (4/4)





# Summary

- First part of PSB Ring system is complete
  - All detectors are installed
  - All cables and connections have been verified
- PCB production is on schedule
  - Pre-series to be delivered on Nov14
  - Series to be produced in 2016
- FPGA & FESA development advanced
  - Major functions in firmware and software available
  - Now testing complete measurement line (i.e. from acquisition to data publish)
  - **Several functions to be developed (e.g. self-diagnostic, statuses, interlock)**
- Next steps:
  - Logging database
  - Threshold management
  - Operational applications