CMS Pixel Phase I Upgrade

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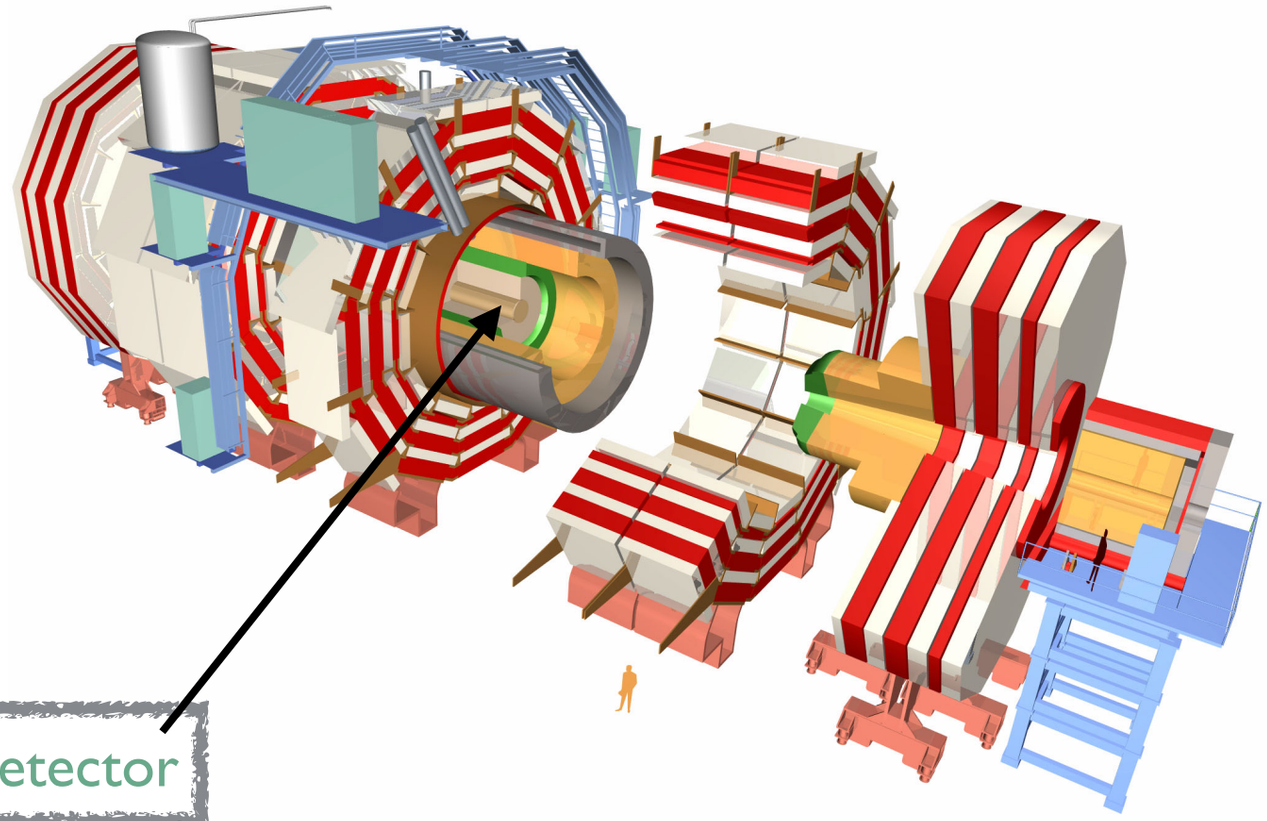
SPS Annual Meeting, Fribourg 30.06-02.07 2014

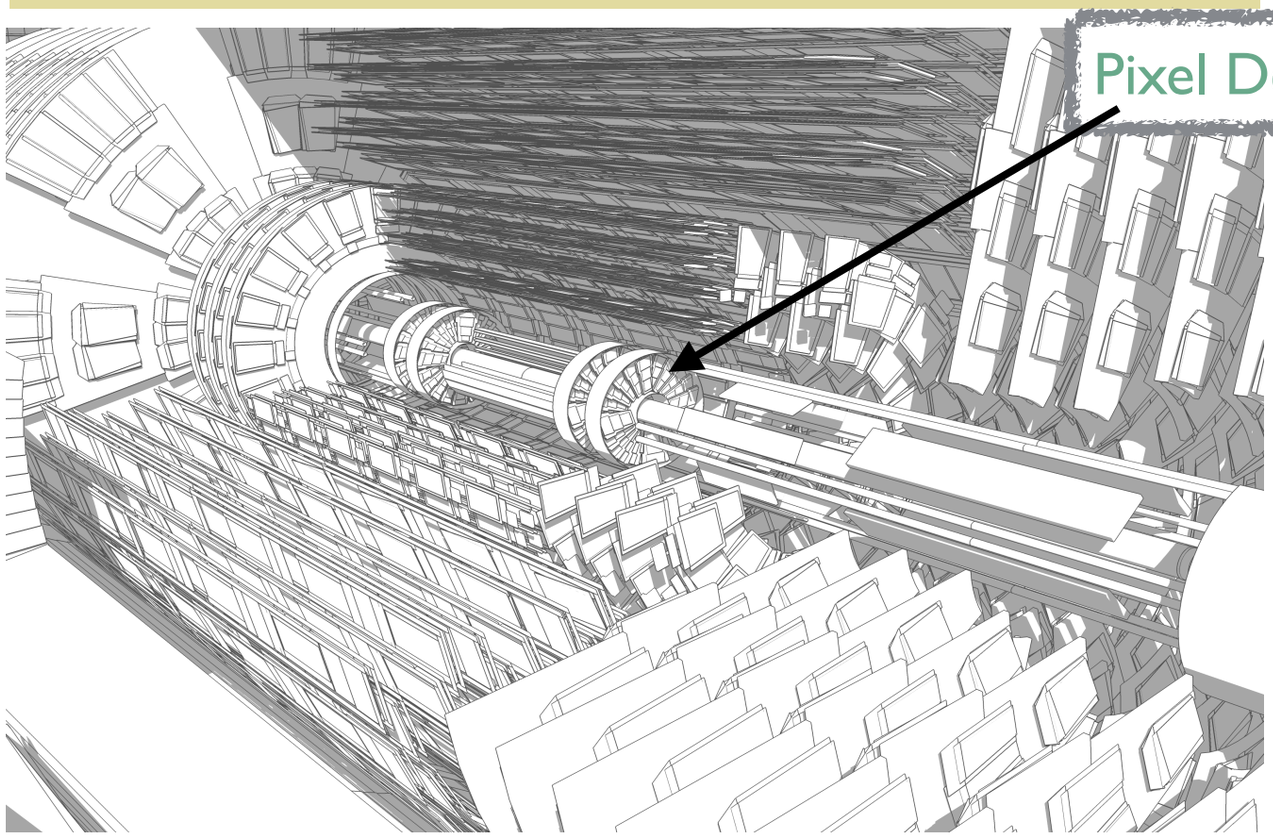
Overview

- CMS Pixel detector
- CMS Upgrade
- Improvements
- State of the art
- Conclusions

CMS Pixel Detector

- Innermost component of CMS, **close to interaction point** (r=4.4 to 10.2 cm for barrel)
- **pivotal role** in tracking syst, primary/ secondary vertex, b-tag, e/γ separation, pattern recognition
- layer structure provides **3D track reconstruction** for charged particles



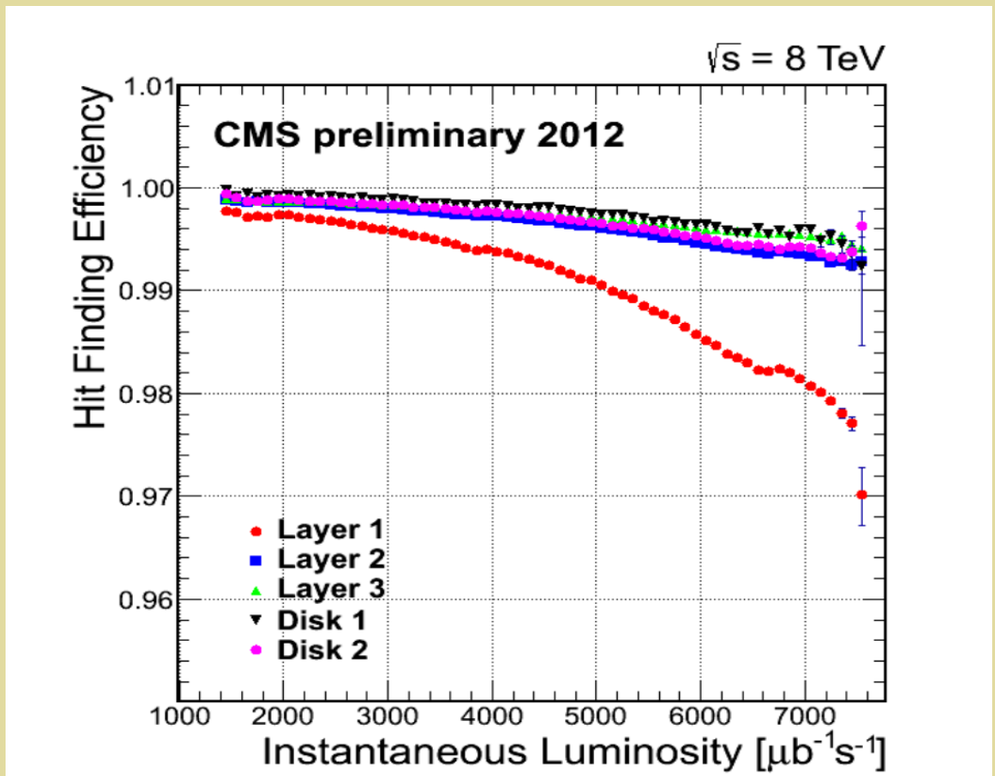


Current Pixel System

- 3 barrel layers (BPIX, 48 M pixels)
- 2+2 forward endcaps (FPIX, 18 M pixs)
- Pixel size 100x150 μm → resolution ~10 μm in rφ, ~20 μm in z

Pixel Upgrade: challenges

- Current pixel detector designed for maximum $\mathbf{L_{inst} = 1x10^{34}cm^{-2}s^{-1}}$ (exp. 2015) → at more extreme conditions performance will **deteriorate!**
- @ $L_{inst} = \mathbf{2}x10^{34}cm^{-2}s^{-1}$ (by 2018) Expected inefficiency for Layer 1:
  at 25ns bunch crossing freq: **16%**
  at 50ns bunch crossing freq: **50%**



Inefficiency mainly due to:

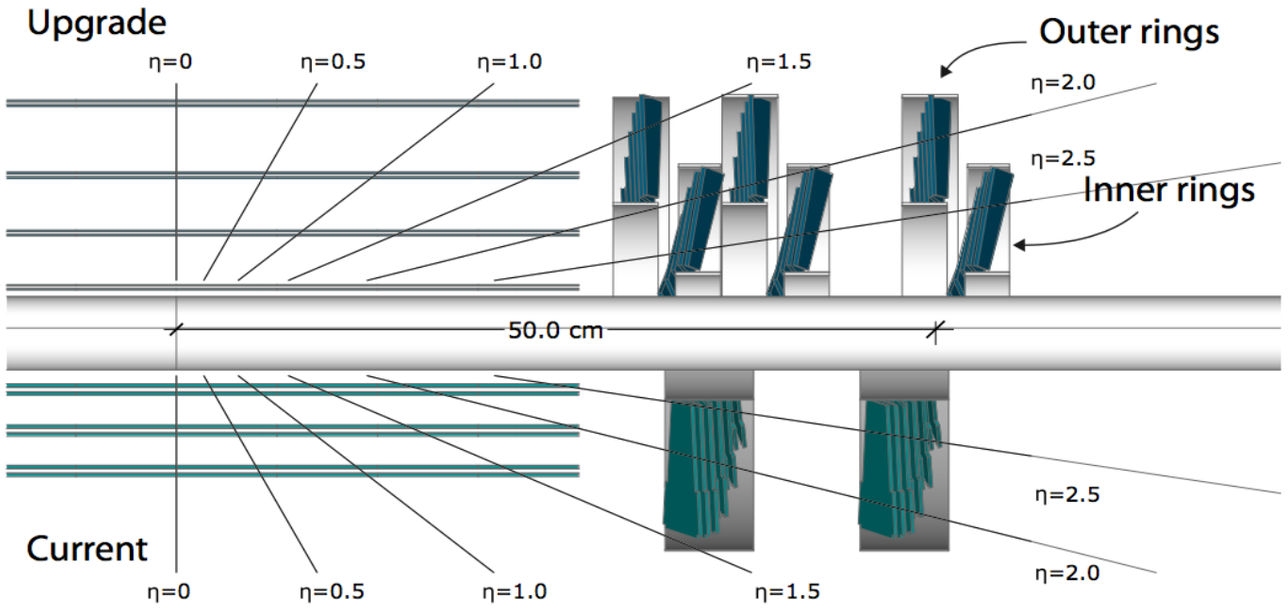
- time stamp and data buffer overflows in the ReadOut Chip (ROC)
- limits in transfer of hits to readout chain

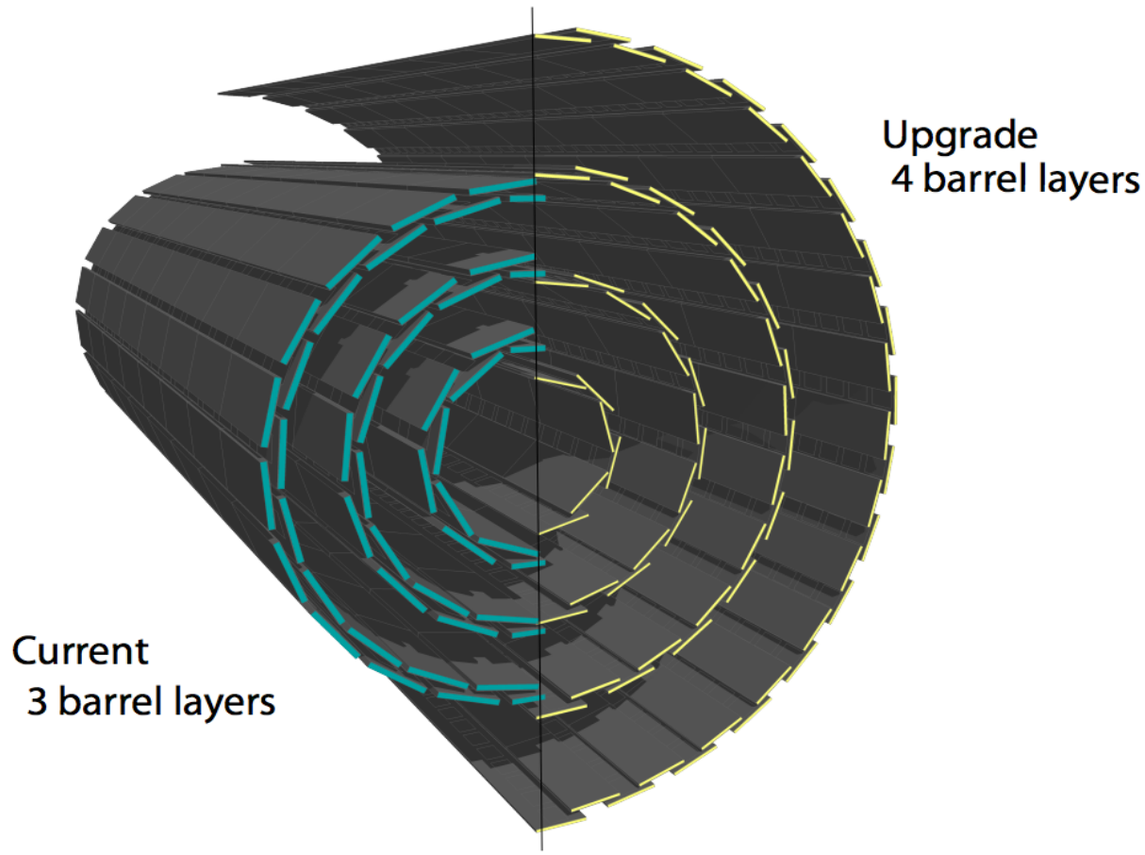
Additional: radiation damage in the sensor causes charge collection reduction and hence loss of spatial resolution

Phase I Upgrade:

- ✦ time constraints: ready by 2018 2016/17 extended end year stop
- ✦ keep current services
- ✦ maintain current pixel performance (high eff, low fake-rate, resolution) even at 50 interactions per bunch-crossing (PU)

Pixel Upgrade: structure



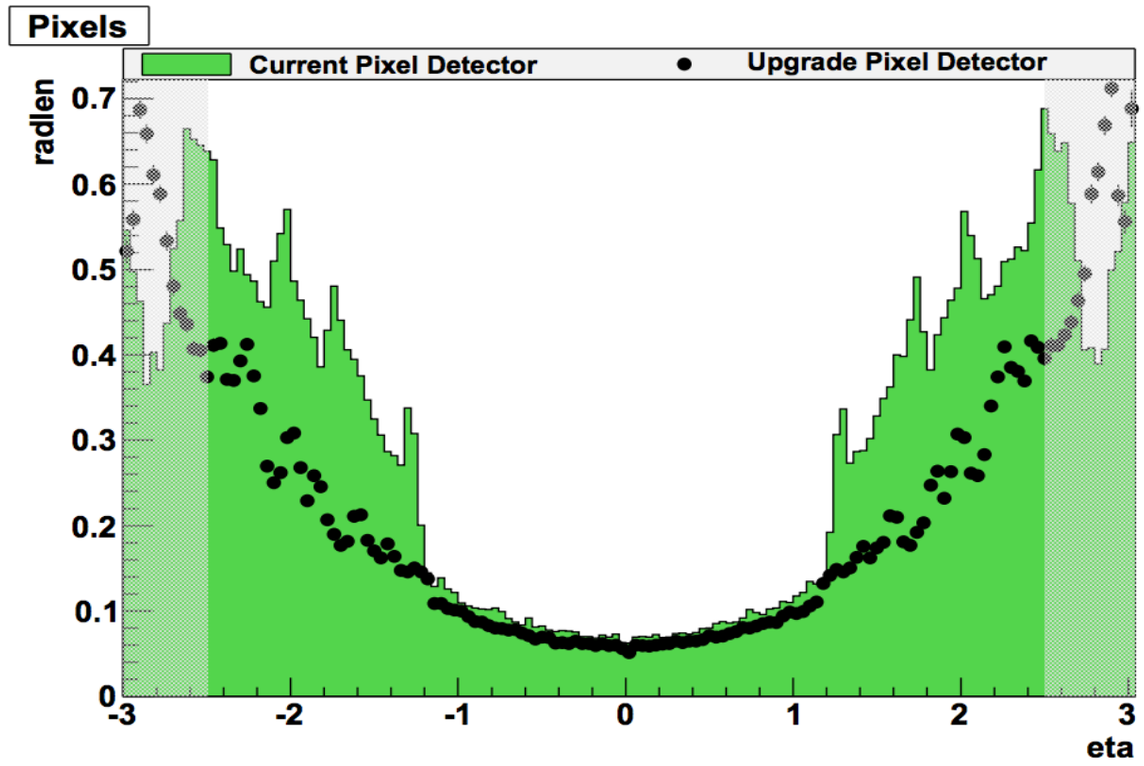


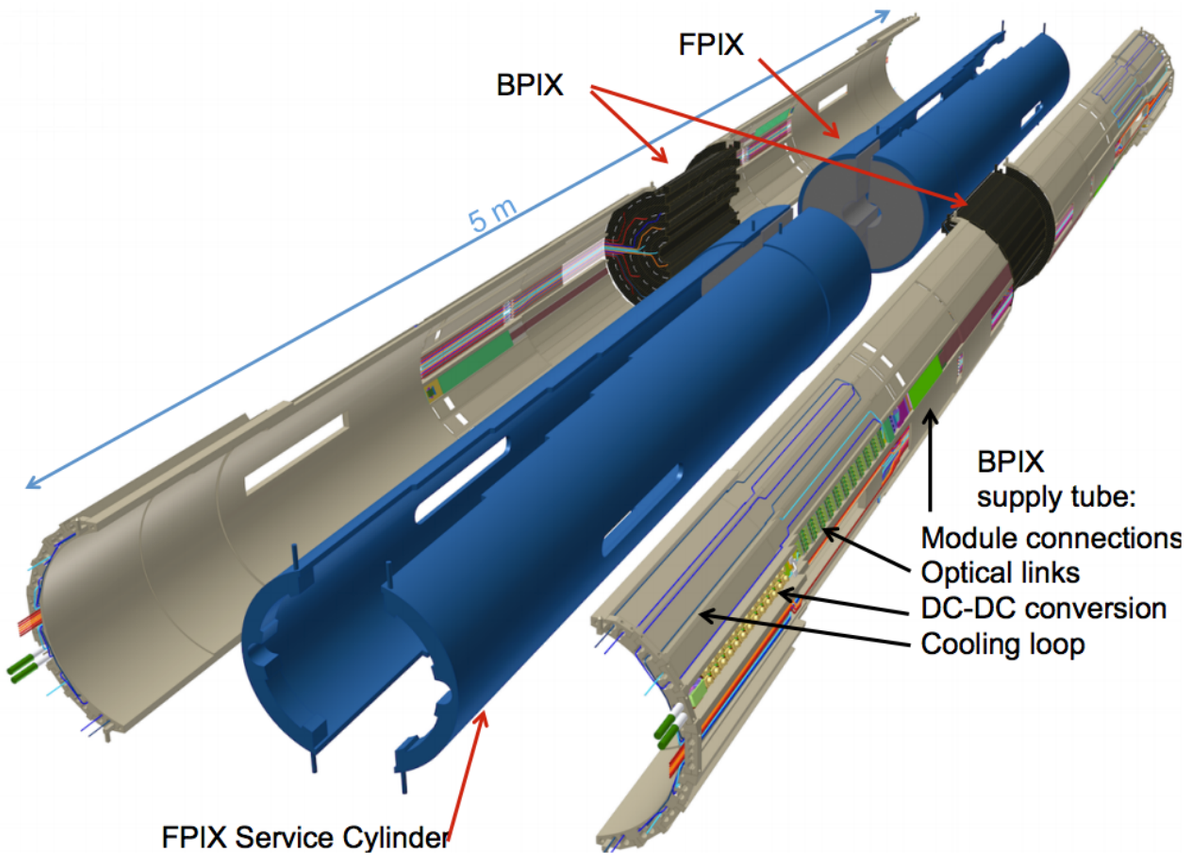
- Optimized layout **4-hit** coverage for η=±2.5 range
  - 4th BPIX layer: 48M → **79M pixel**
  - 3rd FPIX disc: 18M → **45M pixel**
- **Recovery of degradation** in inner strip tracker layers

- Improved **efficiency and resolution** for pixel-only tracks
  - High Level Triggering
  - full track seeding: higher full track efficiency & lower fake rate
  - Vertexing primary and secondary

Material

- One more layer (disc) wrt to current detector in BPIX (FPIX)
  → ~50% more modules
  Nevertheless:
- upgrade/current BPIX mass ratio = 0.40
- upgrade/current FPIX mass ratio = 0.82





- More layers but less material!
- Thanks to:
  - moving passive material out of tracking volume
  - new two phase CO_2 cooling system (current C_6F_{14})
    → low mass and smaller pipes

Other changes

New Digital ReadOut Chip:

- current analog ROC is major bottleneck for readout efficiency
- increased buffers, readout speed, better radiation hardness, …

see next talk after the break …

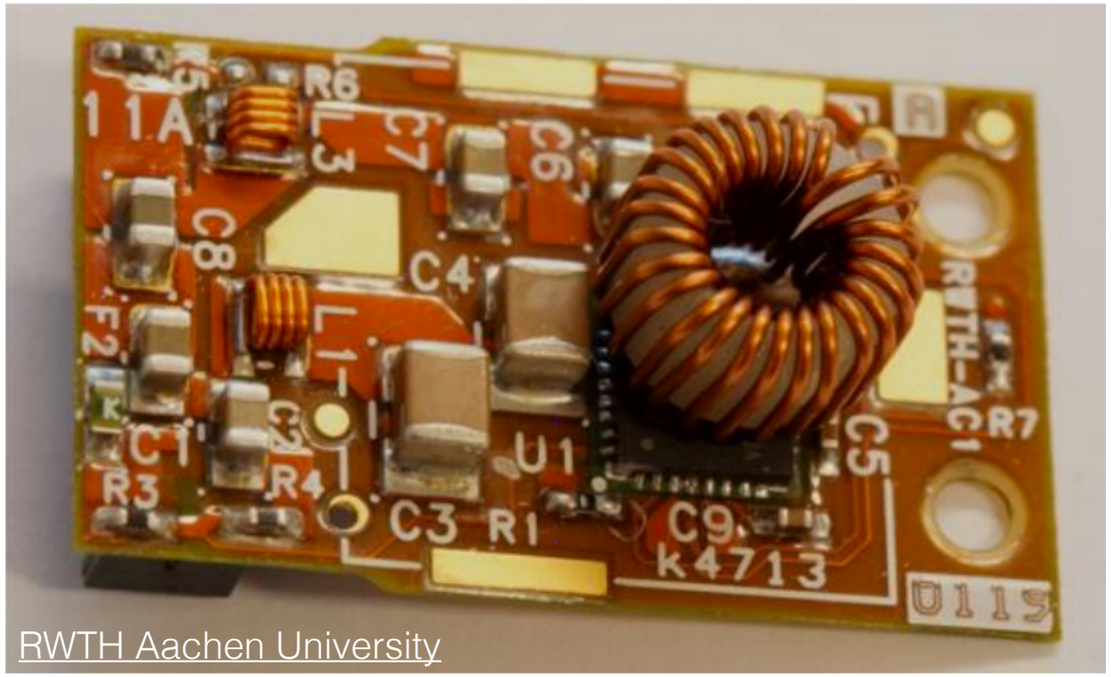
Cooling system:

- bi-phase CO_2 cooling system replacing monophase C_6F_{14}
- system occupies a smaller volume, but it's able to cool down a larger volume

Power supply:

- higher amount of modules
- higher voltage required by new ROCs **more power!**
- supply infrastructure cannot be upgraded

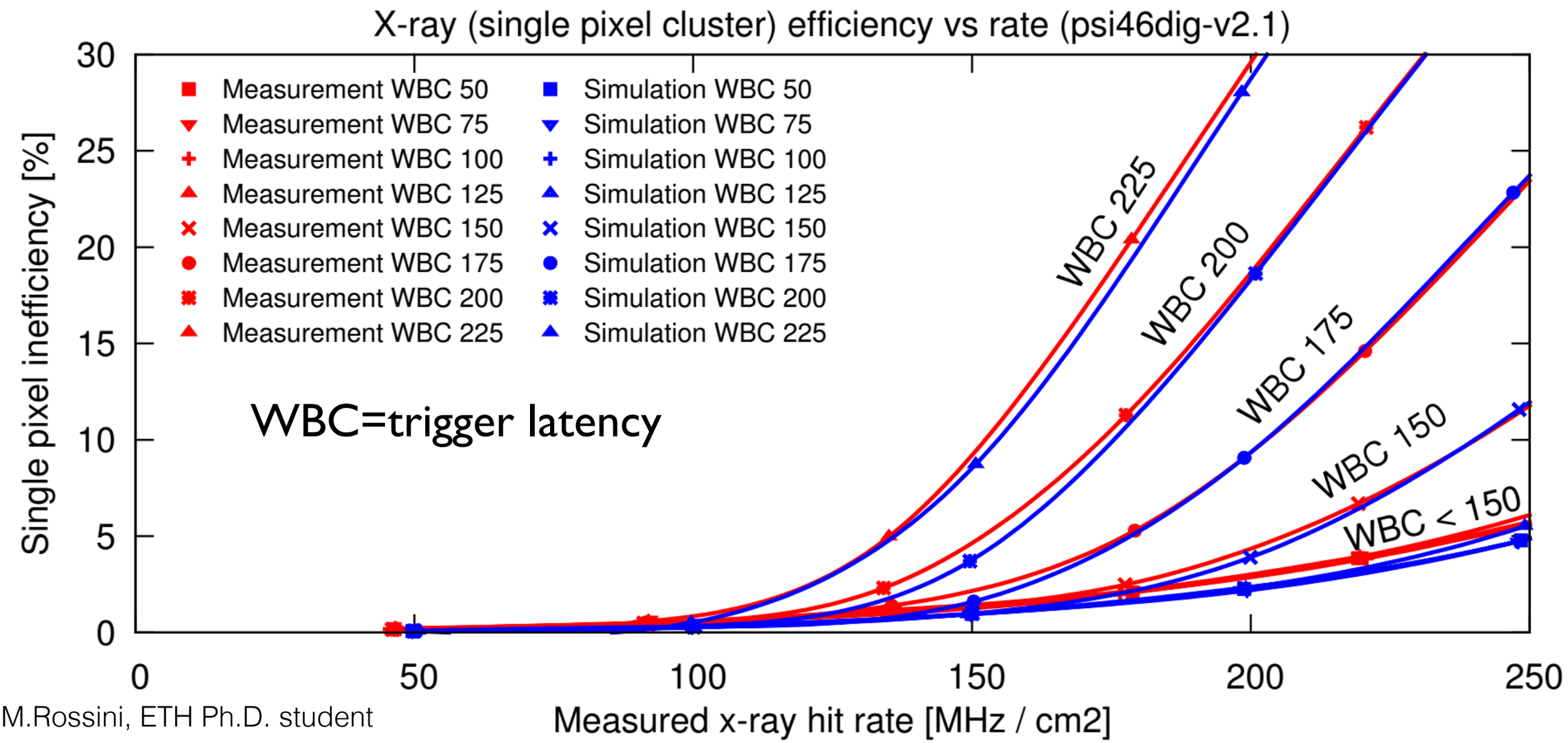
→ DC-DC converters close to the detector



RWTH Aachen University

Efficiency at high fluxes

Single pixel efficiency **simulated** and **measured** at ETH
Measurements performed with high rate x-ray background using internal calibration signal of the chip



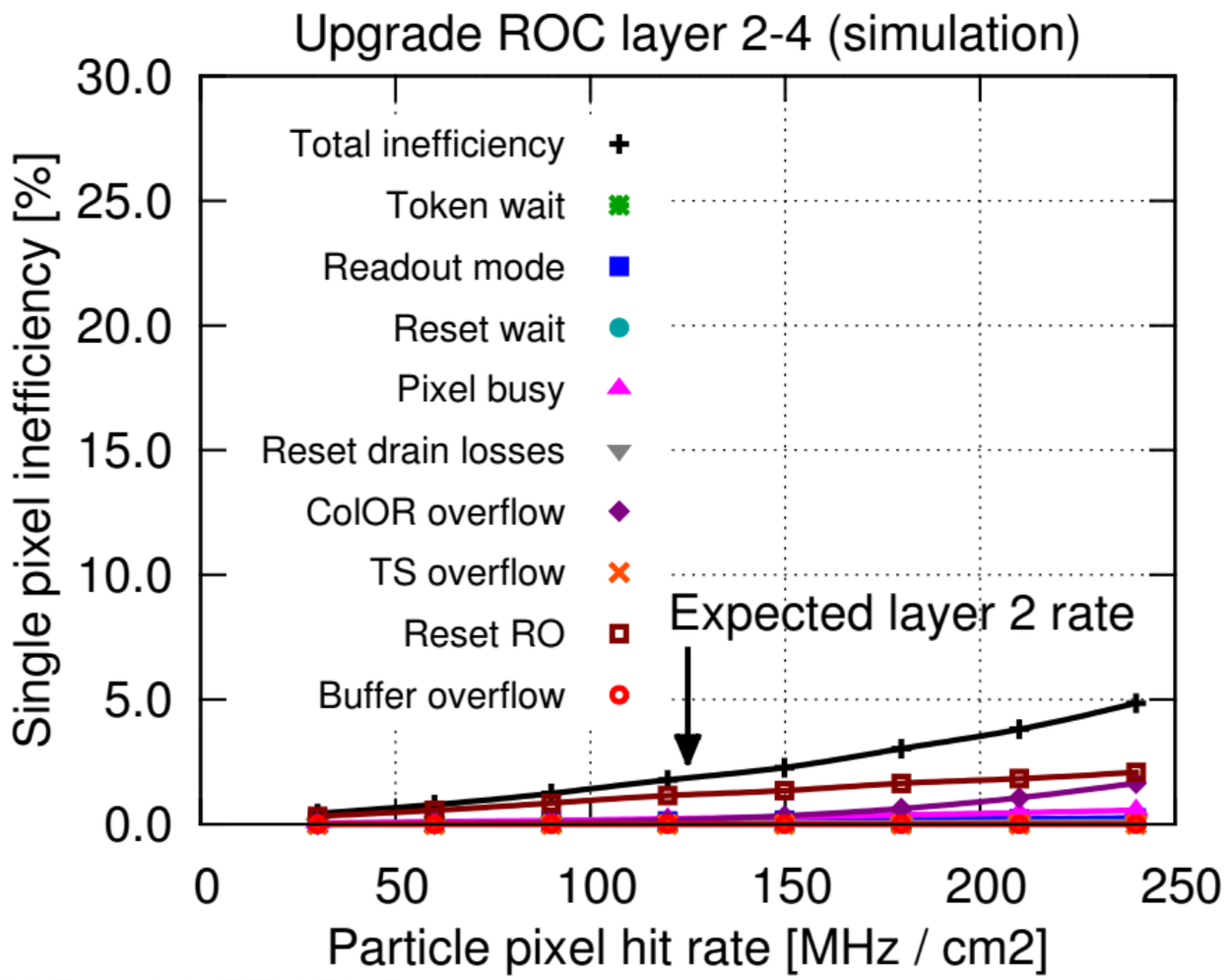
M.Rossini, ETH Ph.D. student

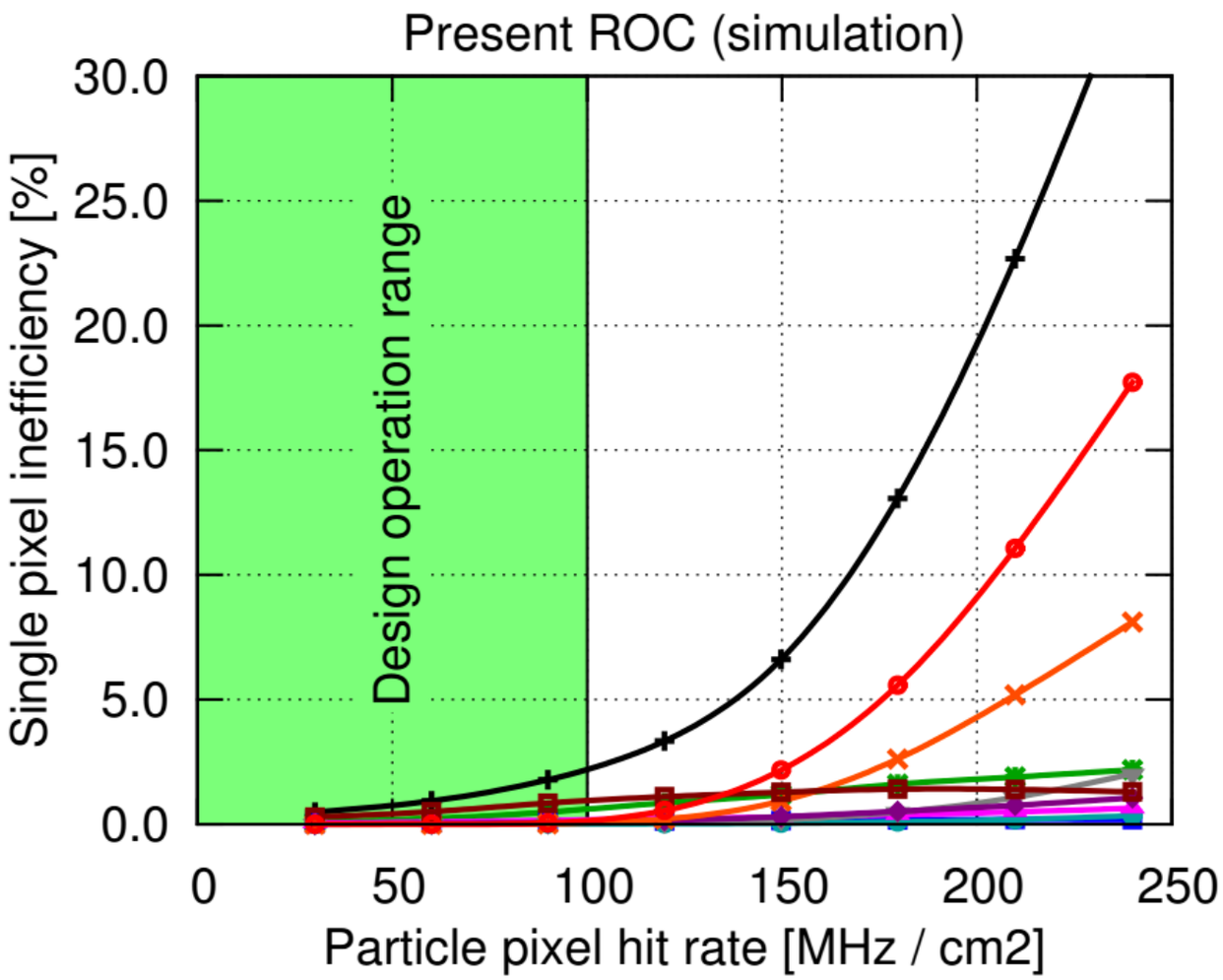
Efficiency at high fluxes: particles

Simulating **particle** high flux through detector:

- CMS trigger latency ≈ WBC 153
- expected flux for L2≈ 120 MHz/cm^2

New ReadOut Chip shows significantly smaller inefficiencies at high rates than current one!





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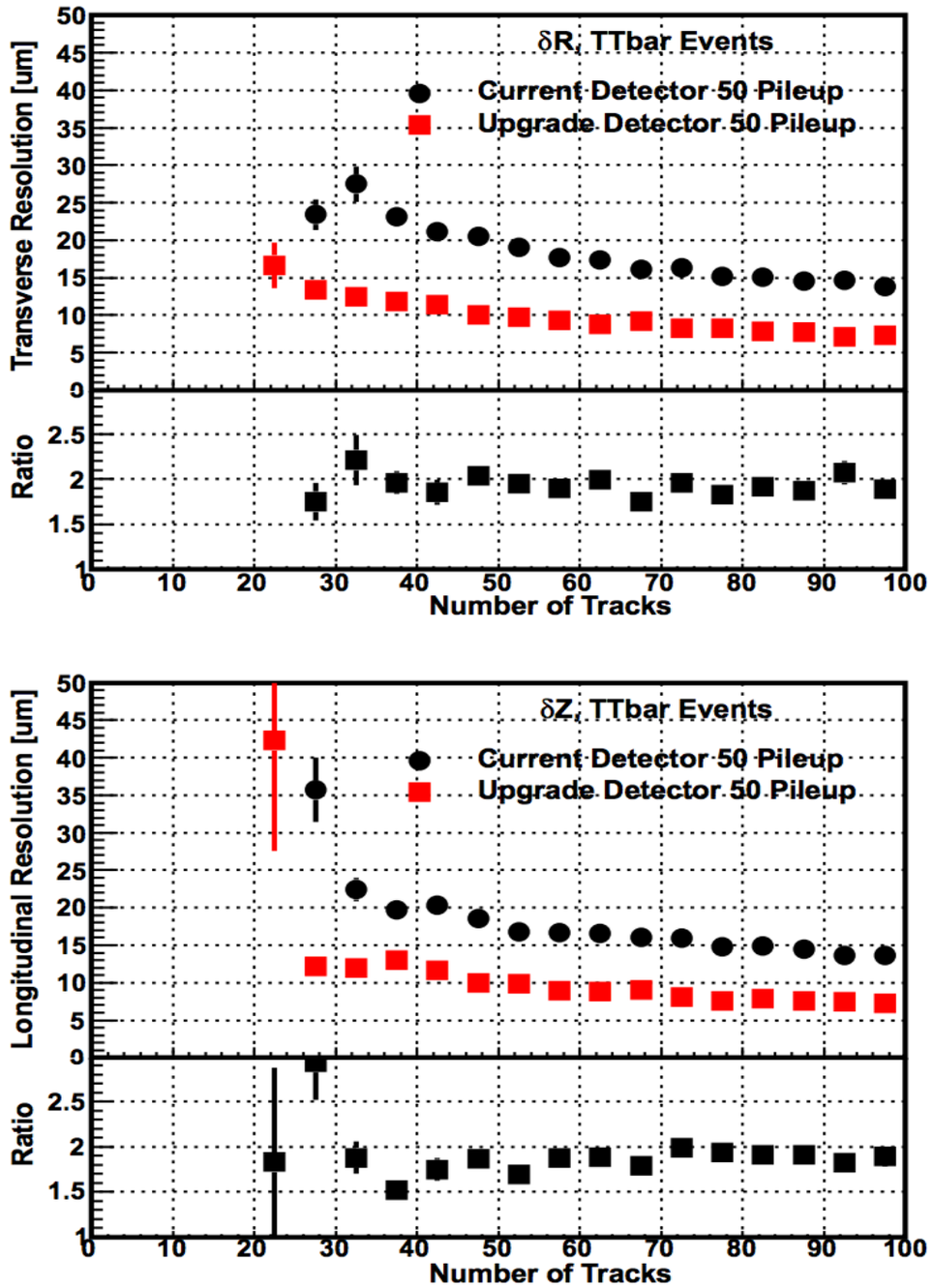
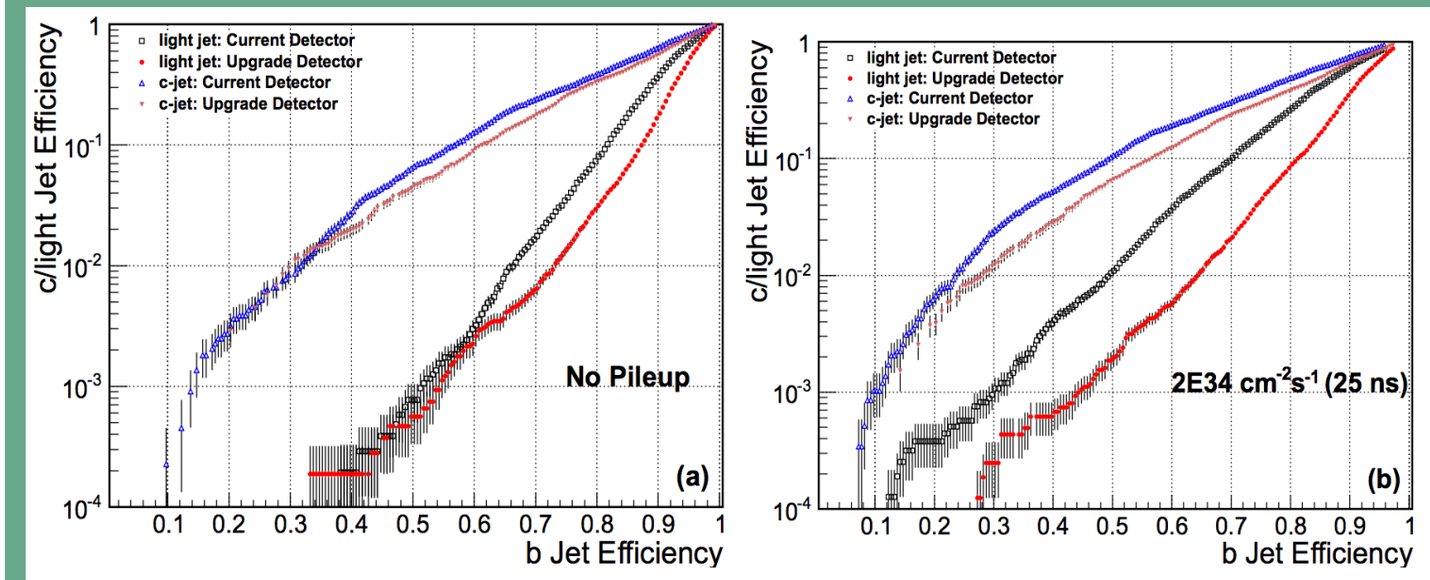
Performances

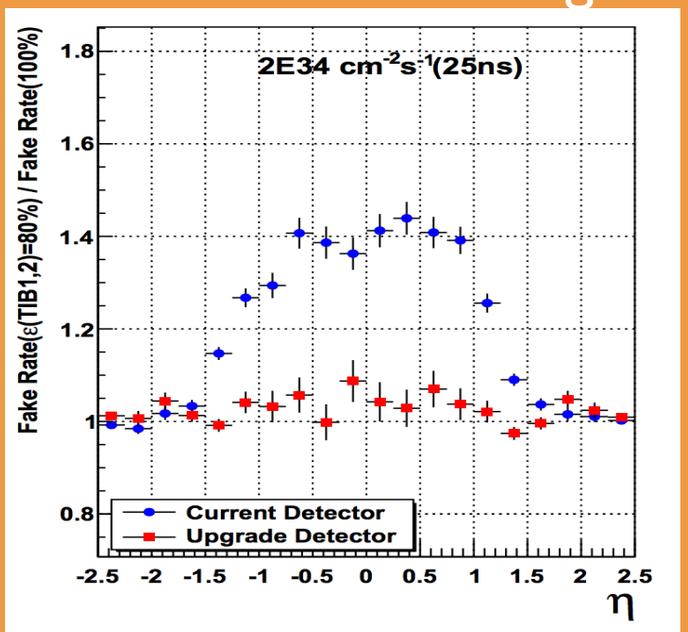
Primary vertex resolution

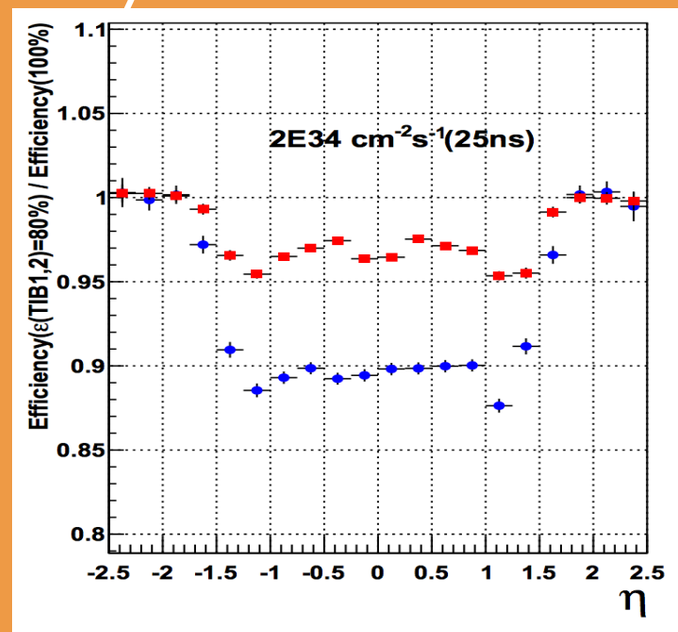


b-tagging



Fake rate and tracking efficiency

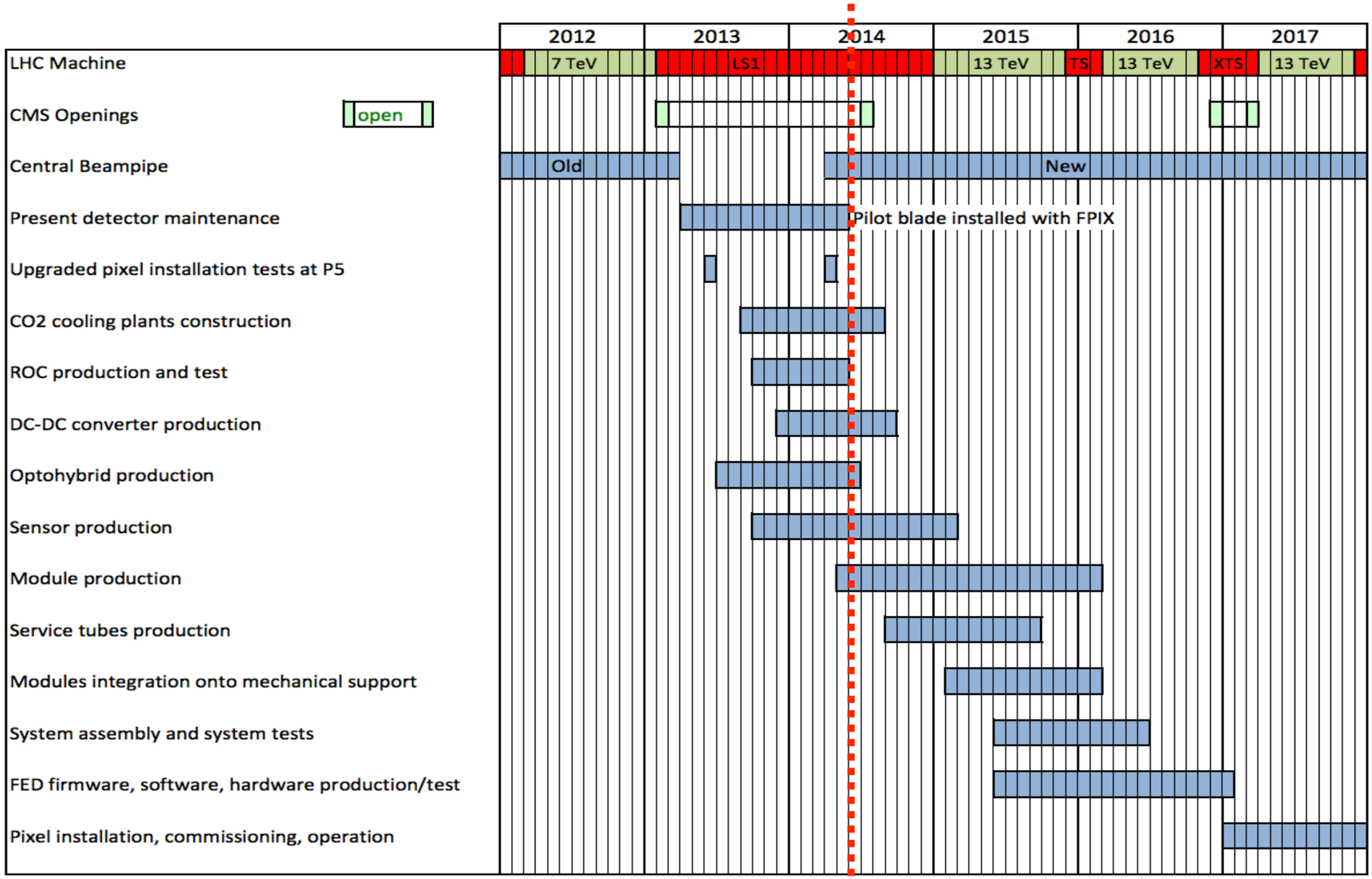




Current&Upgrade: summary

Parameter of Pixel System	Current	Upgrade
# layers	3	4
Beam pipe radius (outer)	29.8 mm	22.5 mm
Innermost layer radius	44 mm	29.5 mm
Outermost layer radius	102 mm	160 mm
Pixel size (r-φ x z)	100 μm x 150 μm	100 μm x 150 μm
Pixel resolution (r-φ x z)	13 μm x 25 μm	13 μm x 25 μm (or better)
In-time threshold	3500 e^-	1500 e^-
Cooling system	$C_6 F_{14}$ (monophase)	CO_2 (biphase)
Material budget X/X_0 (η=0)	6%	5.5%
Material budget X/X_0 (η=1.6)	40%	20%
Pixel data readout speed	40 MHz (analog)	400 Mb/s (digital)
Readout chip pixel rate capability	~120 MHz/cm^2	~580 MHz/cm^2

Timeline and where we are now



Swiss Consortium (ETHZ, PSI, UZH): ROC design and testing, supply tube, CO_2 cooling, L1 and L2 modules production and testing

Conclusions

- Pixel detector Upgrade essential to keep current physics performances at higher luminosities
- Upgraded detector allows for more robust tracking and radiation hardness
- State of the art meets the schedule, entered the module pre-production phase

Backup

2015
2016
2017
2018
2019
2020
2021
Q1 Q2 Q3 Q4
LHC Injectors
Run 2
LS 2
Run 3
2022
2023
2024
2025
2026
2027
2028
LS 3
Run 4
2029
2030
2031
2032
2033
2034
2035
LS 4
Run 5
LS 5

Efficiency simulation

Simulation describes one double column.

Input parameters:

- number of pixels
- buffer sizes
- signal delays
- hit rate
- trigger rate
- trigger latency
- cluster size distribution
- bunch spacing
- simulation time

During the simulation, hits and triggers are randomly generated. Different mechanisms of data loss can be identified:

- **Token wait, readout mode, reset wait**: during readout and reset no hits are read out.
- **Pixel busy**: an activated pixel waiting to be read cannot receive further hits
- **Bunch crossing migration**: hits during two pending column drains can be assigned to a previous bunch crossing. Hits during a Time Stamp buffer overflow are assigned to a later bunch crossing.
- **Reset loss**: after a readout or when a buffer overflow occurs, the DC is reset.