

# TTC upgrade Status

May 2006

- Overview
- AB/RF optical links
- Receiver crate
- Status and schedules
- Documentation

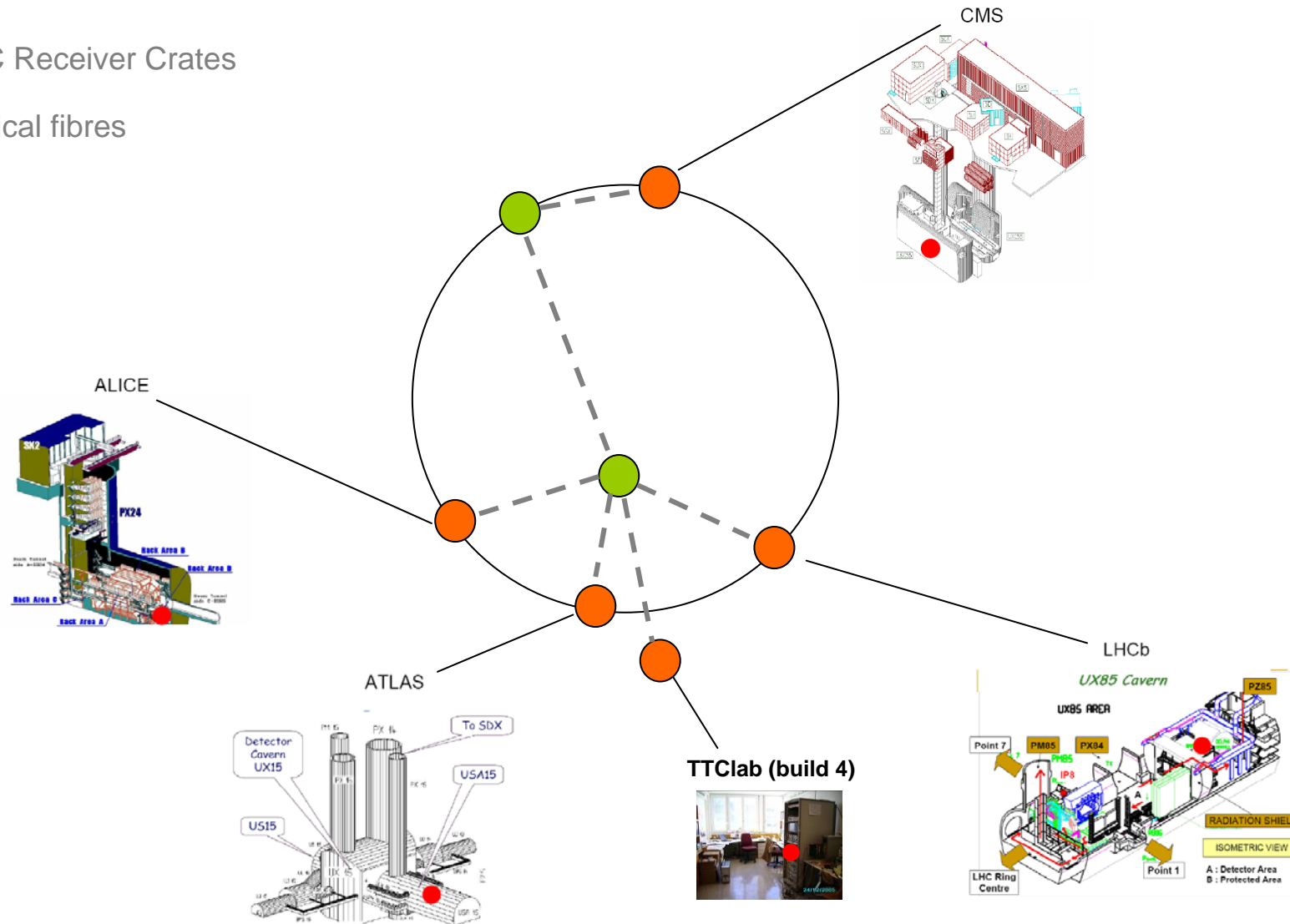
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# OVERVIEW

● AB/RF Tx and Rx modules

● TTC Receiver Crates

- - Optical fibres



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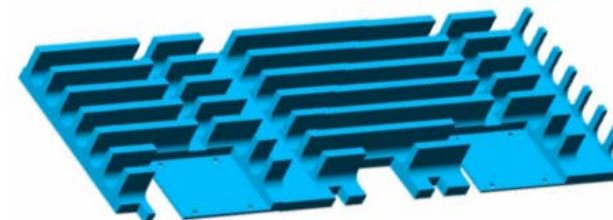
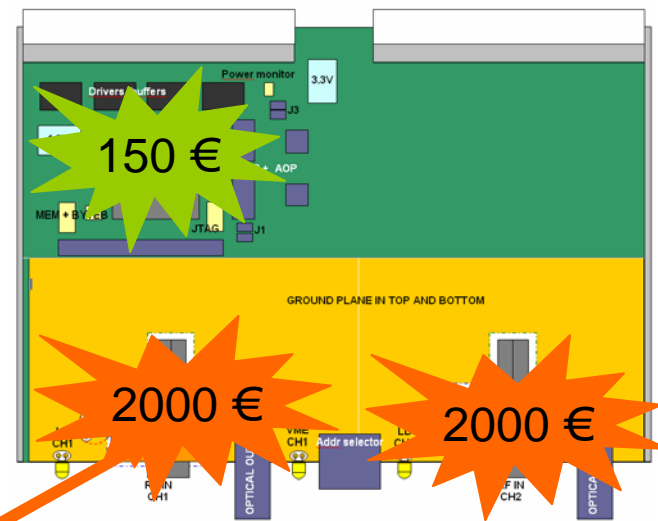
# AB/RF OPTICAL LINKS [Analog solution]

- **Analog Modules**
  - Transmitter module: [RF Tx A](#) (EDA-01331)
  - Receiver module: [RF Rx A](#) (EDA-01332)
- **6U 4TE VME (VME 64x and VME 64 compatible)**
  - 3 internal registers
    - Power warning led threshold (RW)
    - CH/2 1Power monitoring (Read Only)
- **Miteq links 3GHz**
  - validated - [Specs](#):
    - Measured Phase Noise:
      - 400MHz -> 0.4ps (pkpk)
      - 40MHz -> 0.4ps (pkpk)
      - 10MHz -> 13ps (pkpk)

*More results in the [evaluation report](#)*
    - Typical output levels:
      - Bunch Clock = 0dBm continuous sinewave
      - Orbit = 1Vpk pulse on 50 Ohms
    - Quantities:
      - 10 links have been ordered in November05
      - 10 to be ordered soon
      - => Enough to work until 2007



# AB/RF OPTICAL LINKS [Analog solution]



# RECEIVER CRATE [Digital Solution]

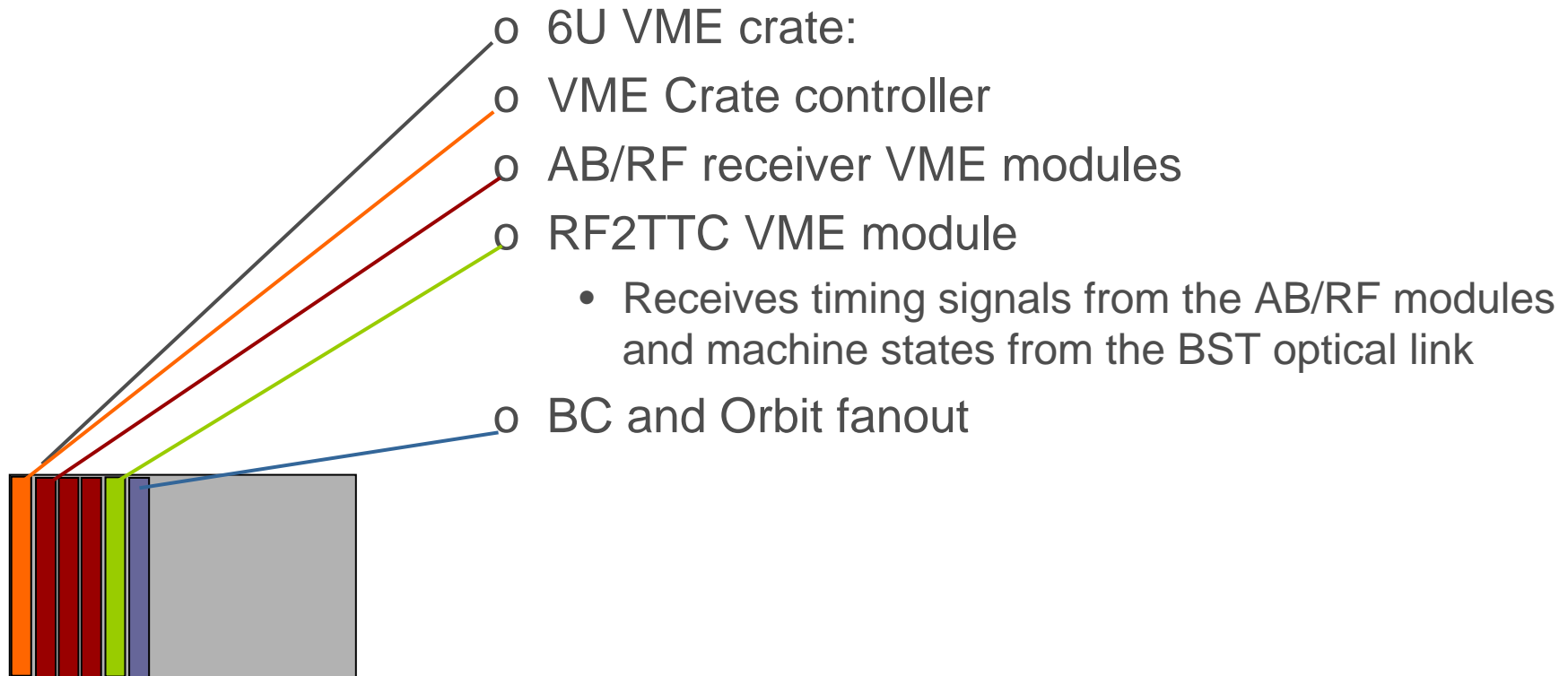
- We tried to find a cheaper solution with the same form factor
- Digital Modules (RF\_Tx\_D and RF\_Rx\_D)
  - o First test boards made with PHOTON 155Mbps/TRR-1B43 pair
    - Standard modules of the TTC modules
    - Performance evaluated on the same setup than the analog links
    - Results available in the [test report](#)
    - AB/RF agreed that this could be a cheaper solution for 70% of the links, including the TTC
    - If the final results are as good as expected, they will use this solution for these 70% and maintain the boards the same way.
  - o Optical components identified and ordered
    - [Photon](#) getting obsolete
    - [OCP components](#) pin compatible components
    - Price:
      - Orbit, 10MHz, 40MHz: 156Mbps links
      - 400MHz: 1.2Gbps
  - o Design on-going (PH/ESS).
    - Close to the analog boards, but higher density.

	Tx	Rx
156Mbps PHOTON	197	97
156Mbps AMS	313	227
1.2Gbps AMS	635	295

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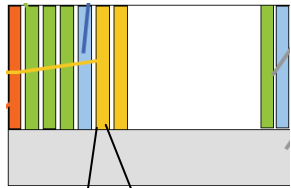
# RECEIVER CRATE [Overview]



# RECEIVER CRATE [Crates – Power Supplies - Controllers]

- Provided by PH/ESS
- Common Crates:
  - 1 LHC standard 6U VME 64x crate per experiment
  - Available
- (less) Common Power supplies:
  - (+3.3V/100A, +5V/100A, +-12V/10A, 48V/12A)
  - ATLAS, CMS, LHCb: OP06.0710
  - ALICE: OP17.0701
- (no) Common Controllers:
  - ALICE: Standard VP315/317 from CCT
  - ATLAS, TTC lab: Standard VP110 from CCT
  - CMS: CAEN PCI-controller card A2818 + V2718 VME-PCI optical bridge
  - LHCb:CAEN V1718 VME-USB bridge
  - POOL items. One of each will be reserved as from August 06.

# RECEIVER CRATE [TTC Clock fanout]



- TTC Clock fanout (EDA-01240-V1, PH/MIC)
  - Dual 1:18 ECL fanout
  - 4 NIM outputs per input (ALICE requirement)
  - 1 status led per input (presence of clock).
  - Maximum density
  - The 2 dual modules can be daisy chained.
  - Fully AC coupled

## Prototype produced and debugged

- Power: 5V-5A,
- Jitter: In/Out skew=8ps rms, Cy2Cy=11ps rms
- Skew between outputs: a few ps

Production will begin after full validation & design modifications

# RECEIVER CRATE [RF2TTC overview]



- VME64x - 6U – 4TE module
- Inputs
  - 3 BC inputs (BC1, BC2, BCref) (RF signals)
  - 2 Orbit inputs (Orb1, Orb2) (RF signals)
  - 1 Optical input for the BST signals
- Outputs
  - 4 ECL BC outputs (BC1, BC2, BCref, MainBC)
    - AC coupled
    - 4 NIM copies
  - 3 NECL Orbit outputs (Orb1, Orb2, MainOrb)
    - DC coupled
    - Synchronised respectively to BC1, BC2, MainBC
    - 3 NIM copies
- Status leds

# RECEIVER CRATE [RF2TTC functionalities]

## Adjustable parameters (via VME registers)

### o BC1, BC2, BCref, MainBC

- Adjustable level on the comparator input (BC1, BC2 and BCref)
- Multiplexing between each input and the internal 40.078MHz clock
- Adjustable phase shift (steps of 0.5ns)

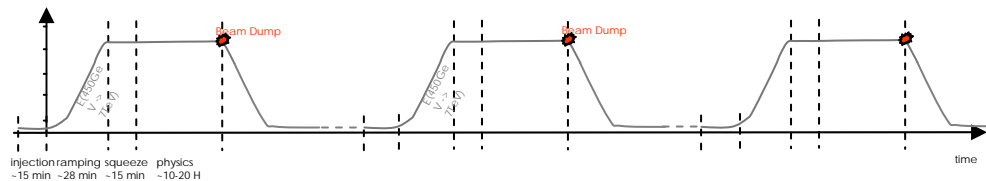
### o Orbit1, Orbit2, Main Orbit

- Adjustable level on the comparator input to match various types of signals (Orb1 and 2)
- Adjustable phase shift before the latching with the corresponding BC (Orb1 and 2)
- Multiplexing between each input and an internal counter
- Adjustable length, coarse delay (steps of 25ns), phase shift (steps of 0.5ns) before the output

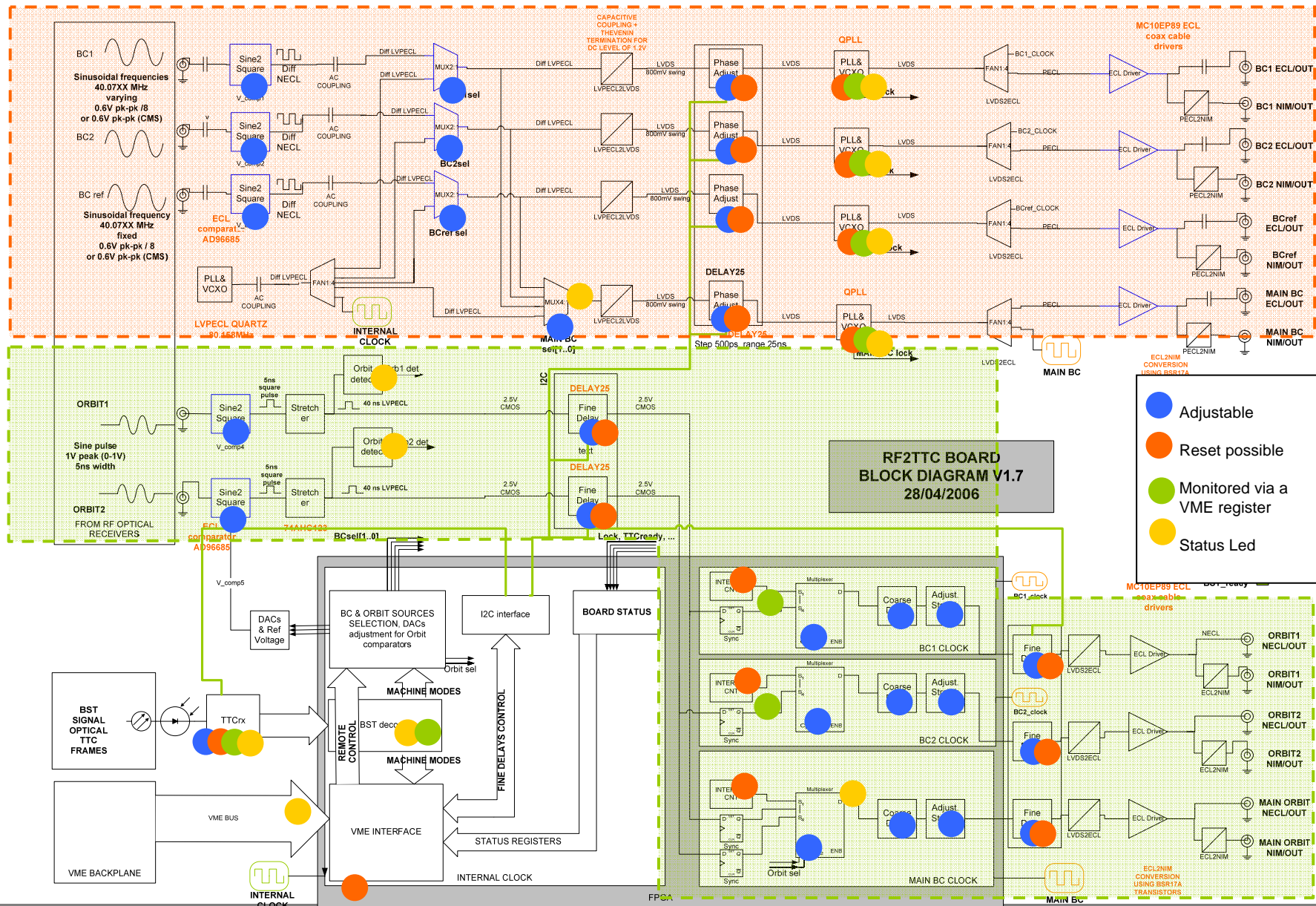
## Status control

- o Status registers (locking BC, BST ready, machine modes, Orbit alignment)
- o Leds

## Manual or automatic mode to switch between the internal clock (orbit) and one of the machine clock (orbit)



# RECEIVER CRATE [RF2TTC block diagram]



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# STATUS & Schedules

	Modules	Specs	Component choice	Schematics	Review	layout	Firmware	Software	Components ordering	Prototype	Validation	Production	
AB/RF modules	Analog Tx and Rx							NOW		NOW	JUNE-SEPT (test beam)	Oct	
	Digital Tx and Rx		NOW					NOW					
Receiver Crate	Crate										AUG-SEPT (test beam)		
	Power Supply												
	Controller												
	Fanout												July
	RF2TTC					NOW 3Weeks	NOW 2Months	NOW 2Months	NOW 6 Weeks	Mid JULY			Oct



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# DOCUMENTATION

- TTC upgrade proposal on EDMS

[https://edms.cern.ch/cedar/plsql/doc.info?cookie=5173380&document\\_id=628545&version=2&p\\_tab=TAB6](https://edms.cern.ch/cedar/plsql/doc.info?cookie=5173380&document_id=628545&version=2&p_tab=TAB6)

- TTC upgrade site

<http://ttc-upgrade.web.cern.ch/ttc-upgrade/Default.htm>

- RF2TTC Review on INDICO/Projects/TTC

<http://indico.cern.ch/categoryDisplay.py?categId=1099>