VMM2 SRS Hybrid

S. Martoiu, A. Rusu
IFIN-HH/CERN

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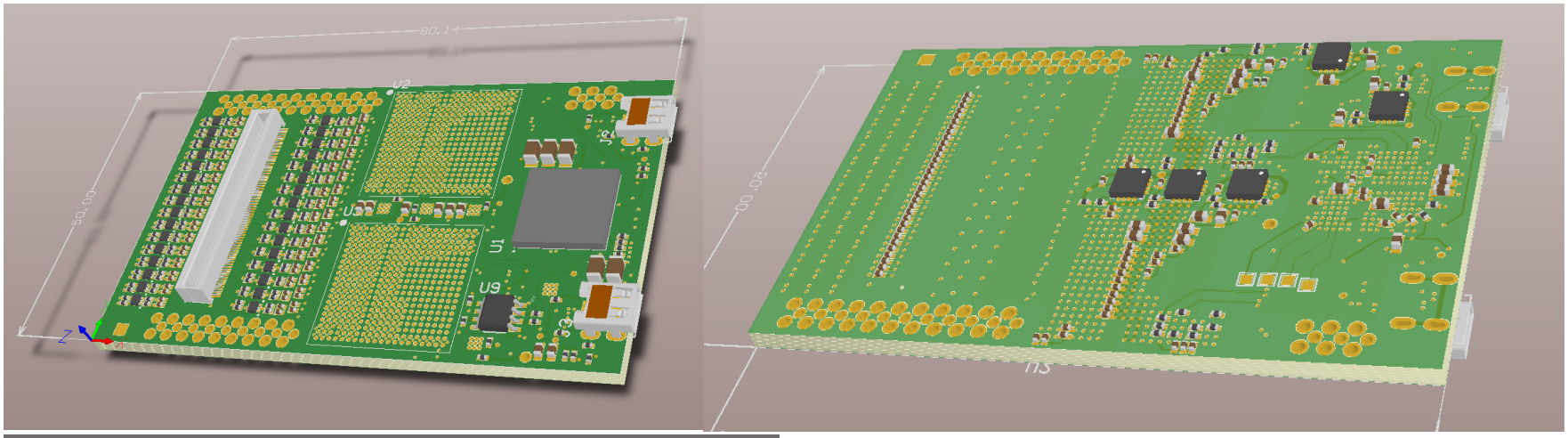

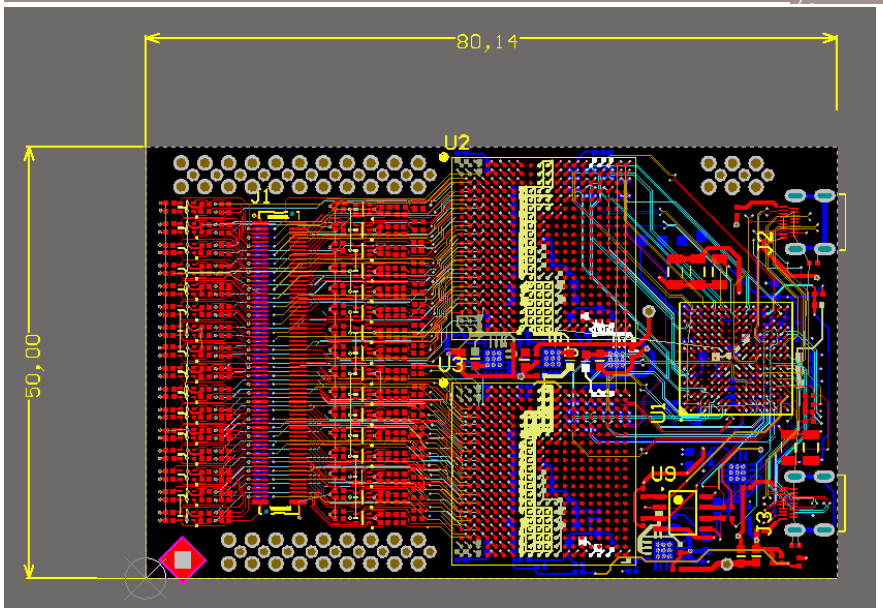

- PCB design by Alex Rusu
- Design being released for fabrication
- Dimensions: 80 x 50 mm

- VMM and FPGA on the “Panasonic” side.
- LDOs and a few caps on the other side

- Prototype completion < 2 weeks
- Higher quantity production depends on VMM2 availability in quantity.

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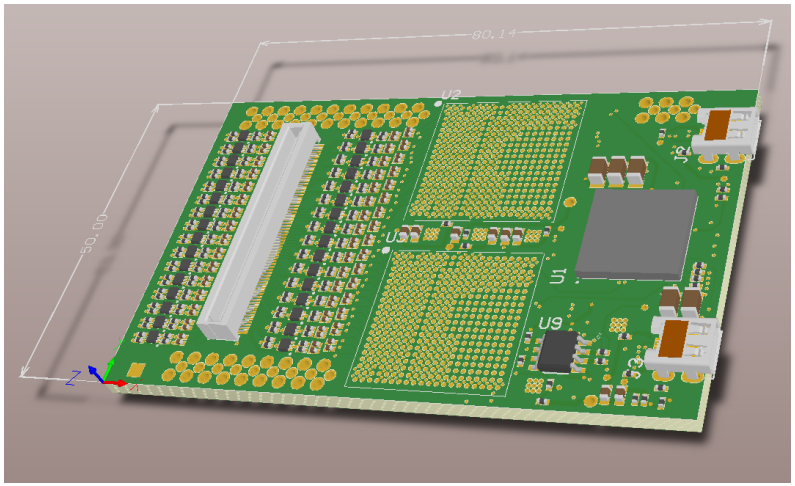
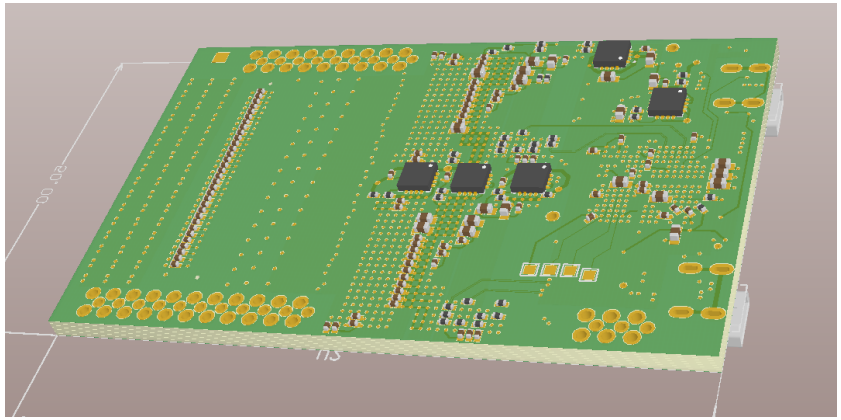
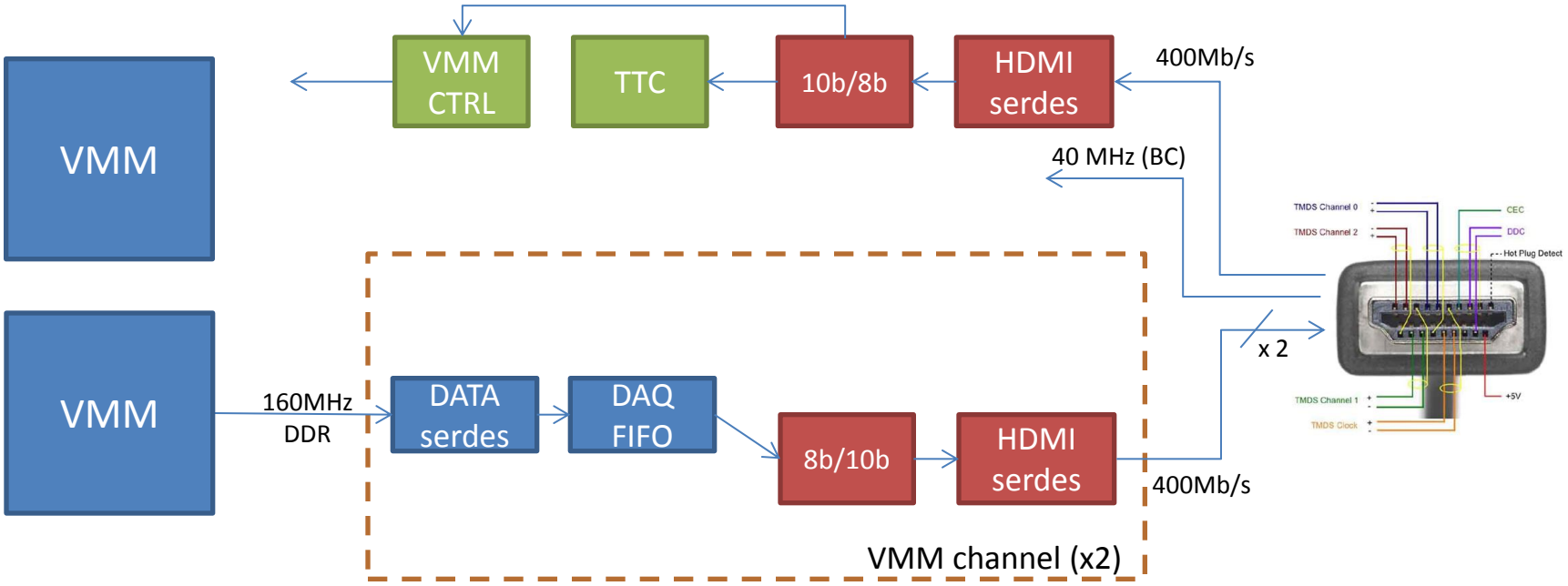




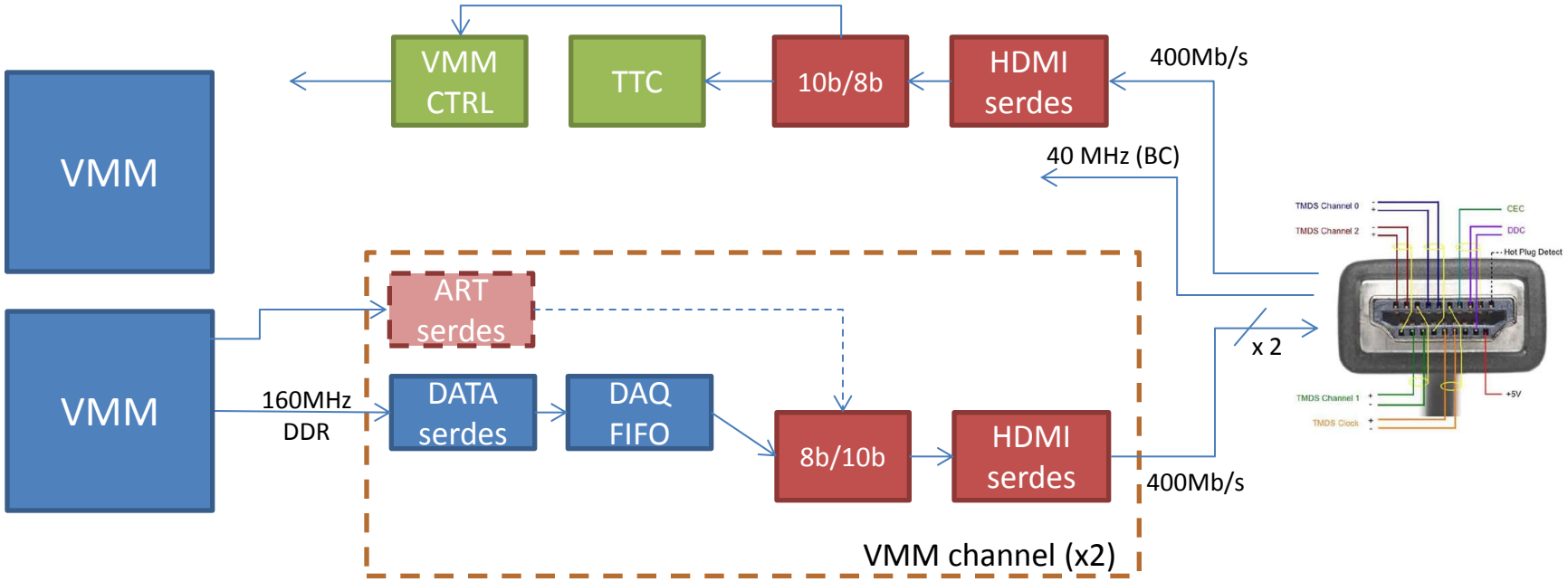
- Spartan6 LX9/16 FPGA for VMM control/data acquisition
- 1 x Micro HDMI for DAQ
  - Clk (40MHz)
  - TTC and configuration (400Mbps – 10b8b)
  - 2x data lines (400Mbps – 10b8b)
  - (opt.) ART info over data lines
- 1 x Micro HDMI for ART
  - Buffered ART signals
  - (opt.) clk, ttc
- Power in via HDMI (> 2.7 V)
- On-board LDOs
  - 4 x 1.2V (analog, a/d, digital, fpga)
  - 1x 2.5V (fpga)
  - ADP1755 (reported to be rad tolerant up to > 2KGy https://indico.cern.ch/event/310595/session/0/contribution/12/material/slides/0.pdf)

Evaluation Firmware



- TTC and Control channels use one HDMI high-speed line with 8b/10b encoding scheme.
- Direct data flow (no L1A selection) with 8b/10b encoding over 2 x HDMI lines (one for each VMM)

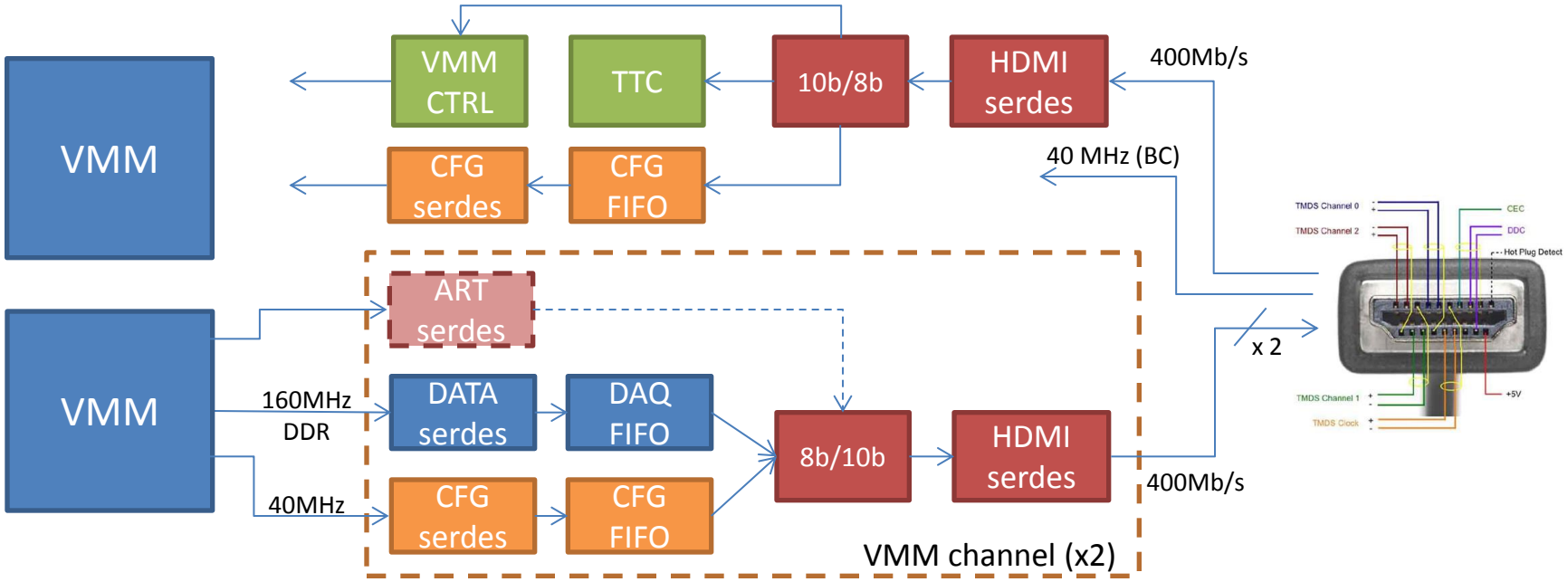
Evaluation Firmware



- (Optional) high-priority ART channel interleaved on the data line (*planned*)

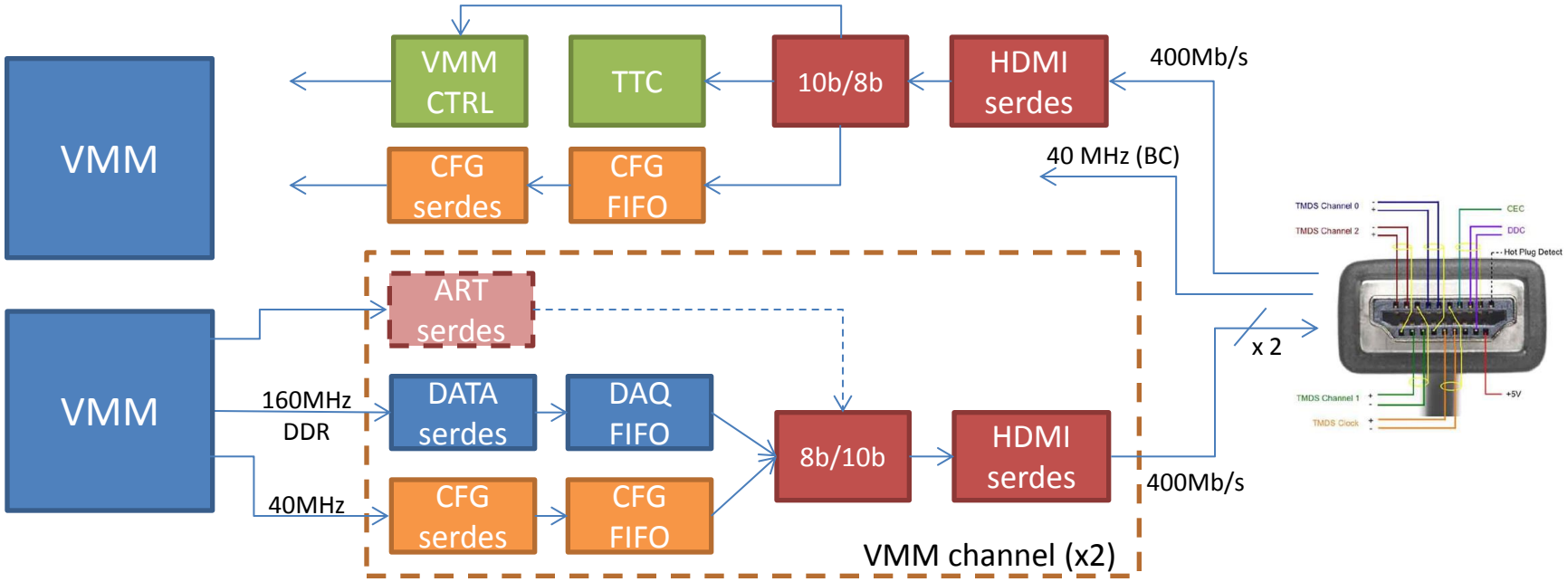
- Second HDMI port is used for a separate ART path (buffered ART signals).

Evaluation Firmware



- Control loop is shared with the TTC,Control and Data path on a low priority basis
- Redundant control and configuration via I2C
- Remote FPGA re-configuration (planned)

Evaluation Firmware



- Evaluation firmware fits in LX9 with enough margin.
- Planning to install LX16 anyway for future developments.

Summary

- PCB design completed, soon under fabrication in prototype run
- Fast assembly queued, prototype turnaround should be less than 2 weeks
- Minimal firmware is done, SRS application firmware under development.
- Higher volume production depends on VMM2 availability in qty.