Status of the MOPOS

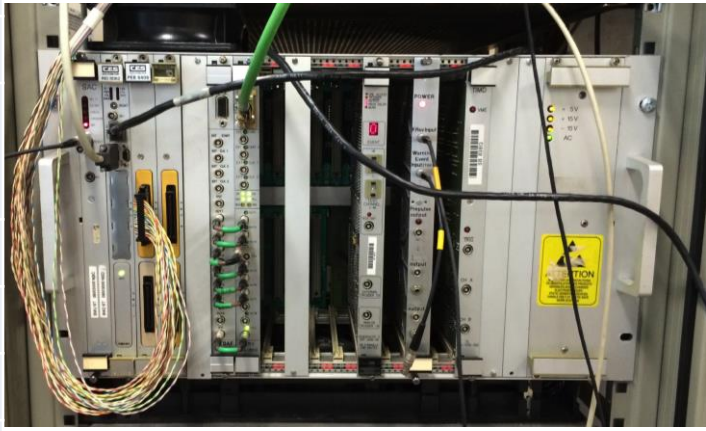
BI TB – 26th June 2014

Existing MOPOS

- MOPOS has been restarting during the last few weeks…no major faults
- Repair of 56 BPM Channels
  - List of faulty BPM identified by OP, including BPA and BPD
  - Replacing mainly analog module
- Replacement of BPA, BPD (resonant pick-up) with BPCE striplines

Existing MOPOS - Spares

Item	Installed	Spares	Comments
MOPOS VME Crate with special P2 Bus	6	1	
SAC	6	1,Std	
PowerPC RIO2 8060 version DA, HA or OA	6	4	may be more..
1Gb RAM extension	6	1	
PCI extension PEB 6406	6	4	'porte avion' 1
PCI extension PEB 6407	6	4	'porte avion' 2
PMC Acquisition card (MACI) mezzanine	24	19	
CTRV	6	Std	
CTDAF	6	3	
SEQ III	6	5	Recuperated from ttpos
TIMD	6	2	
Power Supply	6	3	



Many (>20) spares of analog modules: (pre-amp, filter/calibration, Homodyne receiver, SHAD (digitizer) + some modules to be repaired

Existing MOPOS

- Situation of Spares
  - Having as many ‘hot spare’ as possible (>1 full system)
    - Need to test all spares now
  - VME system and related components are more critical
    - but, we had very little to change over the last 4 years
  - Analog modules are not an issue

- UPS in Ba’s
  - By design VME crate on UPS
    - Some system has not been maintained fully operational, i.e. in BA3
  - Action to be done to run both analog and digital electronic on UPS electrical network

MOPOS Renovation

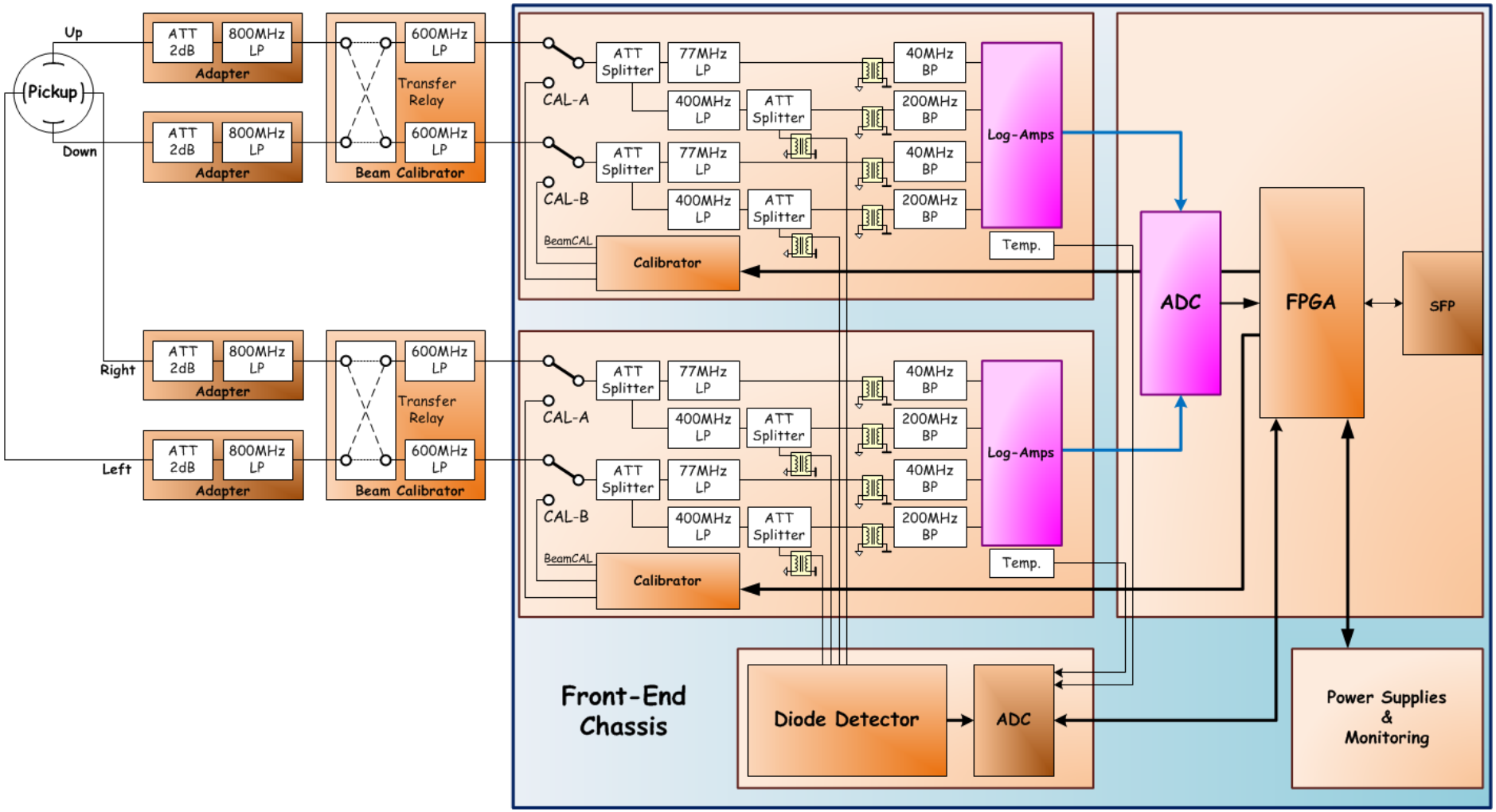
- Hardware Status
- Installation Status
- Short and long-term plans

SPS Beam Position Monitors

Monitor Type	Physical Beam Aperture (mm)	Quantity	Mechanical Section	Comments
BPH	44V x 154H	103	rectangular	Electrostatic shoe-box
BPV	83 x 83	94	square	Electrostatic shoe-box
BPCN	76	7	circular	Strip-line directional couplers
BPCE	206	12	circular	

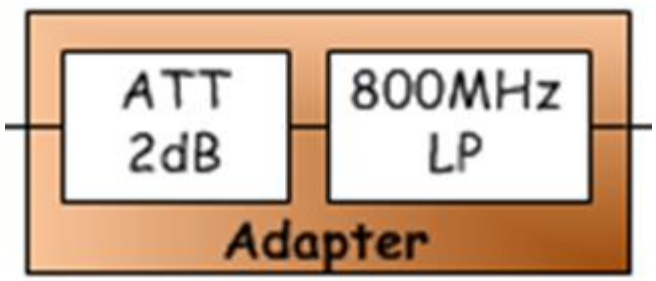
Total = 216 BPMs: 6 x 36 slots

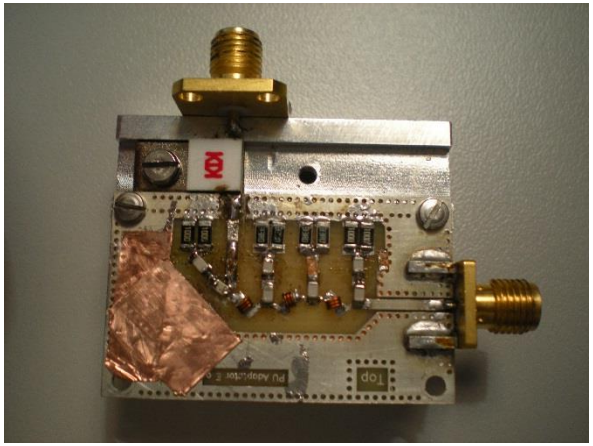
MOPOS Front-End Layout

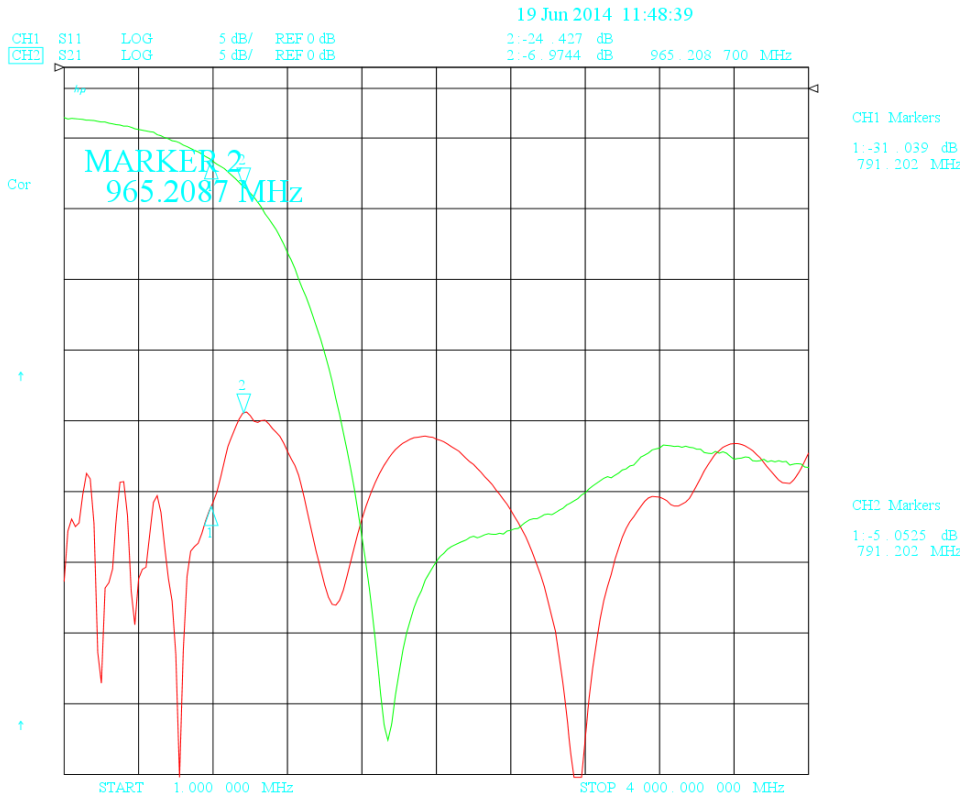


MOPOS Hardware Status

- PICK-UP ADAPTER - DEVELOPMENT:

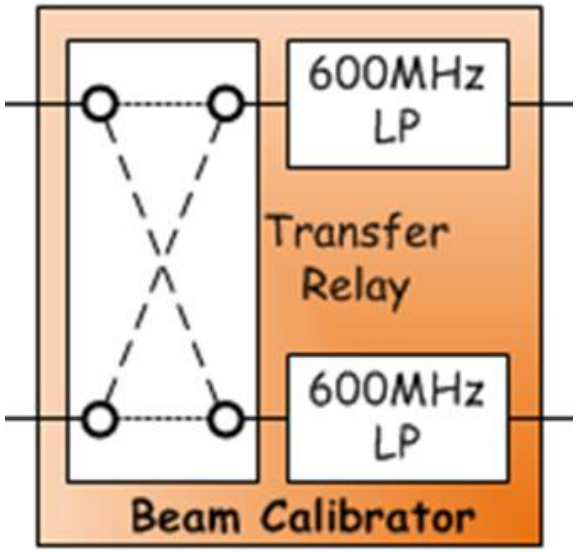


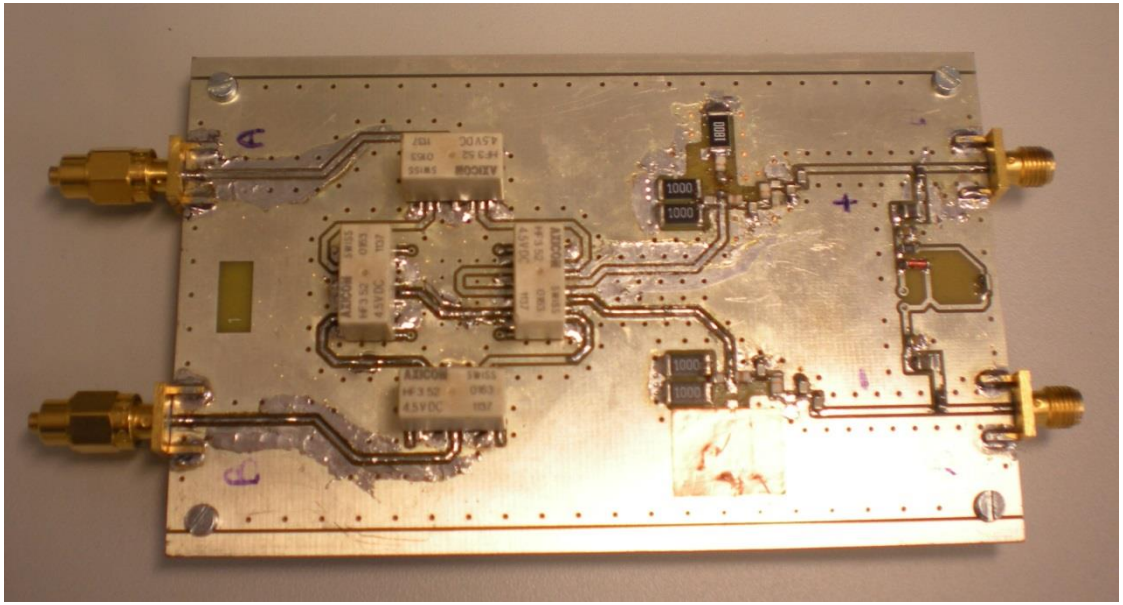




MOPOS Hardware Status

- BEAM CALIBRATION: “Transfer-Relay” development



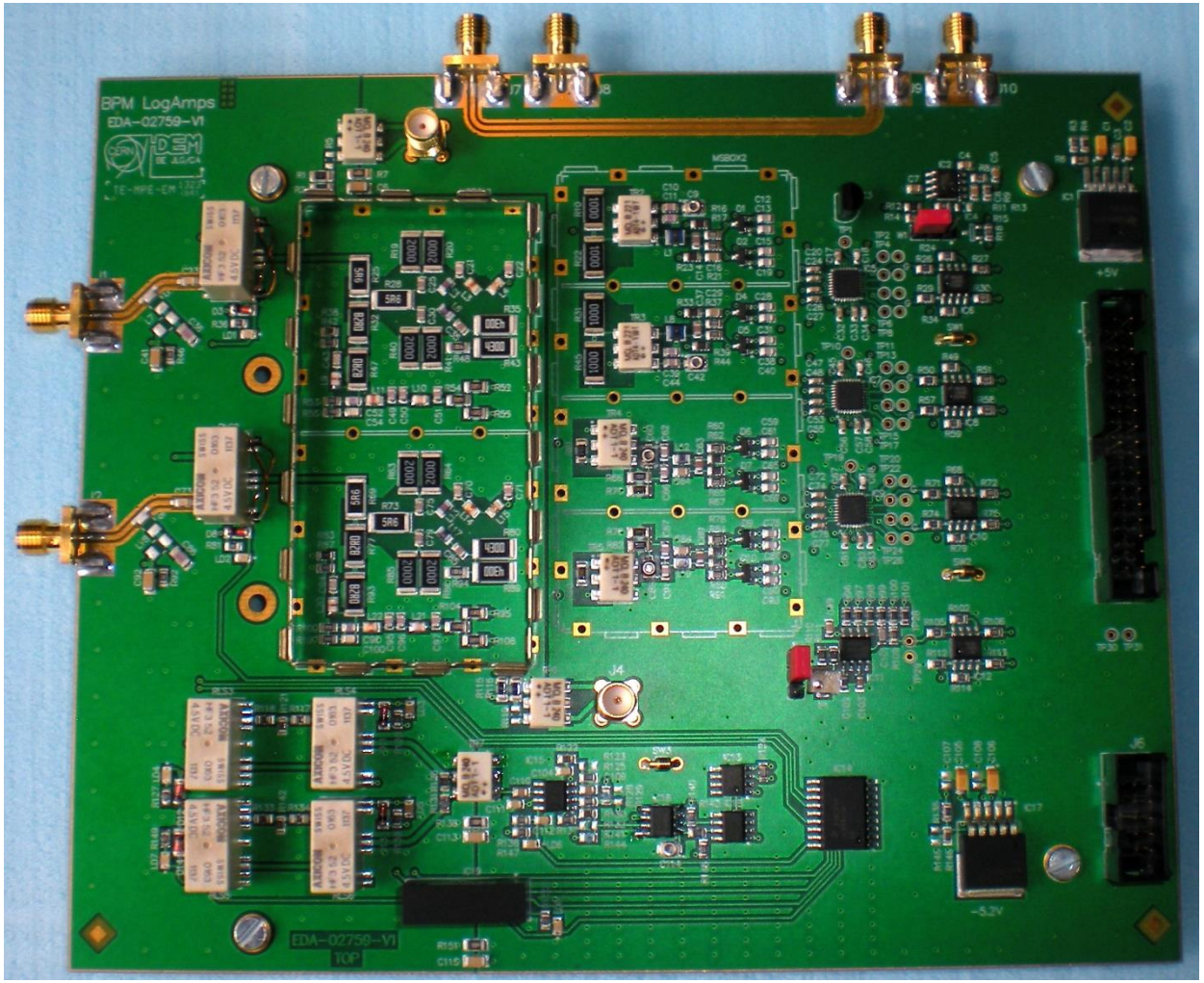


MOPOS Hardware Status

- LOGAMPS

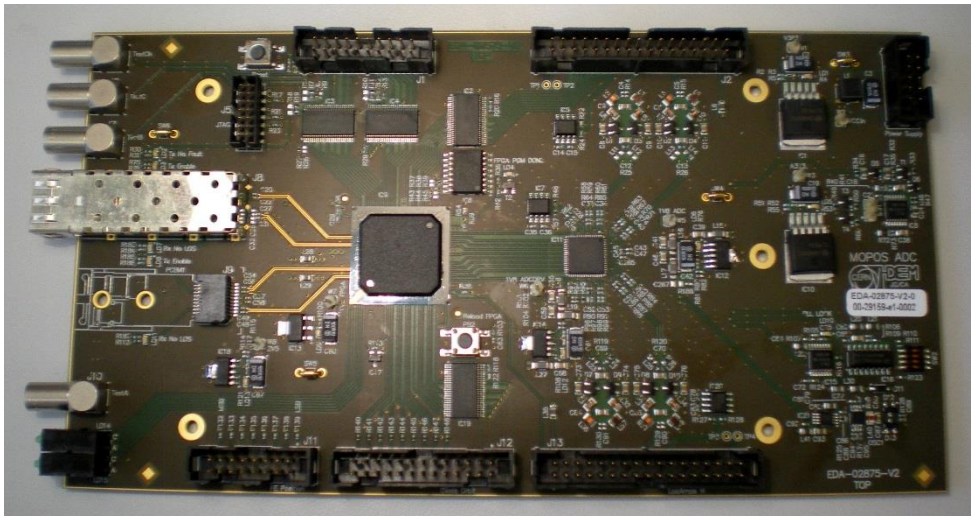
  Need minor corrections

  2nd prototype under test right now



MOPOS Hardware Status

- ADC, FPGA & OPTICAL TRANSMITTERS



  - Octal-14bit-ADC: AD9252
  - Xilinx Spartan-6 FPGA (VFC-V2 Compatible)
  - Versatile Link (rad-hard) & Commercial SFP module
  - Interface for Diode Detector Acquisition (Marek's development)

MOPOS Installation Status

- Mini-Racks
  - The SPS tunnel has been equipped with 6U & 16U Mini-Racks.
- Cables
  - Installation completed in LSS1 & LSS6 (EN/EL)
  - Next (LS2): LSS2…LSS5
  - *Local cabling not done yet*
- Fiber Installation (LS1)
  - Installed: Sextants 1, 5 & 6 and Shaft 4
  - Still to be done: Shaft 3

MOPOS Tests in SPS-Sextant 6

- Installation of prototype modules (2014/2015)
  - Test and validate the performance of the FE electronic LogAmps, Beam-Calibrator
  - Pick-up adapters foreseen to run Old & New MOPOS in parallel
  - Front-end Electronics modules will be installed both in the tunnel and in surface buildings in order to test their susceptibility to radiation
- Installation of a VME crate in BA6
  - VFC-V2 modules will be used for the New MOPOS functional tests

MOPOS Installation Plans

- Current Plan
  - Development of a radiation-hard digital board (2014..)
    - Test in SPS tunnel and at CHARM (PS)
  - Complete the fibre installation (BA2…BA5) during LS2
  - Commissioning of new system post LS2

- Option : if major issue with existing MOPOS (2016/2017)
  - Use the BPM-cables to transfer the pick-up signals to surface buildings (BA1…6)
  - Based on new VFC-HPC

VFC - HPC

SRAM vs DDR3

External memory requirement for the MOPOS: can DDR3 be used?

- The Capture mode is the acquisition mode that uses the external memory in the MOPOS
- There are 2 “capture modes”:
  - The ***debug mode*** saves all the data but only for one plane
  - The ***operational mode*** stores the data only for the selected sensitivity but for both planes
- Both modes write 4 32bit words each 100ns into the memory leading to a required transfer rate of **1.24Gb/s that is compatible with the DDR3 (1.33Gb/s) but without much margin**
- Both modes have data redundancy that could be eliminated and would reduce the required bandwidth to ≈ 800Mb/s

Plans for VFC-HPC

- Currently testing the VFC with SRAMs
  - Modify the bugs we found
  - Produce an operational version with SRAM at least a gerber file (little amount of work/money involved)
- New VFC with DDR3
  - Outsourcing design and layout
  - Testing a first prototype early next year

Specification

SPS Beam Type	Bunch spacing	Bunch number	Bunch charge [10^{10}]	Bunch length [4σ: ns]
FT / CNGS	5 ns	400-4000	0.1-2	1-4
LHC25NS	24.96 ns	N_{batch} × 72	1-35	1-4
LHC50NS	49.92 ns	N_{batch} × 36	1-35	1-4
LHC75NS	74.88 ns	N_{batch} × 24	1-35	1-4
LHC single bunch	524.4-2022.6 ns	1-16	0.2-35	1-4
LHC ion / Pb82+	100 ns	N_{batch} × 4	0.05-2	1-4

N_{batch}: Protons[1-4]; Ions[1-13] Bunch charge dynamic range: 57dB

- Orbit acquisition: averaged over 40 turns [40x23µs=920 ms] (@1kHz up to 100s) 100k turns total
- Trajectory acquisition: 50 first turns (automatic) & 10k turns total (on request)
- Resolution over ±15mm aperture, for large intensity beams (>2.10^{10} p):
  - Orbit mode: 0.1 mm ↔ BPH [Na=77mm]: 0.1% BPV [Na=41.5mm]: 0.2%
  - Trajectory mode: 0.4 mm ↔ BPH: 0.5% BPV: 1%
- Resolution over ±15mm aperture, for single bunches (LHC pilot [2.10^{9} p]):
  - Orbit mode: 0.4 mm ↔ BPH: 0.5% BPV: 1%
  - Trajectory mode: 1 mm ↔ BPH: 1.3% BPV: 2.4%
- **Required accuracy (without alignment): 0.5 mm** ↔ BPH: **0.6%** BPV: 1.2%