Proposal of new electronics integrated on the flanges for LAr TPC

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Outline

- *ICARUS readout architecture*
- *Limitations of the existing system*
- *Proposal of a new readout design*
- *Cold front-end (jFet matrix)*
- *Conclusions*

T600 electronic racks on top of detector at LNGS

- ICARUS T600 read-out electronics, designed to provide continuous digitization and waveform recording of signals from each wire of the TPC, has proven to perform quite satisfactorily in the run on CNGS beam at LNGS since May 2010.
- It consists of an analogue front-end amplifier followed by a multiplexed parallel AD converter (10 bit) and by a digital VME module performing local storage, hit finding and data compression.
- T600: ~54000 channels. 96 racks host 1720 analog + 1720 digital boards.

Critical considerations

- It is important to remember that DAQ architecture for T600 was conceived in 1997 and front-end dual channel BiCMOS circuits were designed in 1998. The full system was designed and built from 1999 to 2000 and operated first time in 2001.

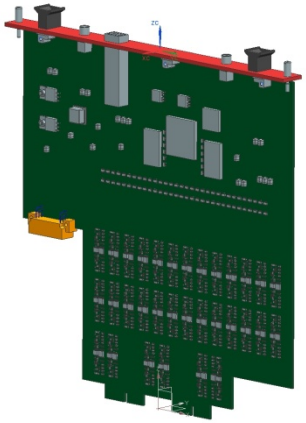
- In this scenario it's very important to make a critical analysis at **system level** to spot areas where the necessary changes could led to a more efficient structure.

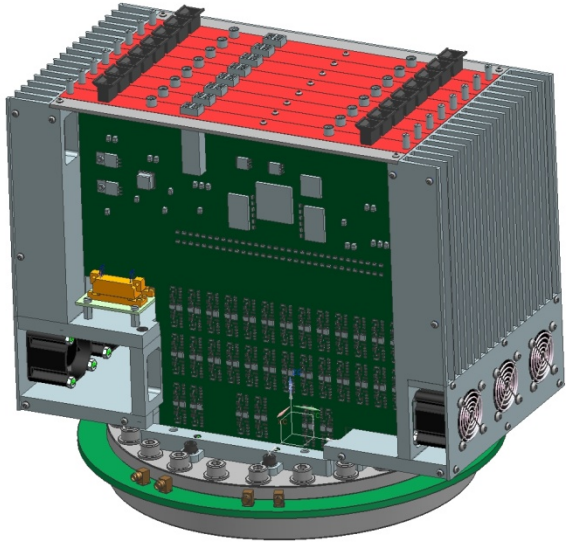
- Adopting a top down approach one **evident limitation** of T600 DAQ is due to the choice of the VME standard (8-10 MB/s), perfectly legitimate at that time.

The flange of T600 is an opportunity

- For T600 a very reliable and cost effective flange has been developed.
- Presently it allows for the connections of 18 twisted pair flat cables, each conveying 32 signals from wire chamber to external electronics. (576 ch's per flange).
- **It is conceivable with a compact design to host the full electronics on the flanges,** using the external side of the flange as a sort of backplane that support both analogue and digital electronics.
- It requires a minor change of flange design. The overall cost will be drastically reduced.

Electronics on the flange

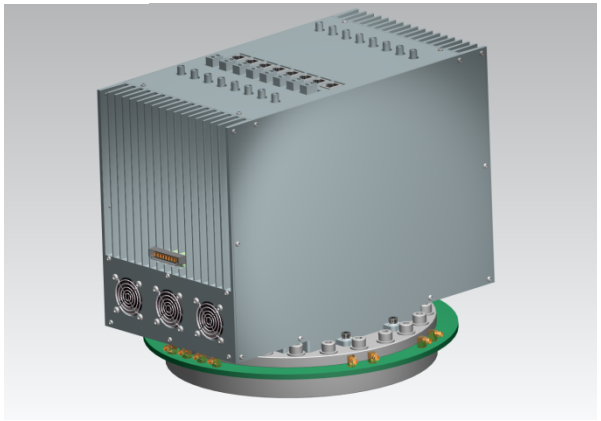




Optical connectors
Lemo connectors
Ethernet connector

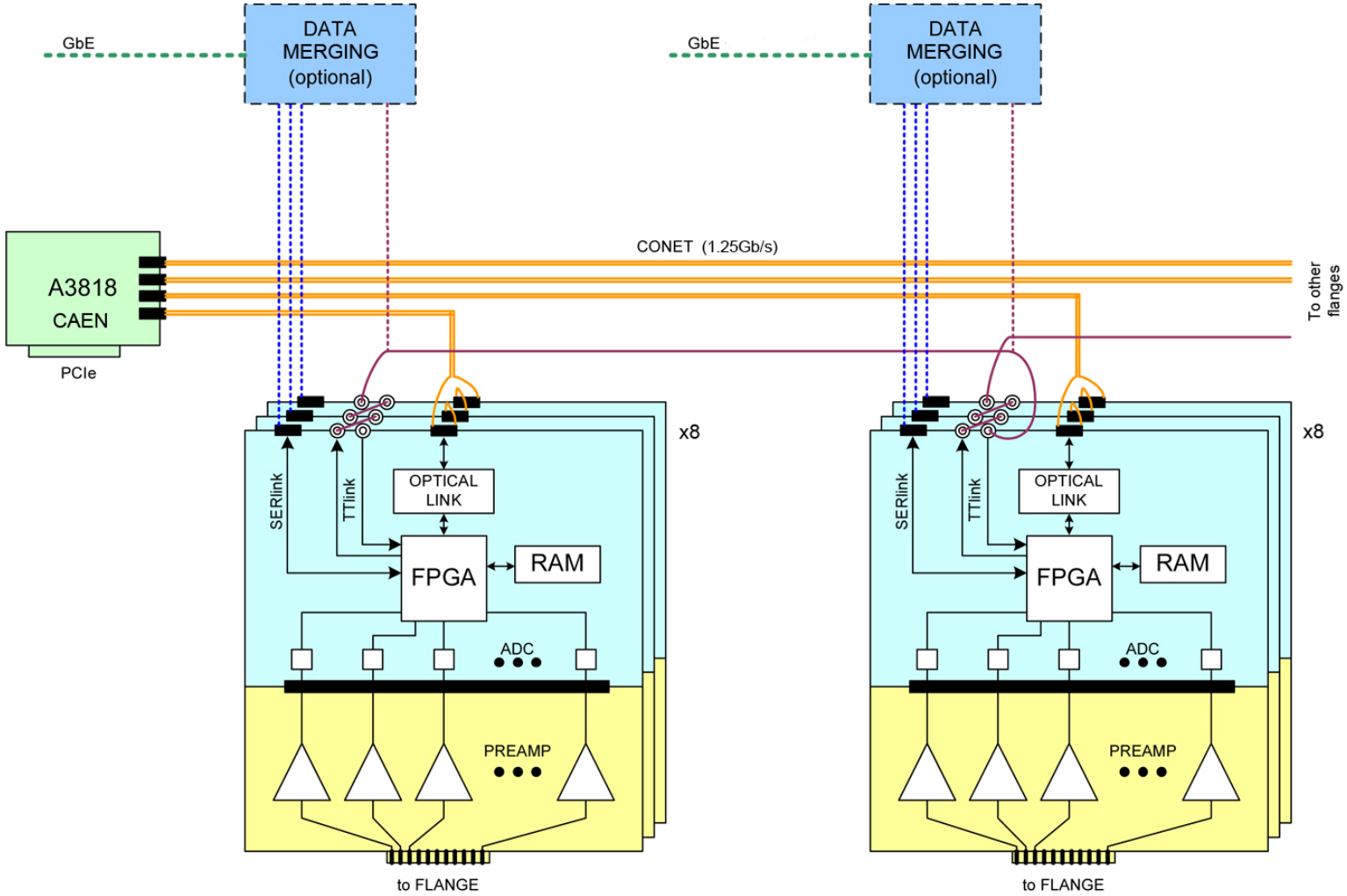
Backplane integrated on the flange

Power distribution on the auxiliary connectors on side bus

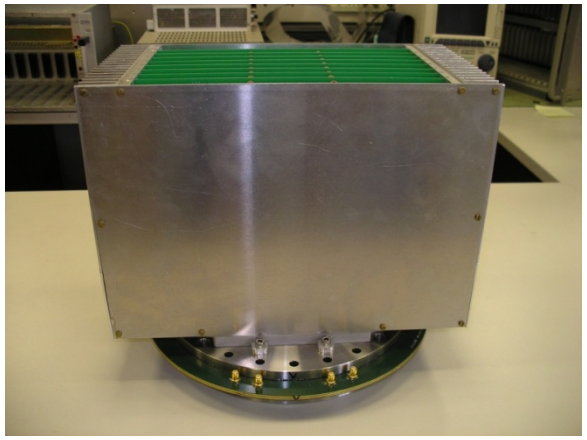
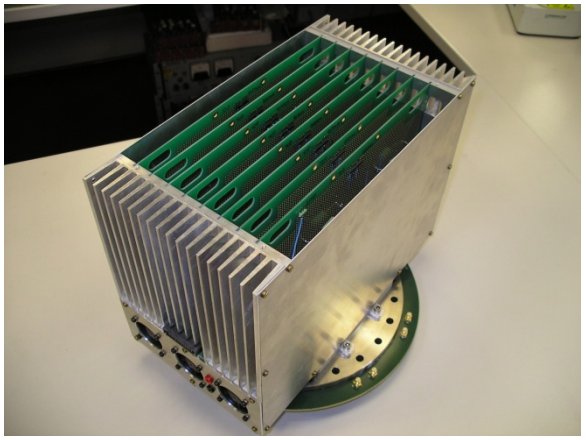
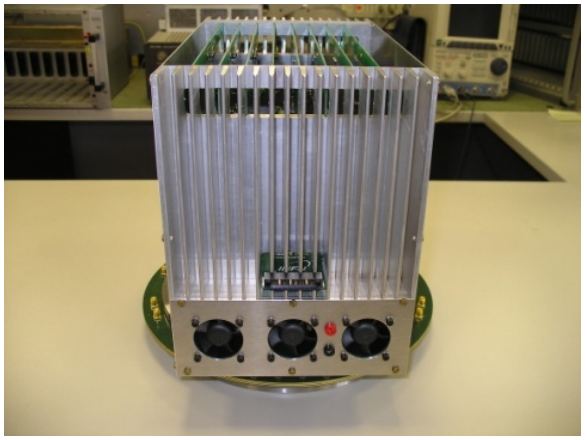
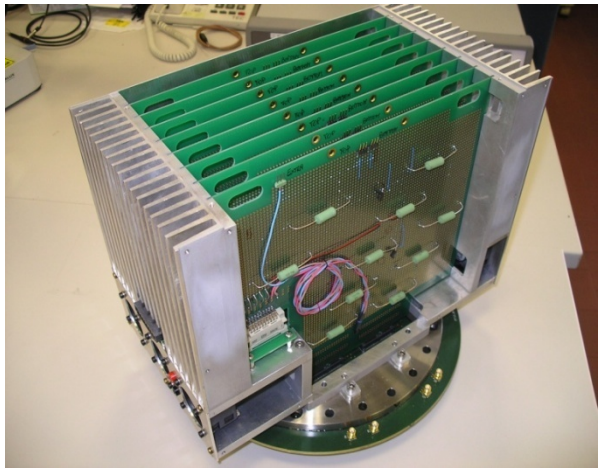
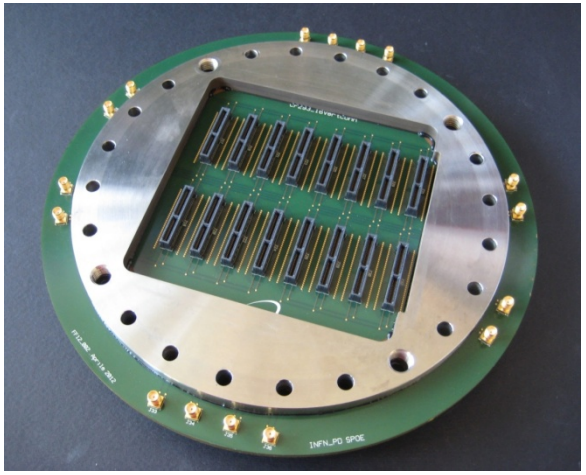
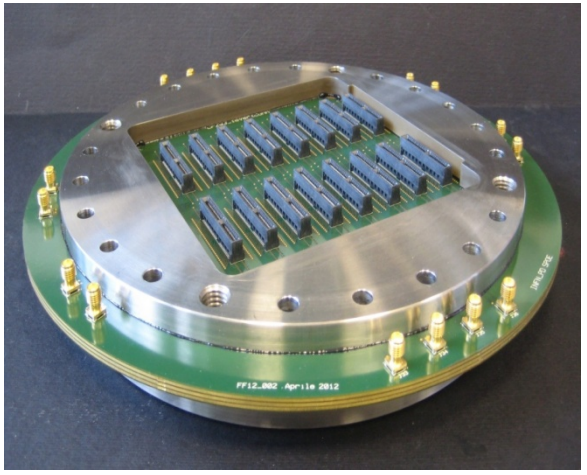


Proposed architecture

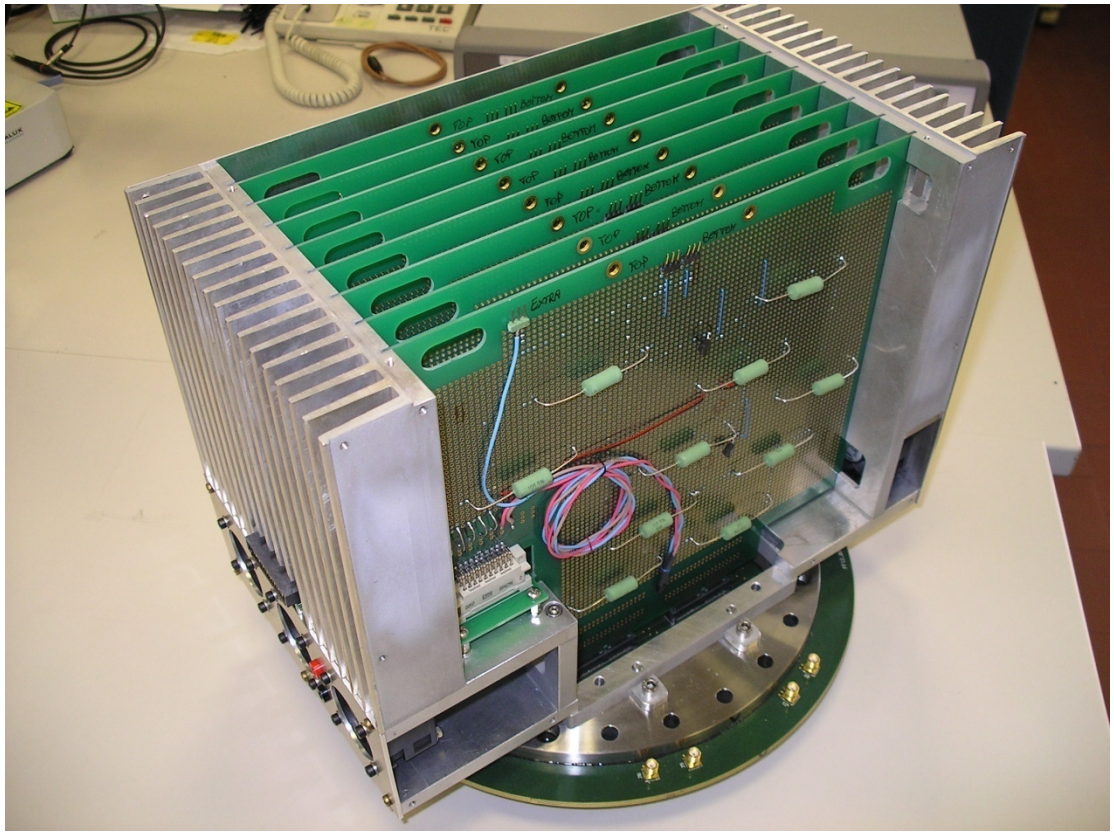
Off the shelf solution for easy testing

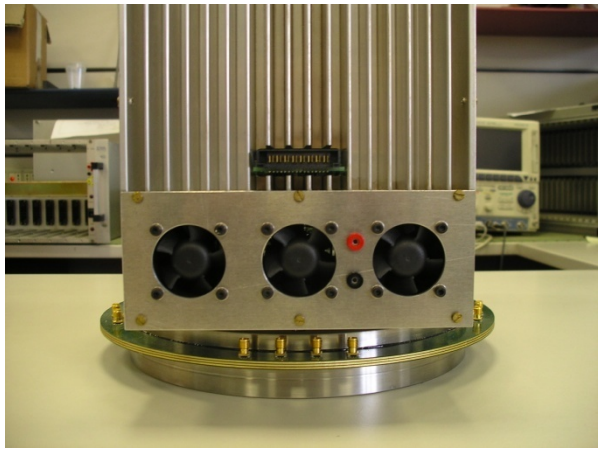


Prototype of flange under test

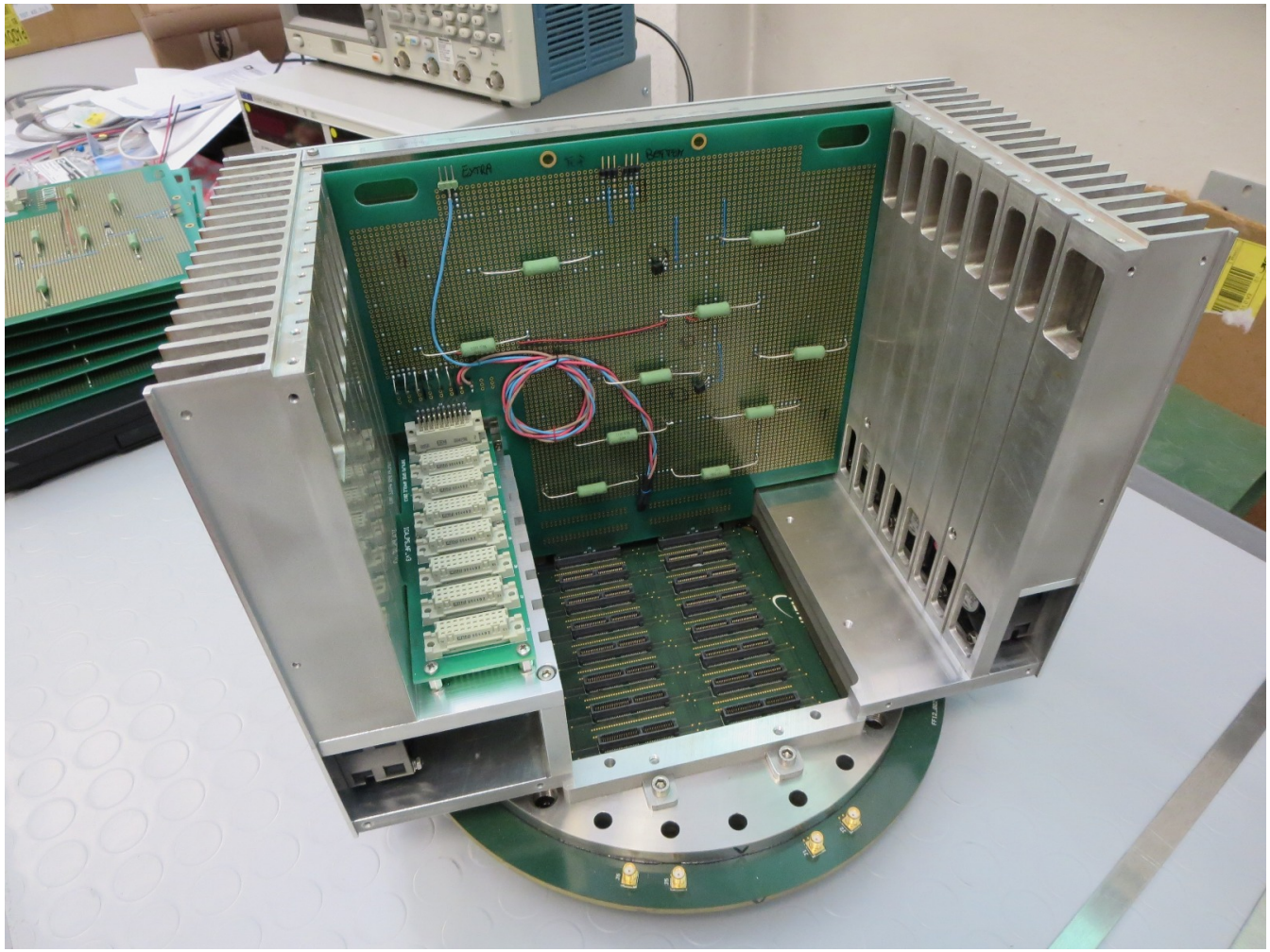







Measurement of heat dissipation





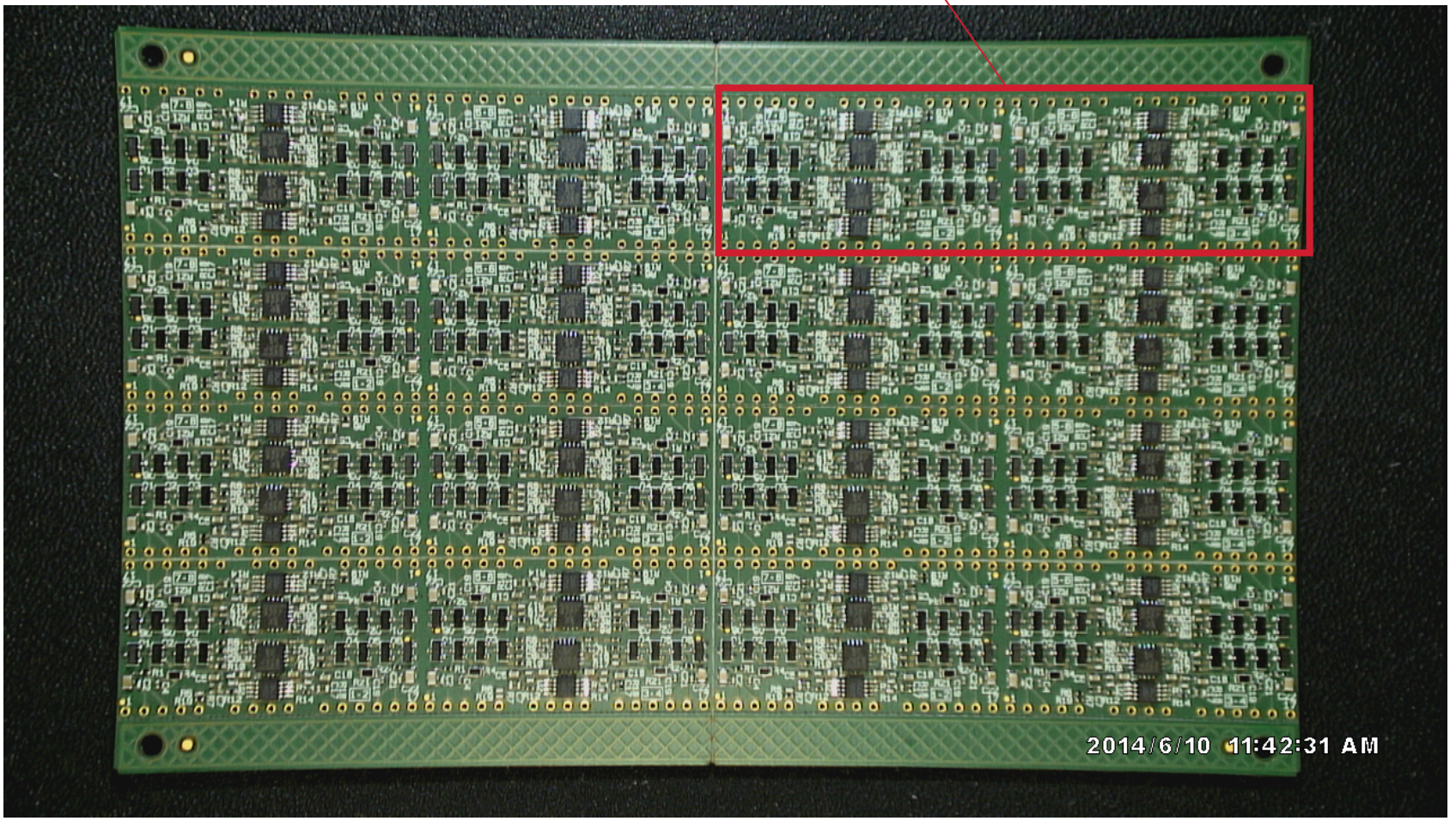
- Total of 200W distributed on eight boards (512 chs)
- The temperature inside the crate increases less than 20 degrees with respect to the ambient



Detail of the local bus for boards interconnection/control and powering
Connections and protocol defined in cooperation with CAEN

Layout for 8-channels submodules

Every FE of 8 channels is about 90x23mm



Final considerations on DAQ

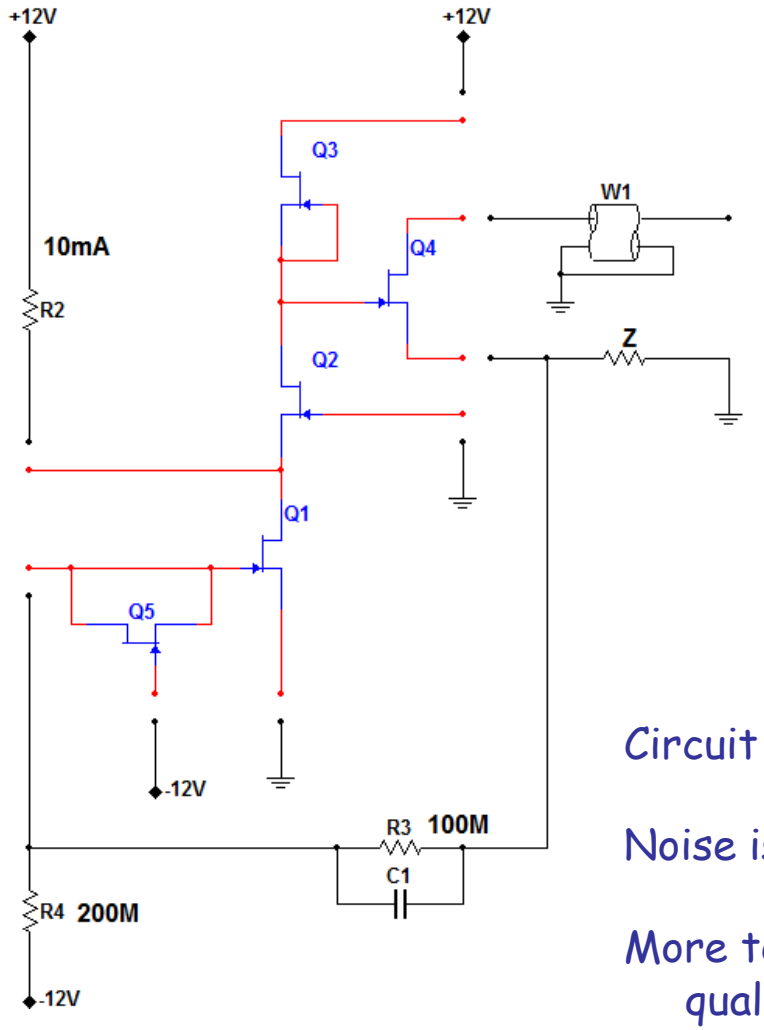
- The ICARUS DAQ basic architecture is well suited even for larger size LAr-TPC.

- Main upgrades concern:

  - More compact version of the front-end amplifier;
  - Adoption of high frequency serial ADC;
  - Adoption of a modern serial bus architecture;
  - Optical links for Gb/s transmission rate;
  - The proposed warm electronics (4 full boards) ready for test end of Sept. 2014

  Housing and integration of electronics onto flanges or cold electronics? Or a mix: cold front-end and warm digital processing?

jFet Matrix for cold front-end



$$Q1: g_m \geq 40ms @ I_D = 10mA (eg: IF4500)$$
$$Q2: V_{GS} \cong -1.7V @ I_D = 1mA, g_m \geq 20ms$$
$$Q3: I_{DSS} \cong 1mA$$
$$Q4, Q5: GeneralPurposeAmplifier$$

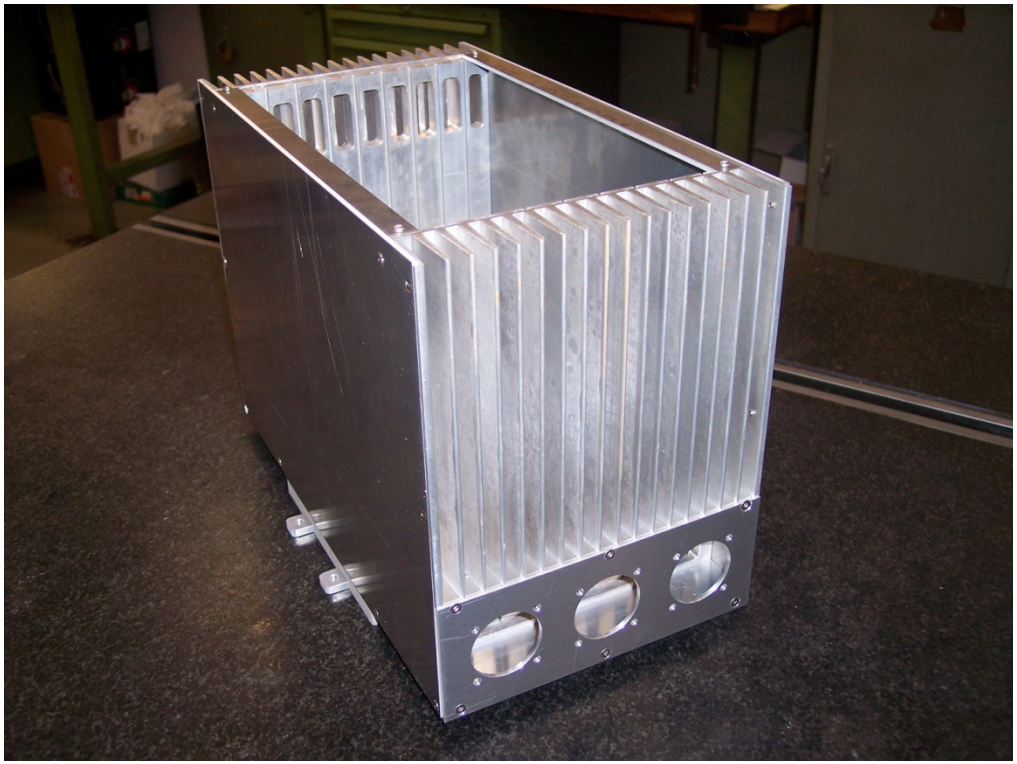
Circuit already tested with discrete jFets with success:

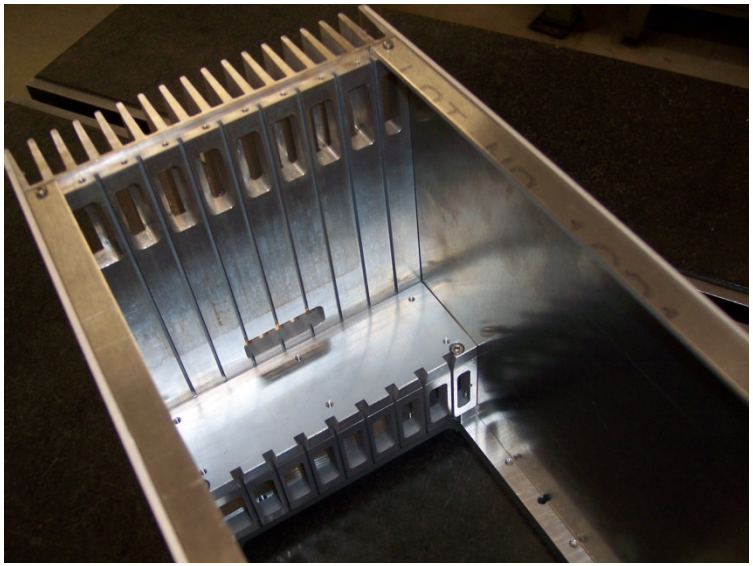
Noise is 1300 e ENC with Cd=100pF @ LN temperature

More tests to be performed for passive components qualification and noise improvement

Backup

Prototype of flange under test

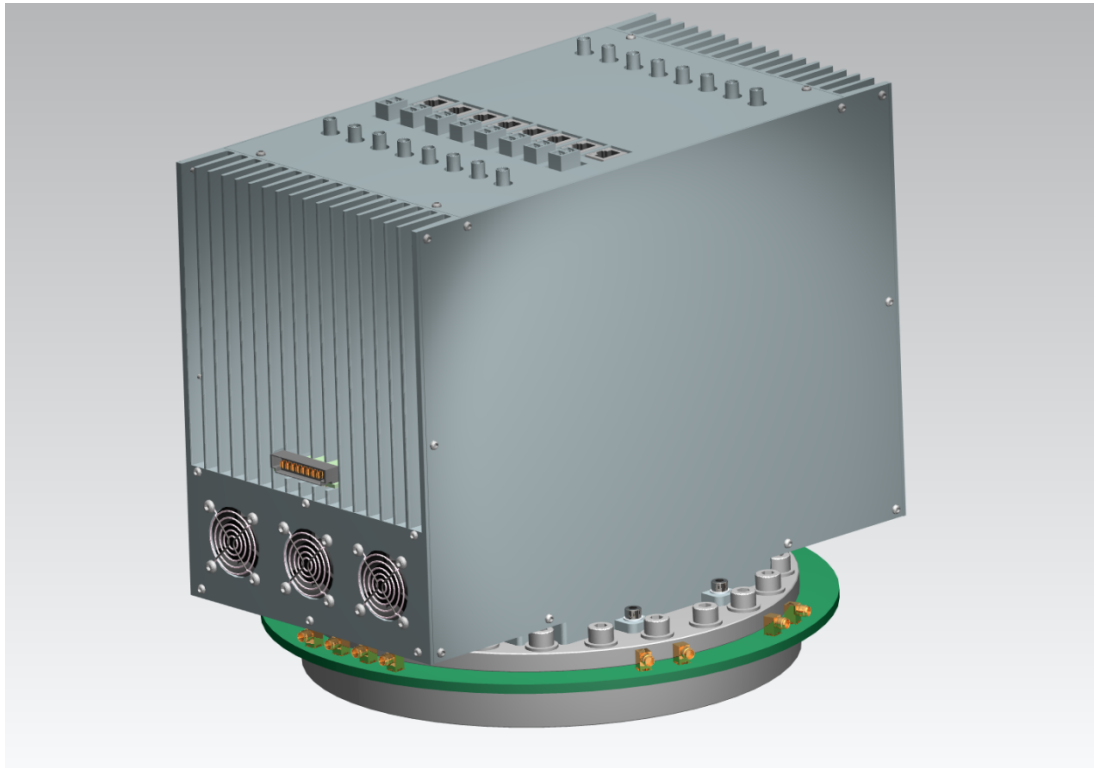




New readout system

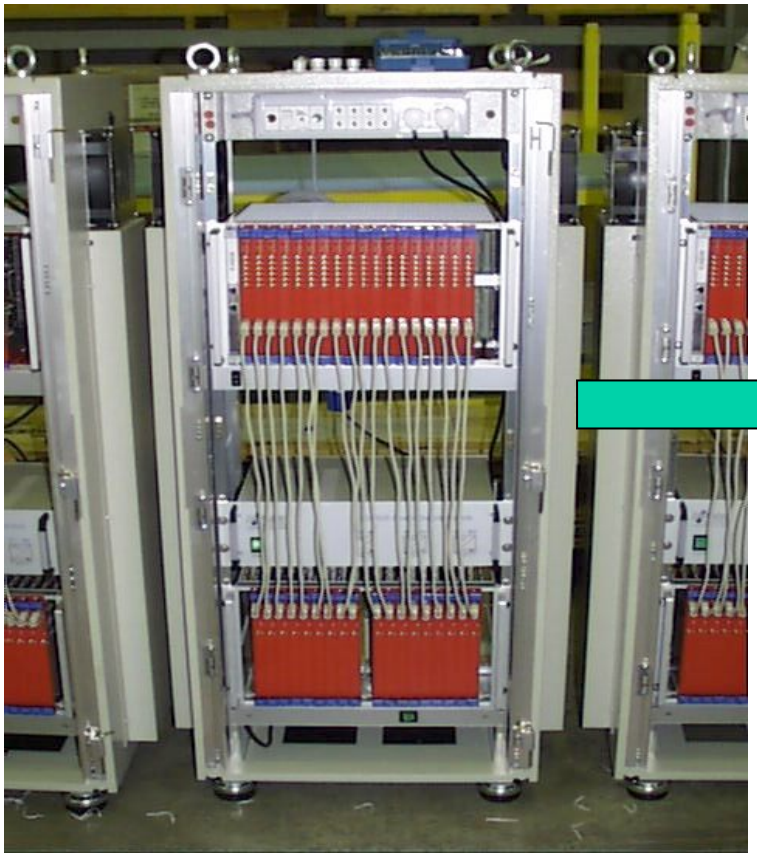
- Electronics can be hosted in a compact crate(~10 liter volume). One feed-through flange forms a sort of **backplane** for 8 electronics boards(512 channels)

- External cables for signals from wires will be eliminated



General comparison

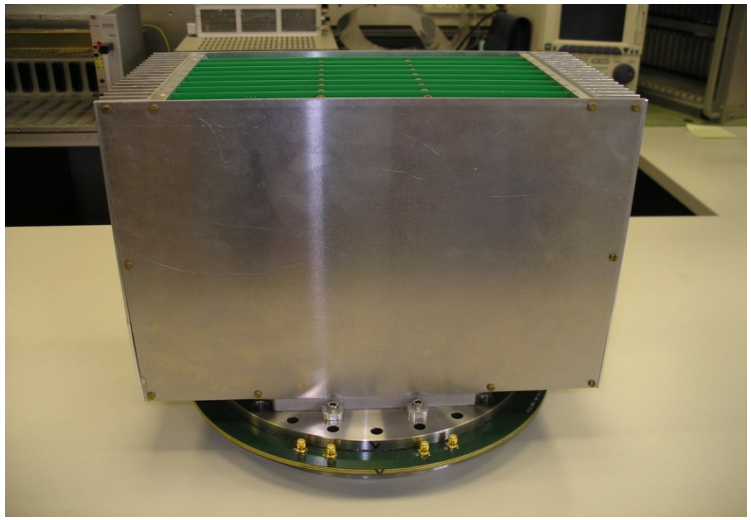
Present T600 electronics



~595 liters, 576 chs (modulo 32)

Bandwidth: 10MB/s

New high density solution
Integrated onto the flange



~10 liters, 512 chs (modulo 64)

Bandwidth: >1GB/s