Current Status of the Pixel Phase I Upgrade in CMS:

Barrel module production

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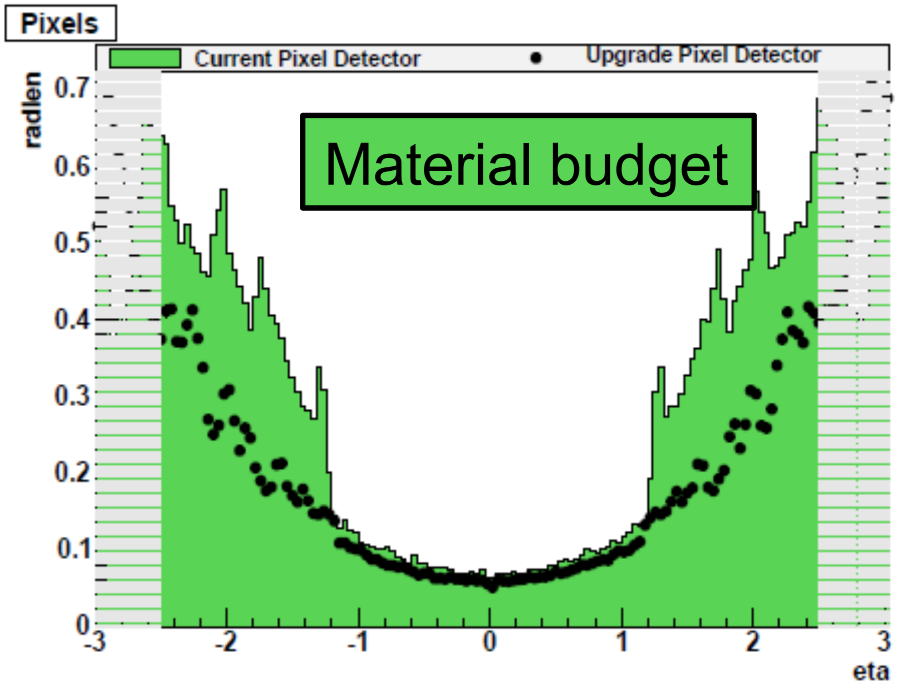
The CMS Phase I Upgrade

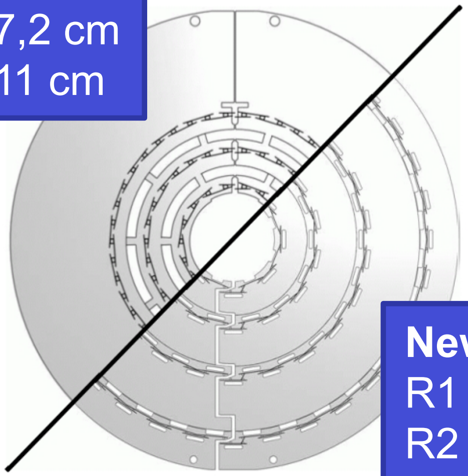
What's the plan for Phase I ?

- Upgrade of the CMS pixel detector in extended year end technical stop 2016/17
- One additional Layer of detector modules
  - 4 layers in the barrel region
  - 3 layers in the forward region
- Reduction of material budget
  - Electronics moved forward of active detector area
  - CO_2 cooling
  - Carbon structure support
- New beam pipe (installed during LS1) will make it possible to bring the first layer as close as 3 cm to the interaction point
  - A simultaneous increase of instantaneous luminosity by the LHC will lead to a steep rise in the particle flux passing through each layer of the pixel detector



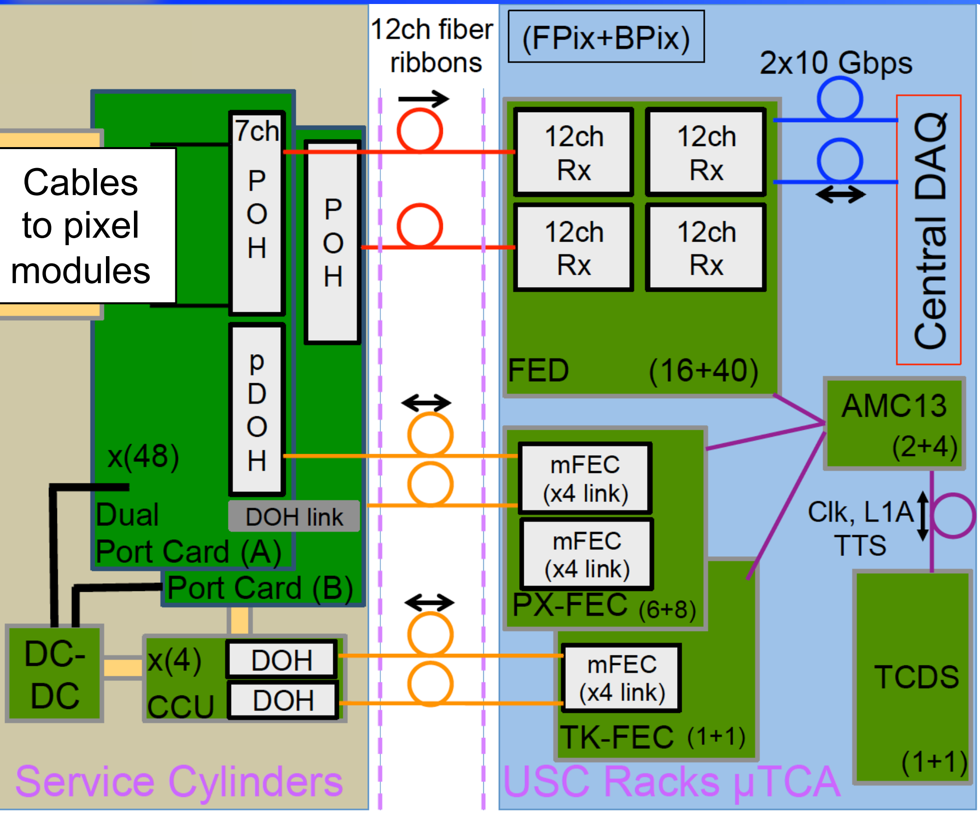
Material budget

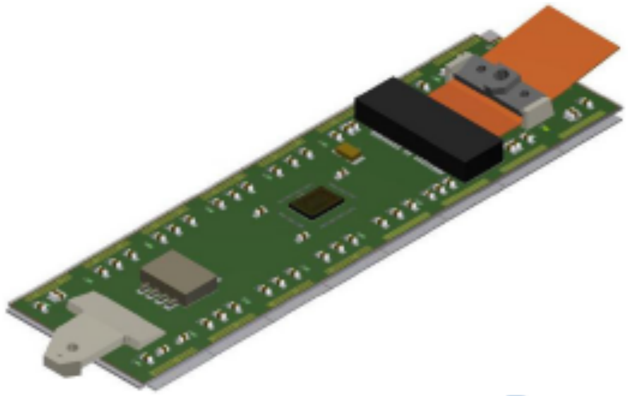
Old Radi
R1 = 4,3 cm
R2 = 7,2 cm
R3 = 11 cm

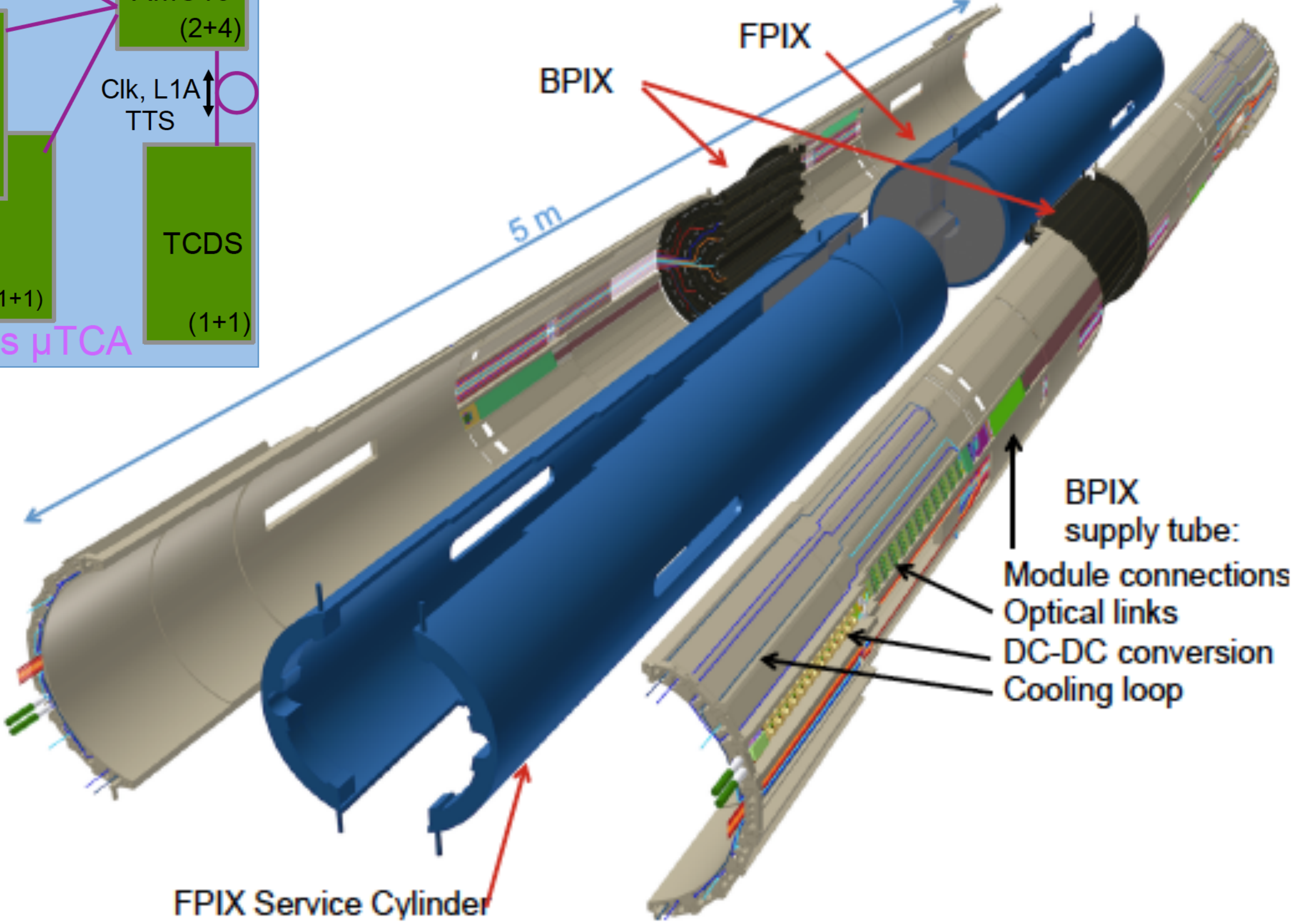


New Radi
R1 = 3,0 cm
R2 = 6,8 cm
R3 = 10,9 cm
R4 = 16 cm

Pixel Phase I Project







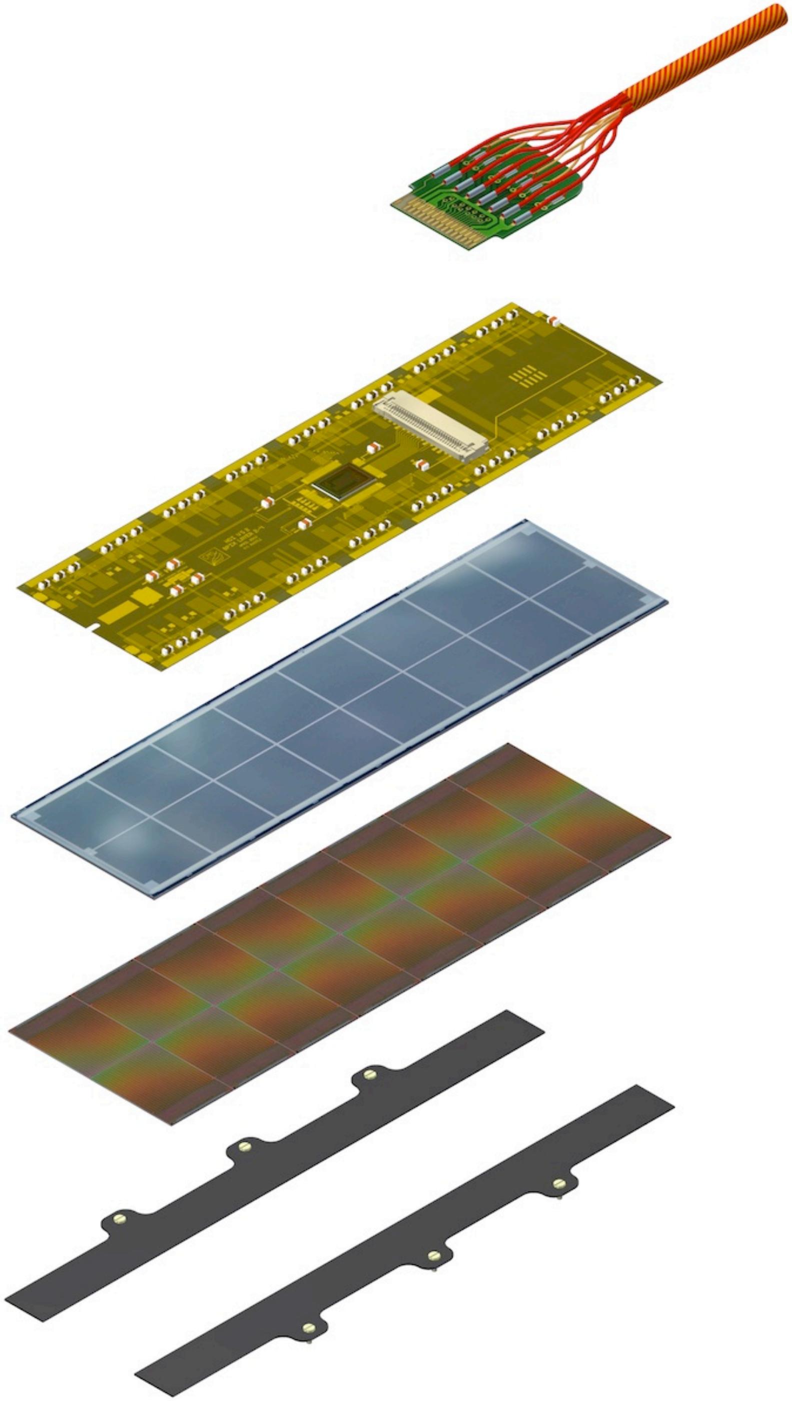
Barrel module production

Anatomy of a module

- Twisted pair cable
- HDI (High Density Interconnect)
- Bare module
  - Silicon Sensor
  - ROCs (Readout Chips)
- Base strips

Layer/Disk	Number of modules
L1	96
L2	224
L3	352
L4	512
D1-3 inner	264
D1-3 outer	408

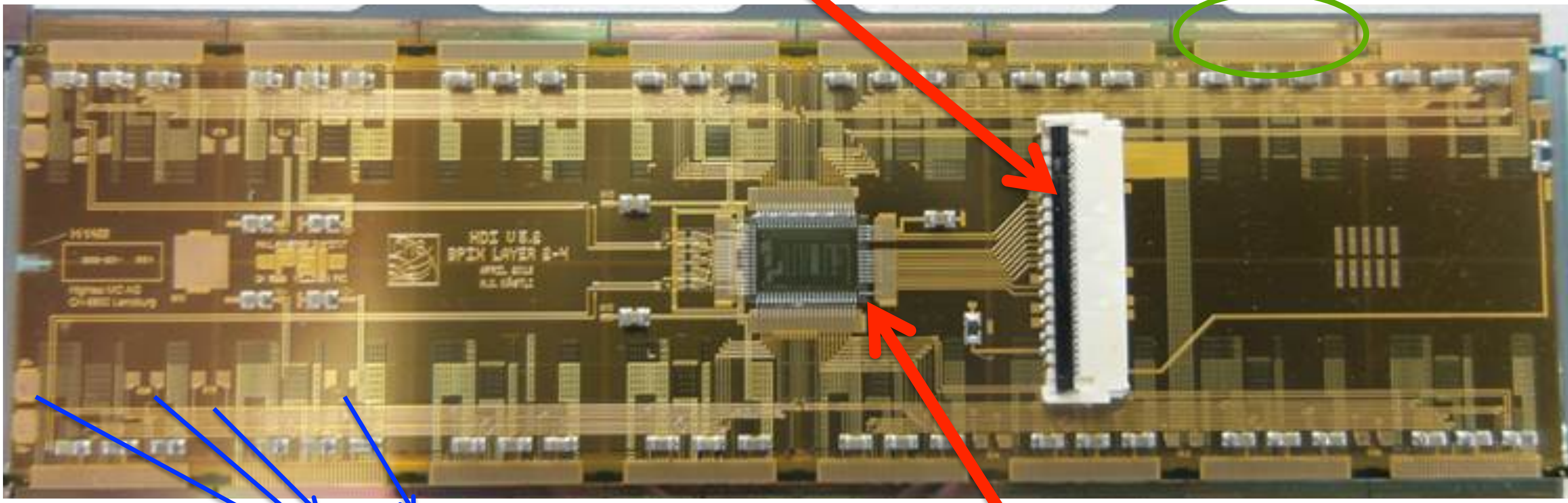
- 16 ROCs of 52 x 80 pixels
  - 150 µm x 100 µm pitch



HDI

- Interconnect between the token bit manager (TBM) and readout chips (ROCs)
- Optimized to be as thin (X_0/X) as possible
  - 50 µm
  - Molex connector 1.15 mm thick
  - TBM thinned to 100 µm

35 signal and power bonding pads



Test pads for HDI electrical test

TBM

HDI Testing

- Provides bias voltage to the silicon
- Tested for electrical signals before glued to bare module
  - Test pads for high voltage, low voltage, clock, calibration, trigger, reset, and serial data on HDI read through needle card on test stand

serial data

Measure	P1:ampl(C1)	P2:freq(C1)	P3:ampl(C1)	P4:ampl(C2)	P5:ampl(C4)	P6:- - -	P7:- - -	P8:- - -
value	21.792 mV	6.770261 MHz		22.345 mV	1.811 V			
status	✓	✓		✓	✓			

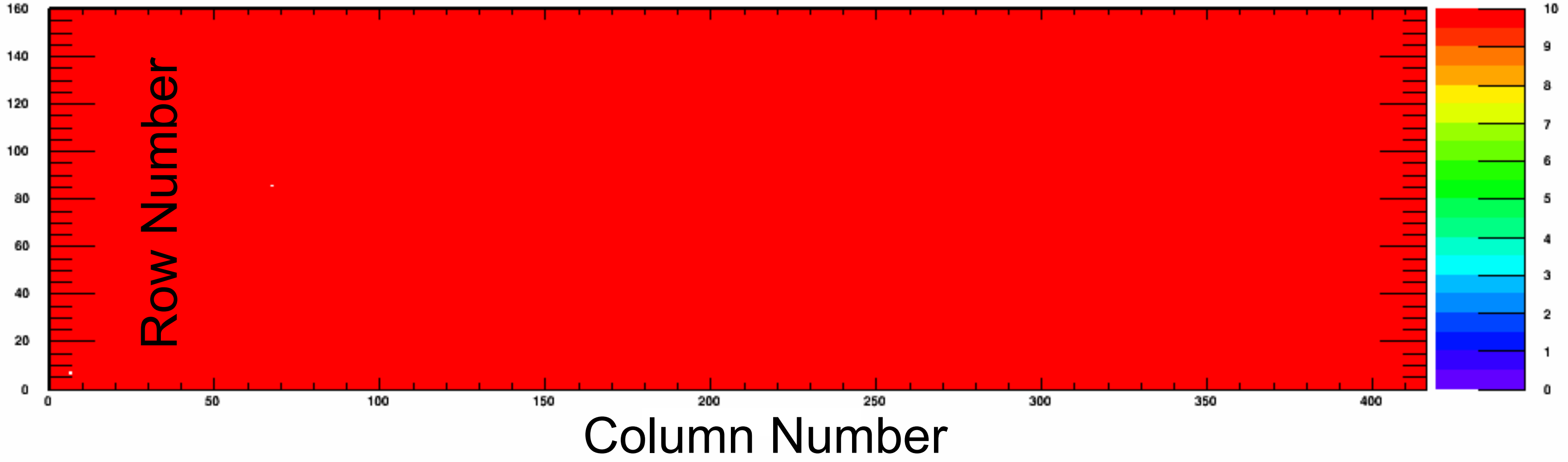
C1 FLT DC50	C2 FLT DC50	C3 DC50	C4 DC50
5.00 mV/div	5.00 mV/div	500 mV/div	500 mV/div
-112.200 mV	-109.800 mV	-1.435 V ofst	-1.445 V ofst
---- 122.20 mV	---- 119.80 mV	---- 2.435 V	---- 2.445 V

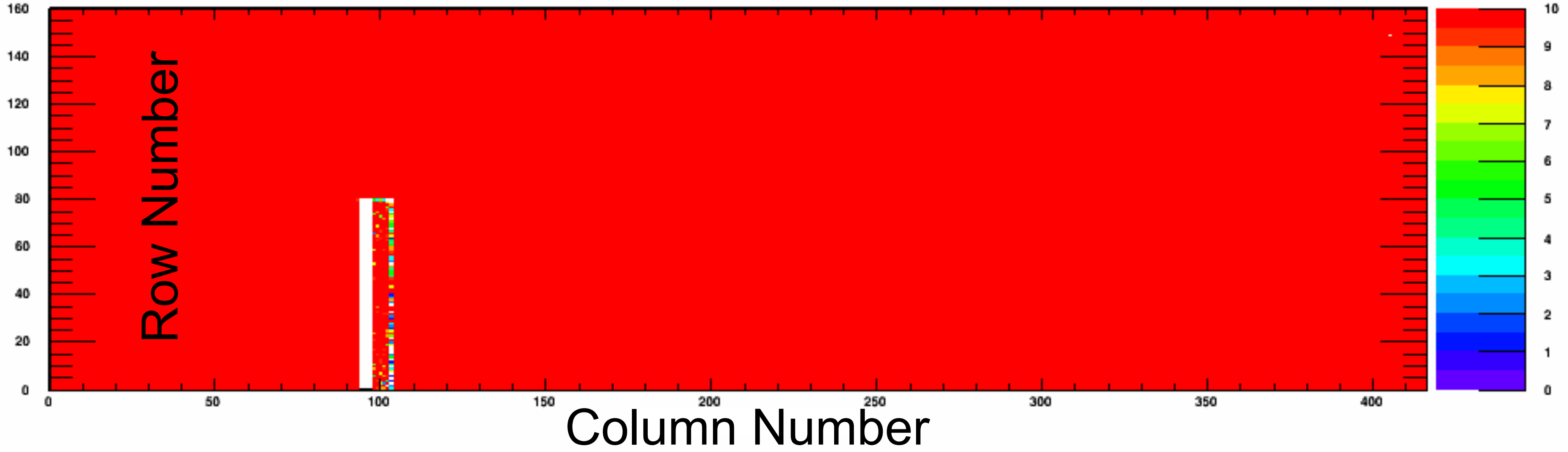
Timebase -2.56 µs
1.00 µs/div
50.0 kS 5.0 GS/s

Trigger C4 DC
Stop 800 mV
Edge Positive

Bare Module

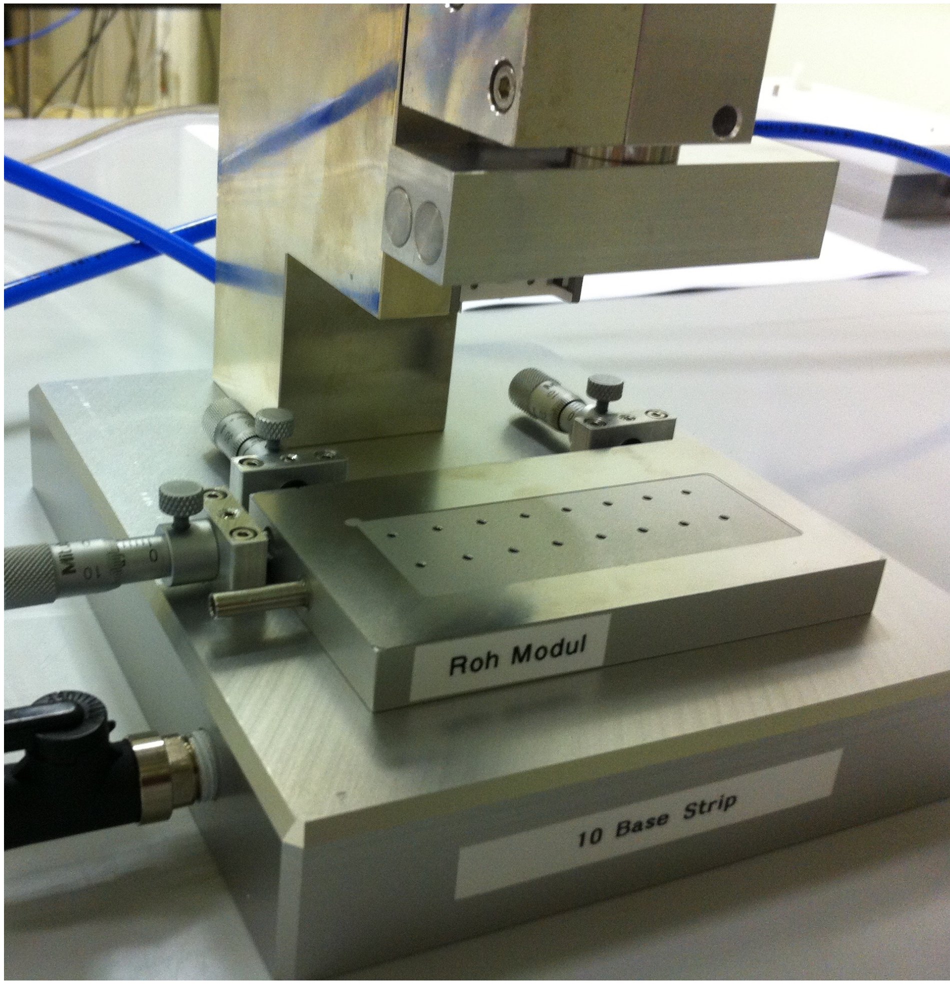
- First step in module assembly is to bump bond silicon sensor to 16 ROCs creating a bare module
- Bare modules are tested before assembly

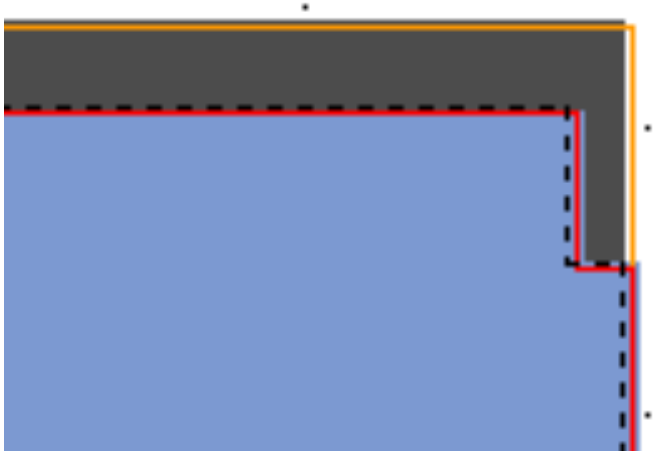




Assembly

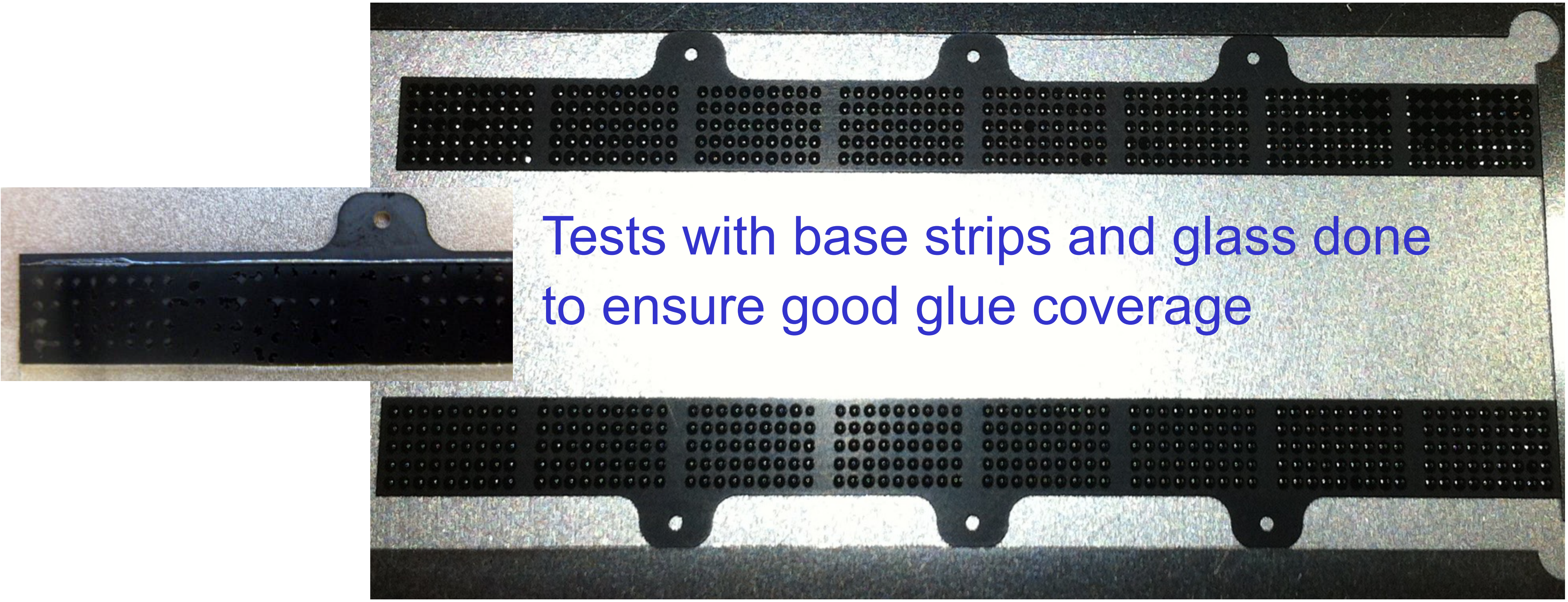
- Gluing in two stages
  - Base strips glued under bare module
  - HDI glues on top of bare module
- Identical jigs used in 5 assembly centers across Europe
- Alignment key
  - 50 µm precision required
  - Computer program developed to use measurements from CMM to set micrometric screws on jig for alignment





Base Strip Gluing

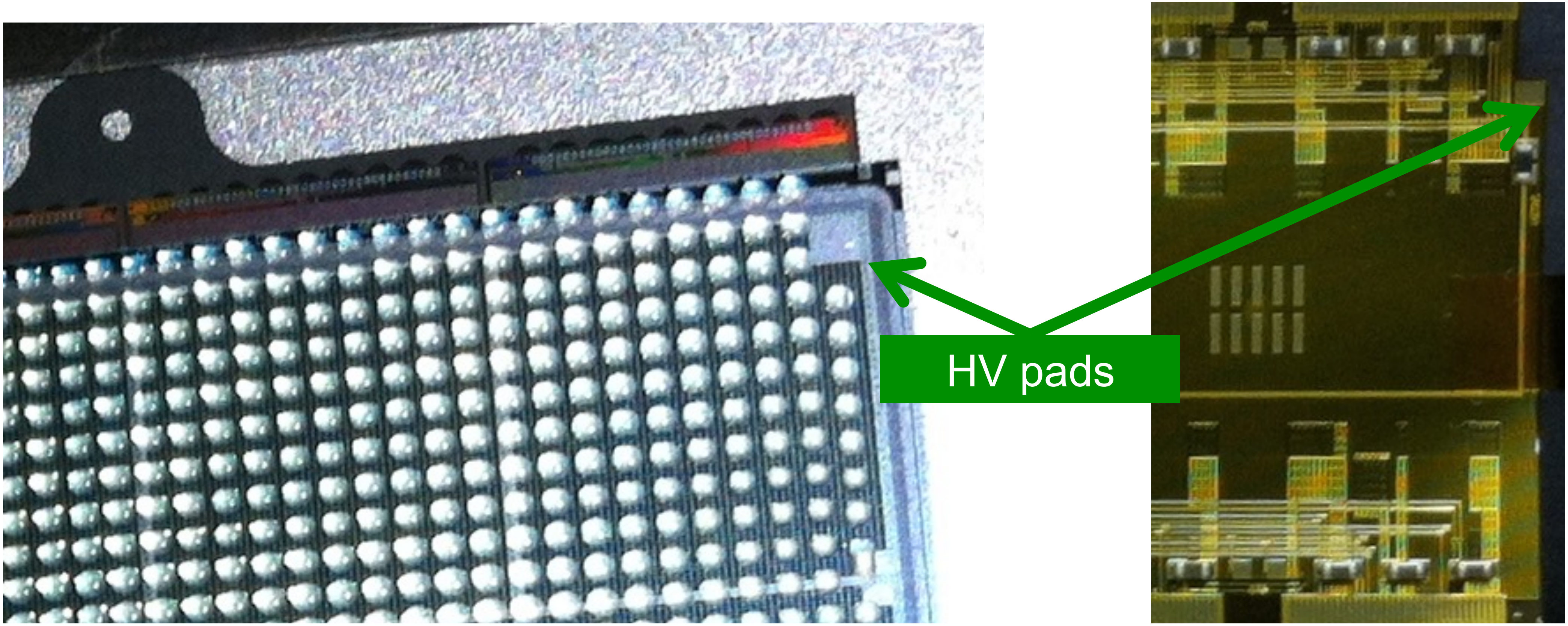
- Desire full coverage of glue on base strips but no glue between ROCs nor outside of the base strip edges
- Base strips cool and hold module in place
  - 200µm thick SiN
- Glue (Araldite 2011) conducts heat more efficiently than air
  - Full, even coverage of glue on base strips essential to cooling modules



Tests with base strips and glass done to ensure good glue coverage

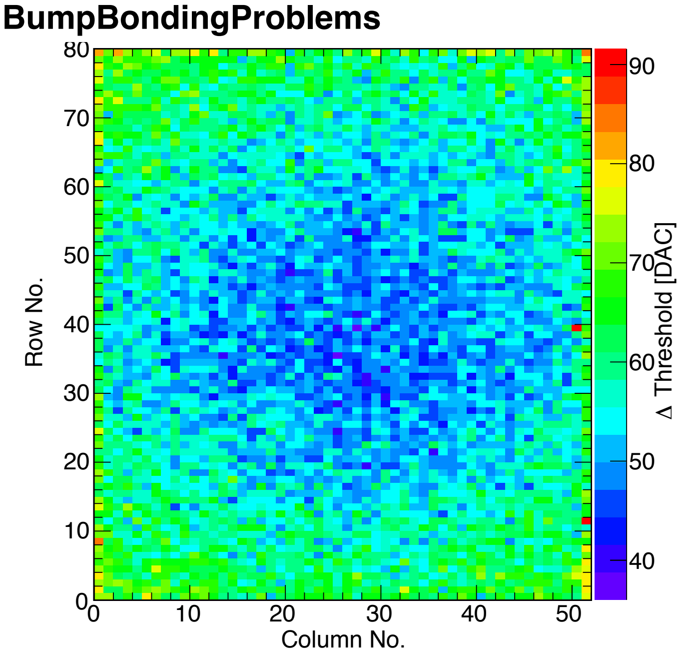
HDI Gluing

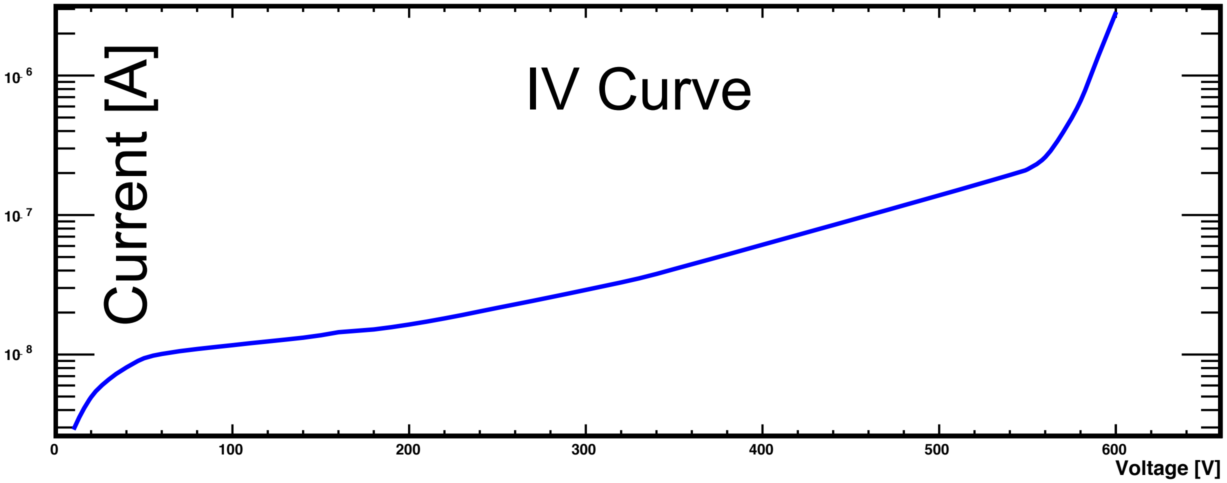
- HDI must be well supported by glue so bonding pads on the edge of the HDI do not move while bonding ROCs to HDI
- HV pad on the HDI is in the corner and must be lined up with the bias pad of the sensor
  - There needs to be enough glue to hold the HV pad but not so much glue that the bias pad of the sensor is covered in glue preventing bonding

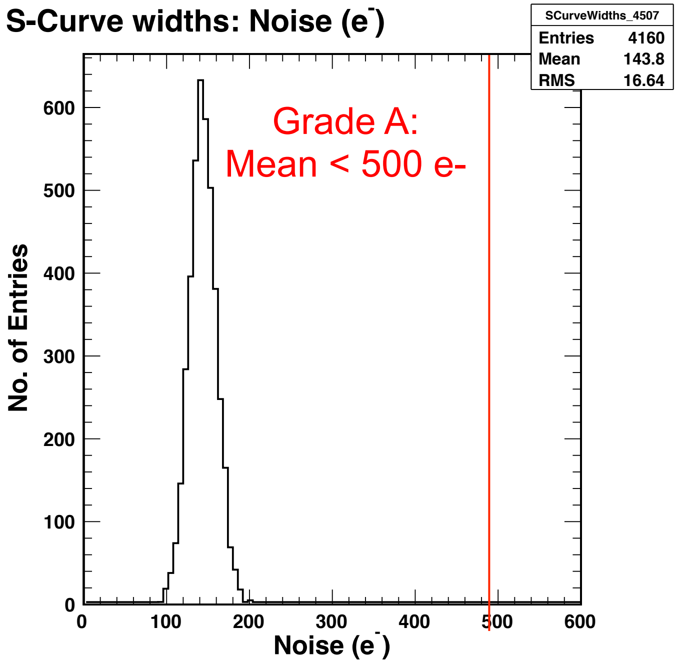


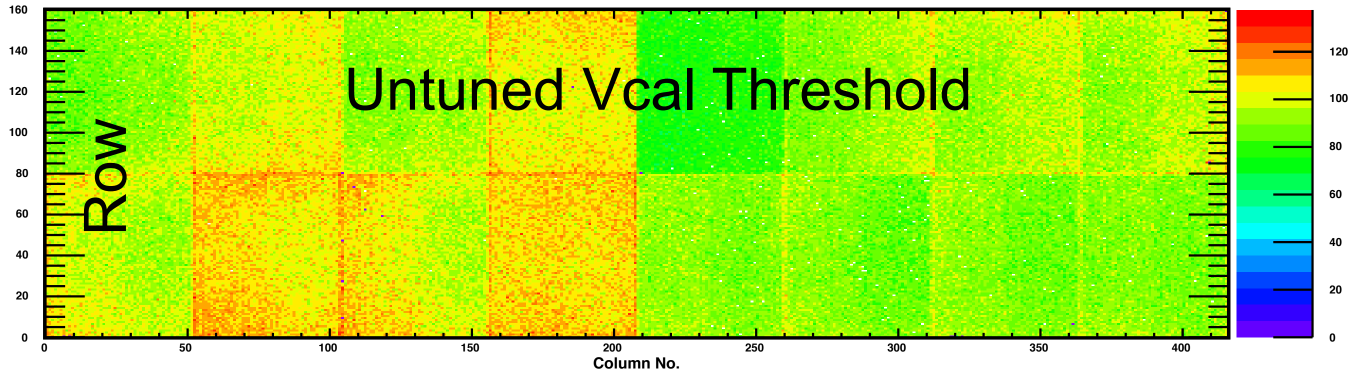
Full Qualification

- Module thermal cycled from 17°C to -25°C ten times
- Modules tested for full functionality at 17°C and -20°C



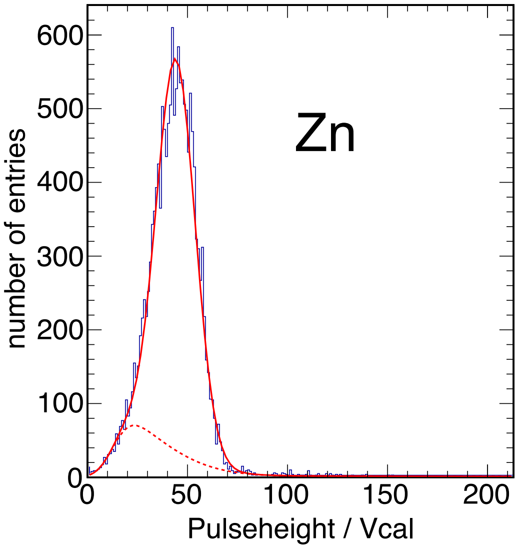


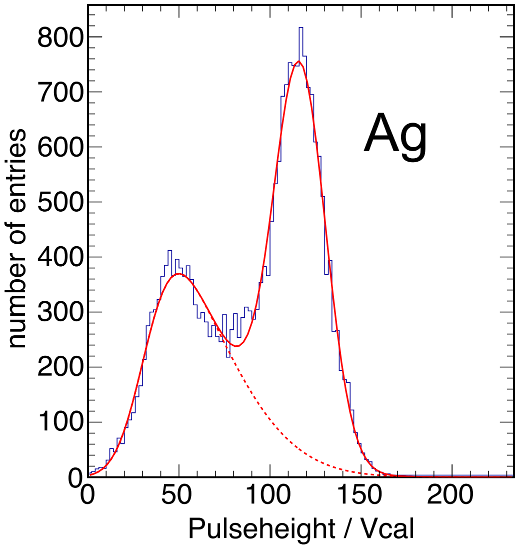


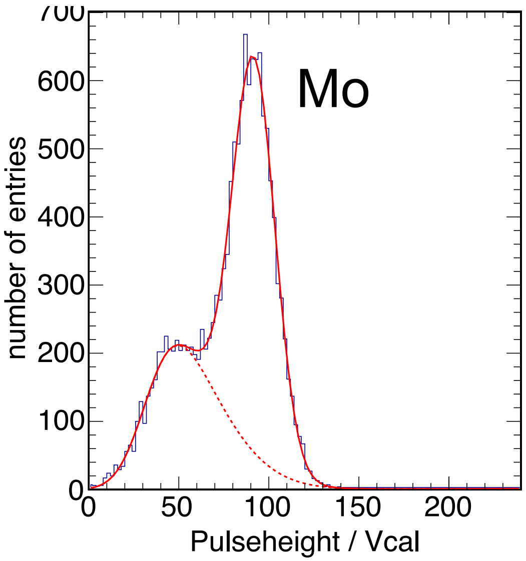


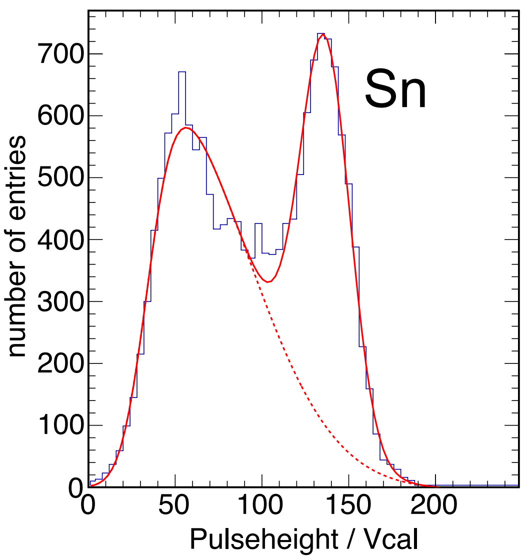
Calibration

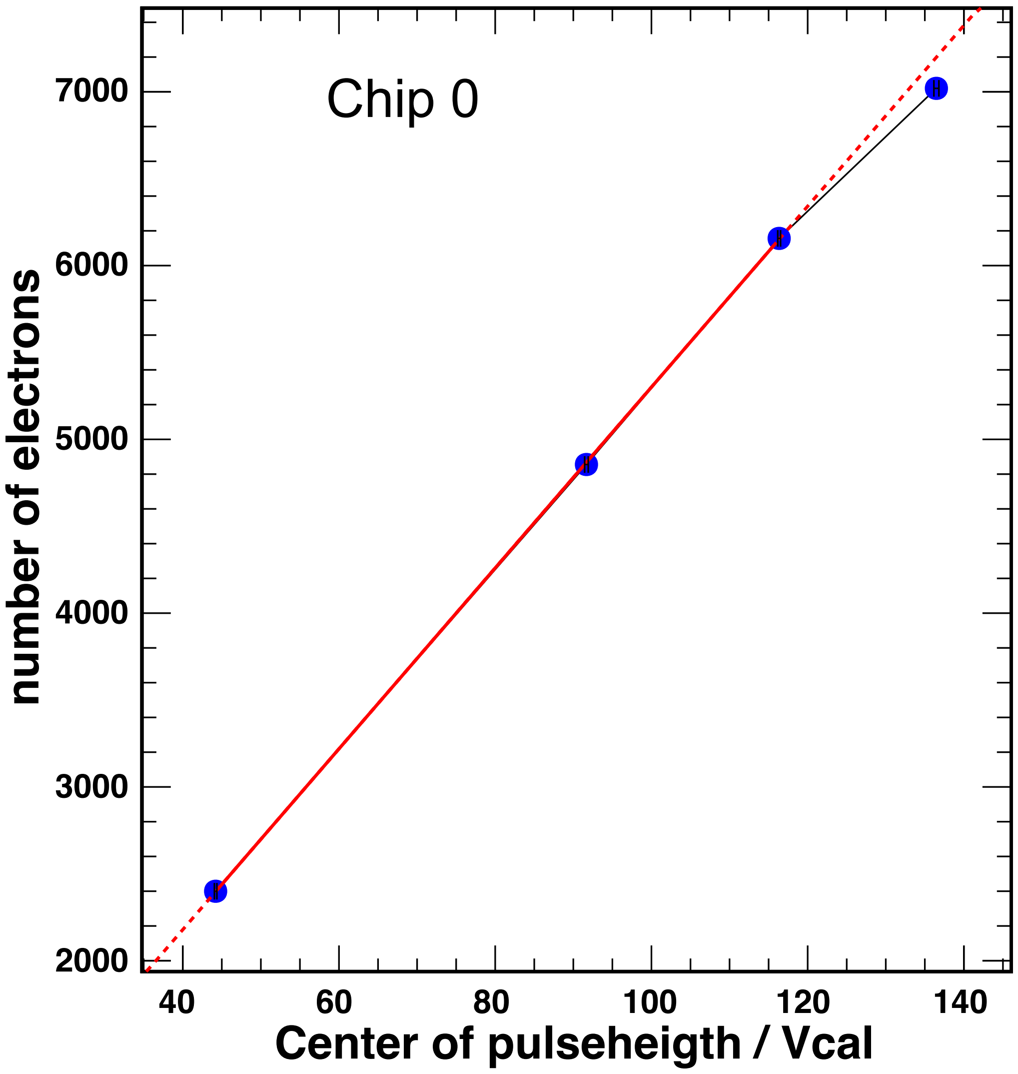
X-rays used to determine the number of electrons for a pulse height at a specific calibration voltage (V_{cal}) using florescence lines from 4 elements: zinc, silver, molybdenum, and tin







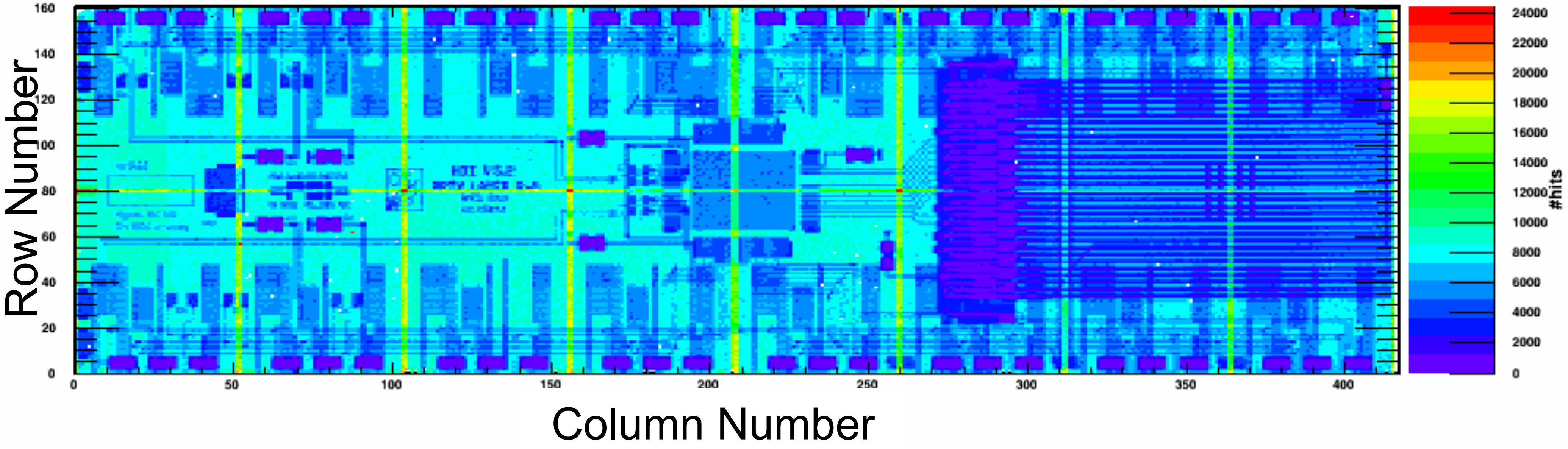




High Rate Test

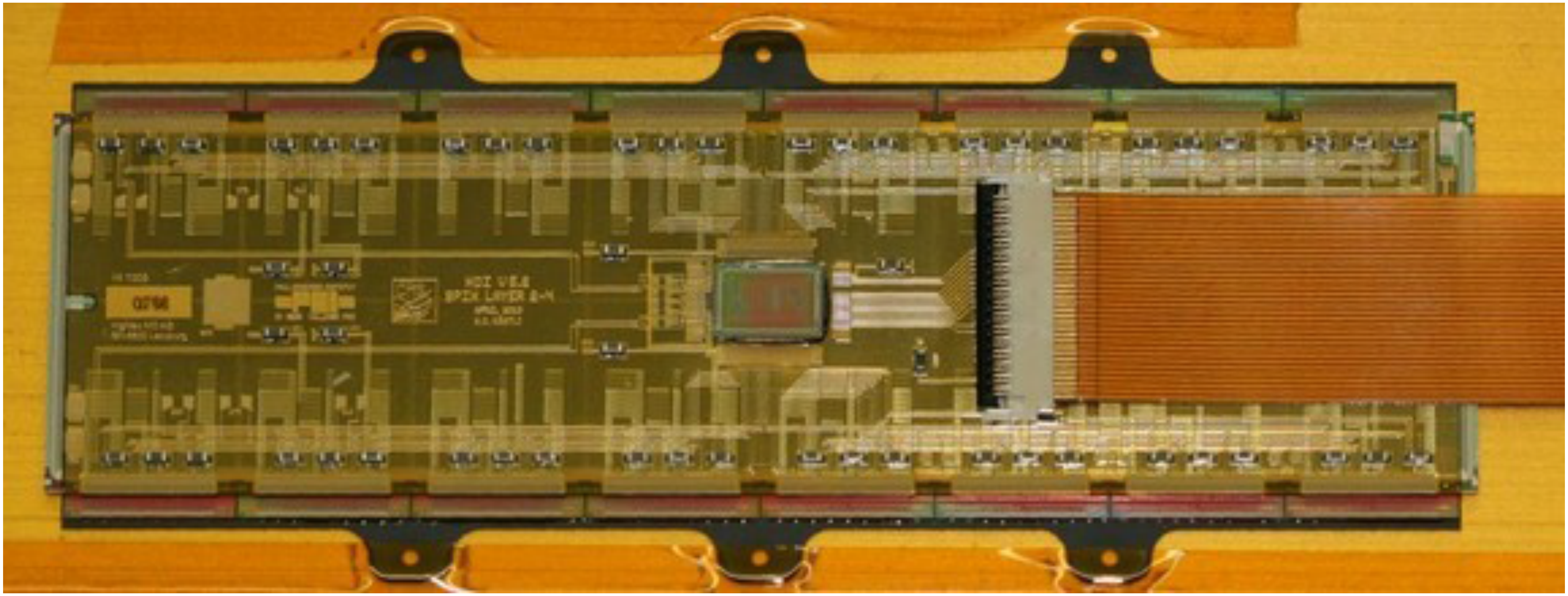
- Module tested at higher rates with X-rays
- Efficiency compared at 50 MHz and 120 MHz to ensure high pixel performance
- Results not finalized
  - software still in development
  - Mask noisy pixel for this test
    - Definition of noisy pixel in flux
- Shadow of HDI can be seen

Module	**M3015**
Grade	A
ROC Grades A/B/C	16/0/0
Pixel Defects	24
Efficiency 50/120	99.94/99.15 %



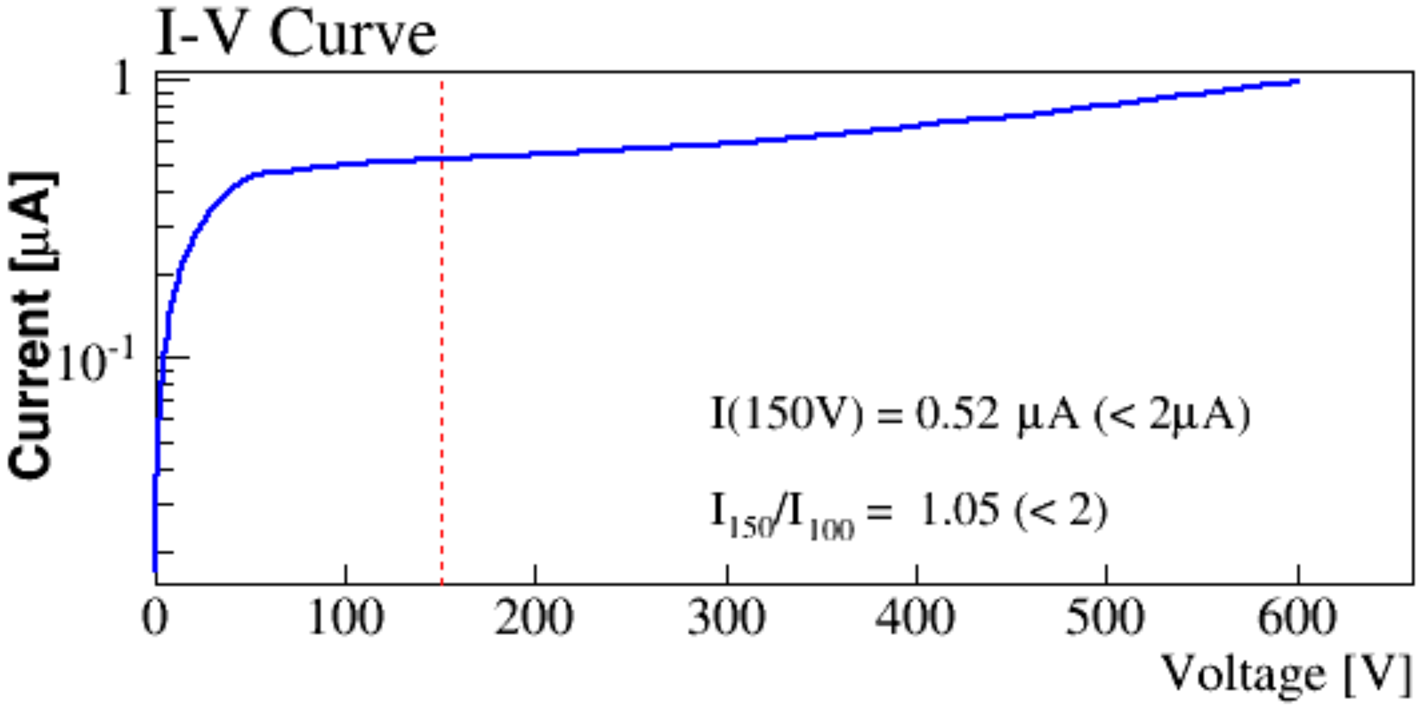
Summary

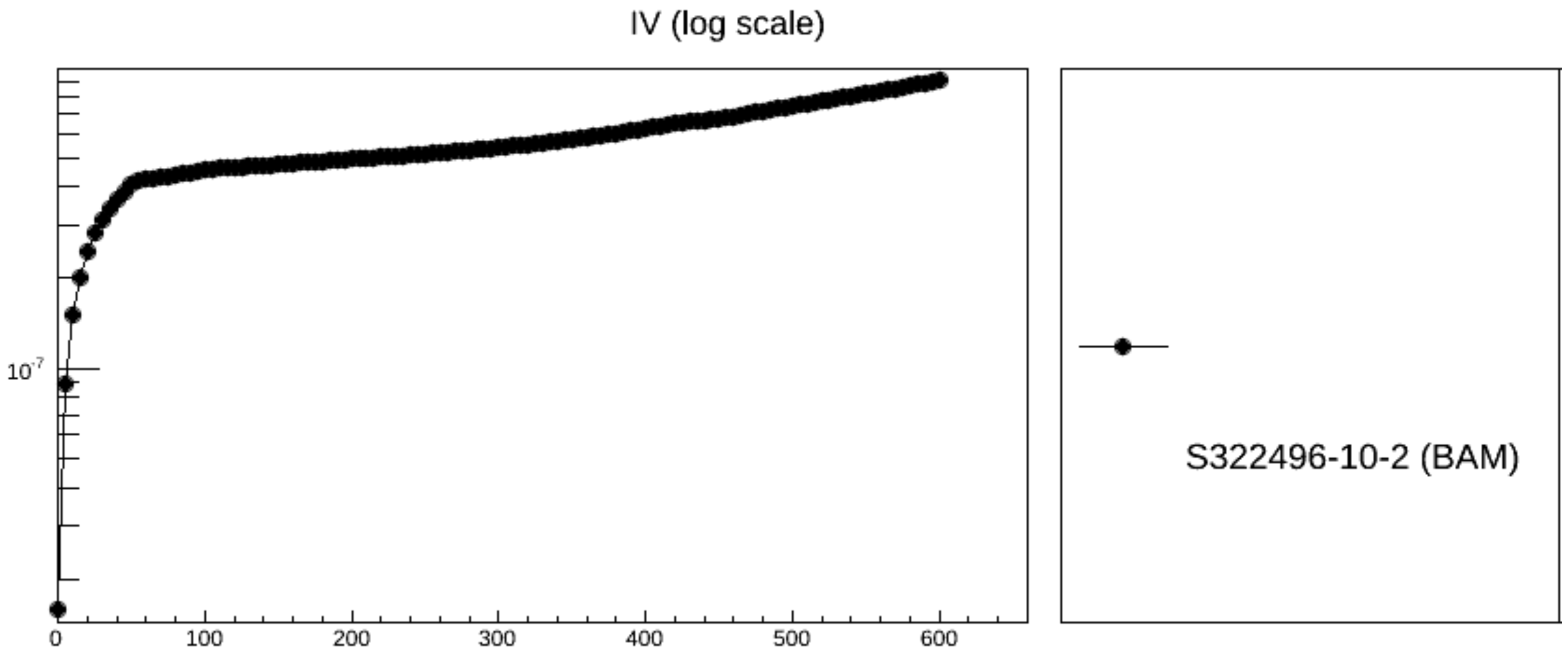
- Production of modules has already started
- Testing done at each stage of assembly to ensure high quality modules



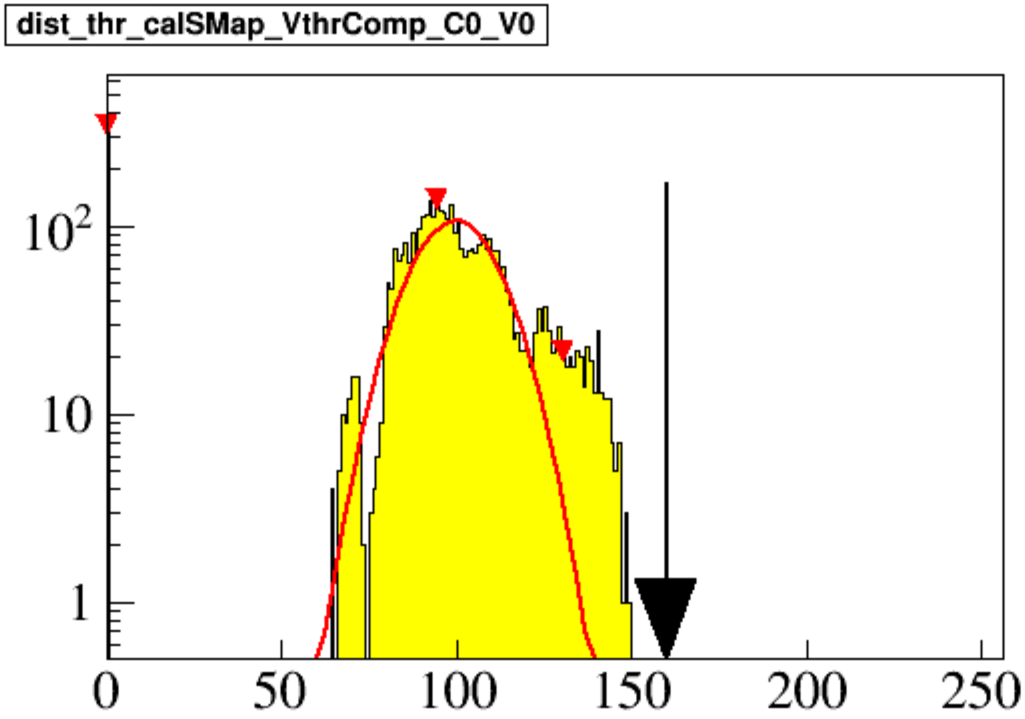
Back Up

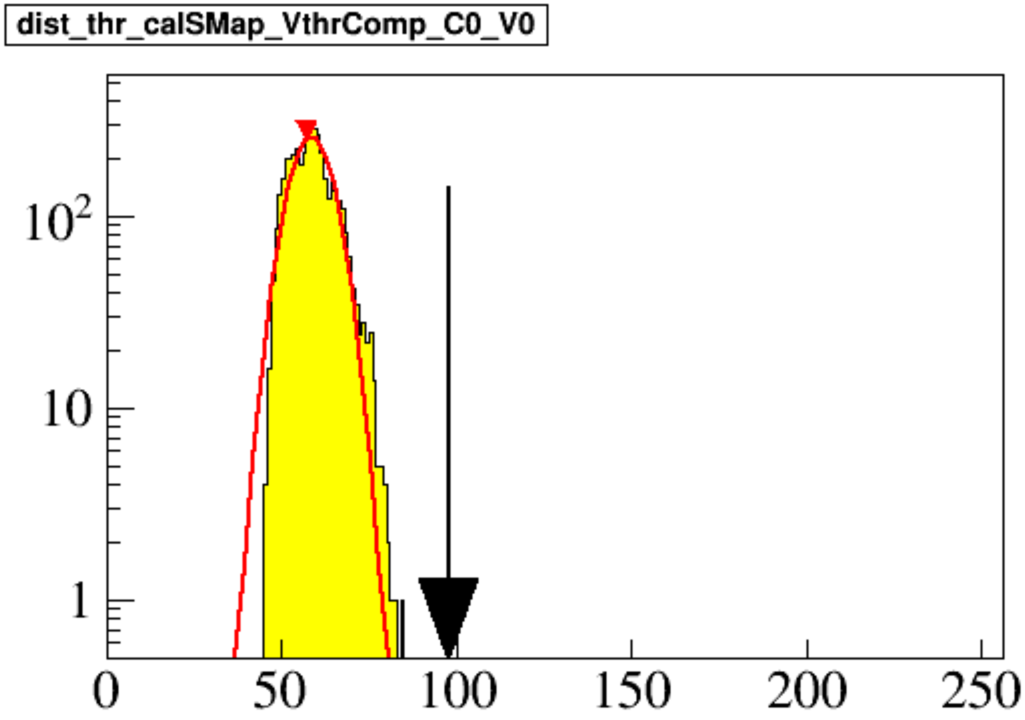
Bare Module IV





Bump Bonding Test





ROC Inefficiencies

Inefficiencies versus particle hit rate from DataFlow simulation