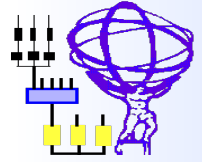


ATLAS DAQ/HLT Architecture for Phase II

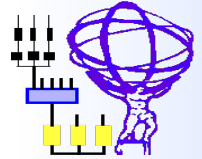
W.Vandelli - CERN Physics Department/ATD



Outline



- ATLAS DAQ/HLT Architecture Evolution from Run 1 to Run 4
- New Detector Readout Architecture
- FELIX Project
- Projected HLT Farm Size



DAQ/HLT Upgrade Plans

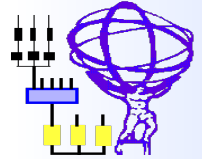


- Driving Parameters

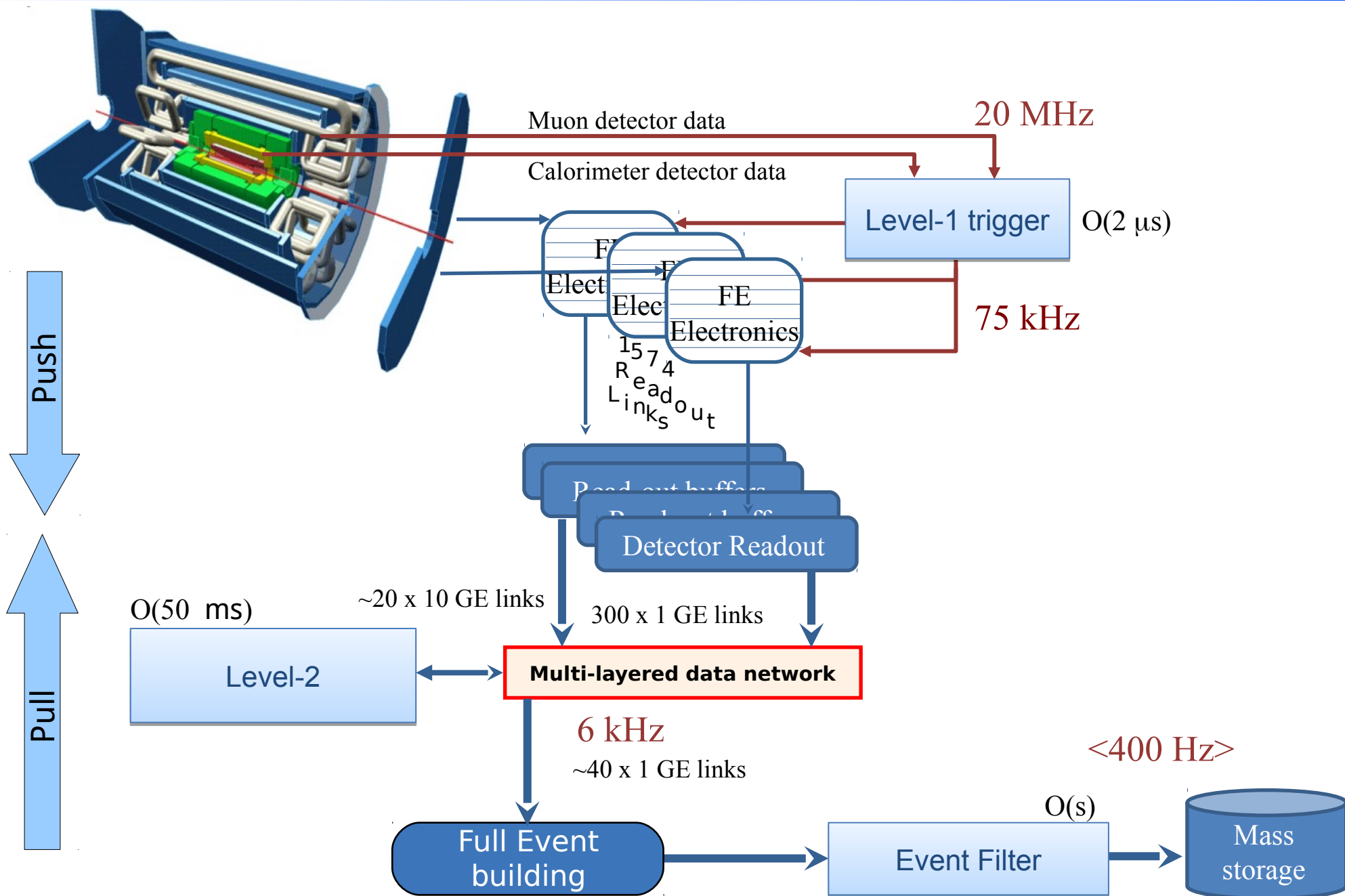
	# of Trigger levels	Level-xRate (kHz)	Event Size (MB)	Network BW (GB/s)	Storage GB/s	Storage kHz
Run 1	3	Lvl-1 75 HLT ~0.4	~1	10	0.5	~0.4
Run 2	2	Lvl-1 100 HLT 1	~2	50	1	1
Run 3	2	Lvl-1 100 HLT 1	~2	50	1	1
Run 4	3	Lvl-1 400 HLT 10	~5	2000	25	10

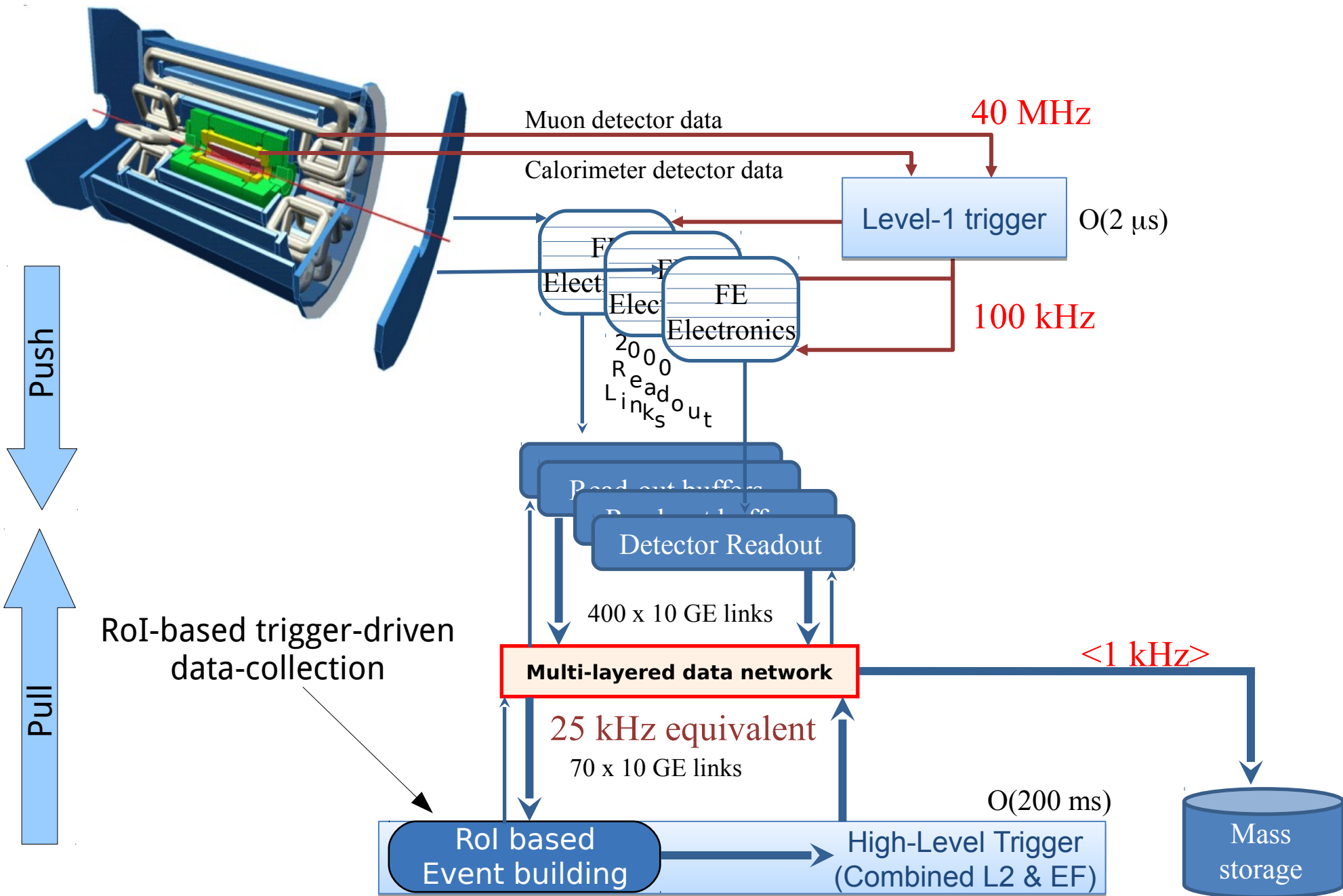
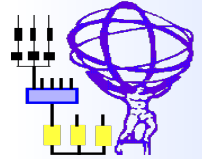
- Notes

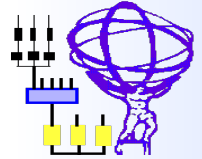
- Storage bandwidth includes compression factors
- Run 3: No major upgrades in the DAQ systems currently foreseen
- Run 4: Two stage hardware trigger (Level-0 and Level-1)**



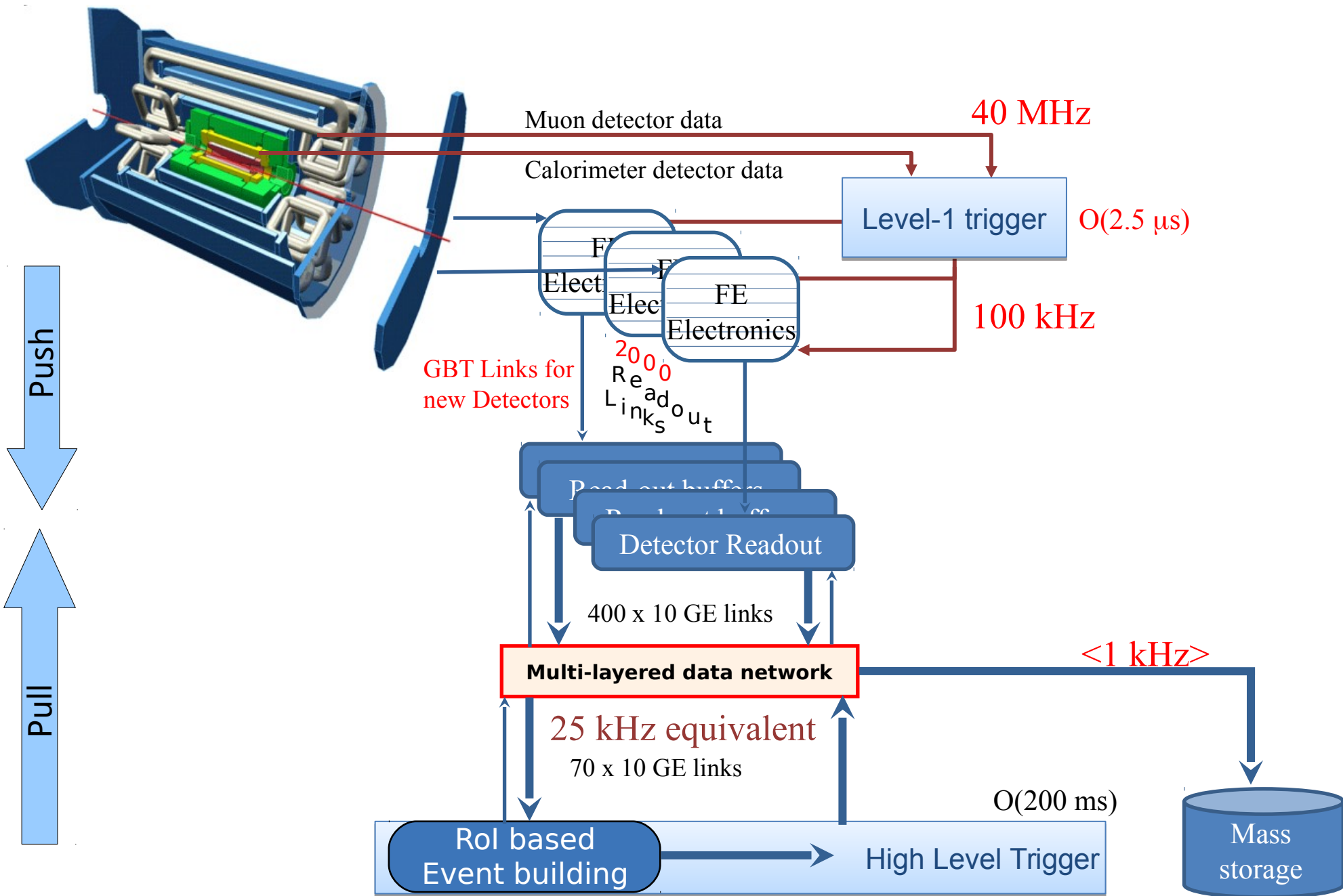
ATLAS Run 1

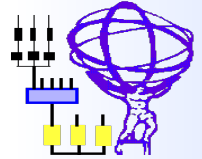




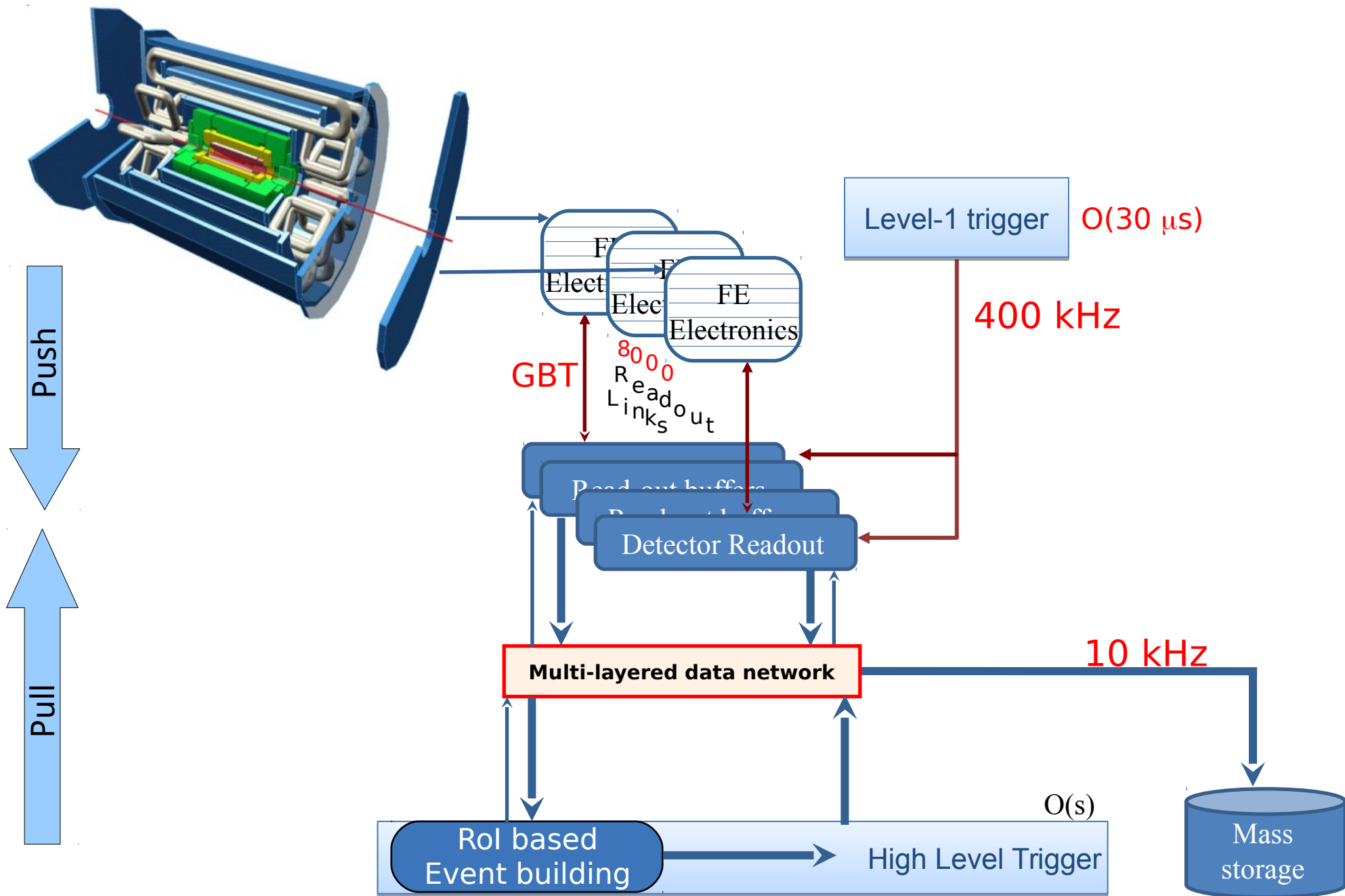


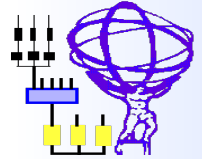
ATLAS Run 3



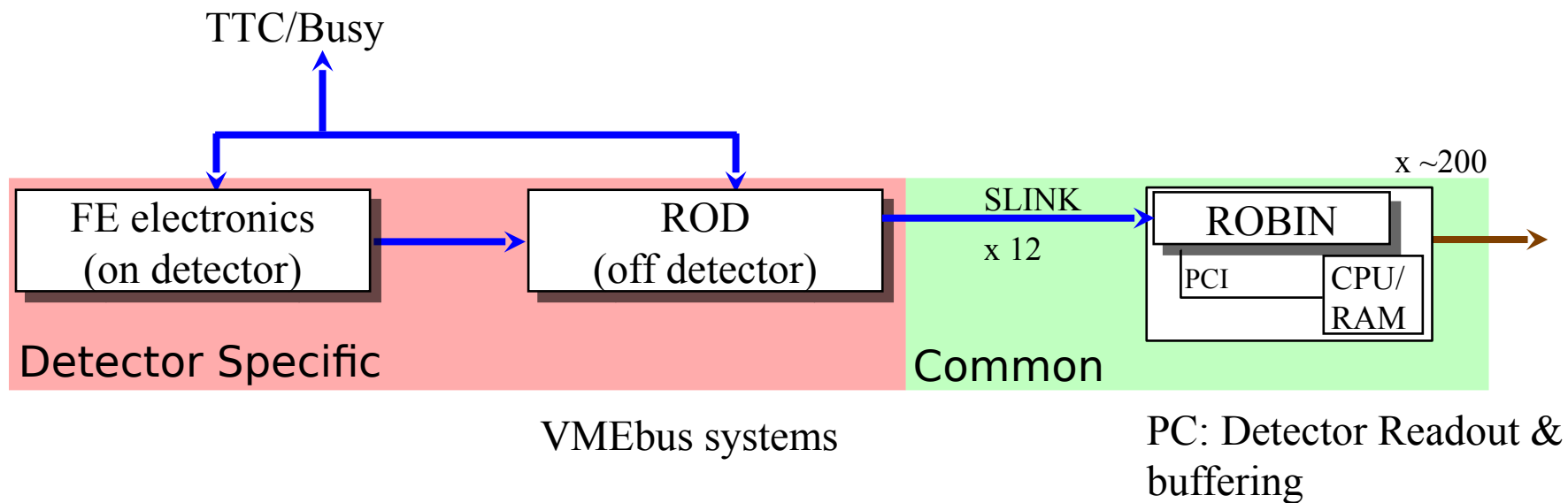


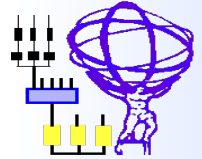
ATLAS Run 4



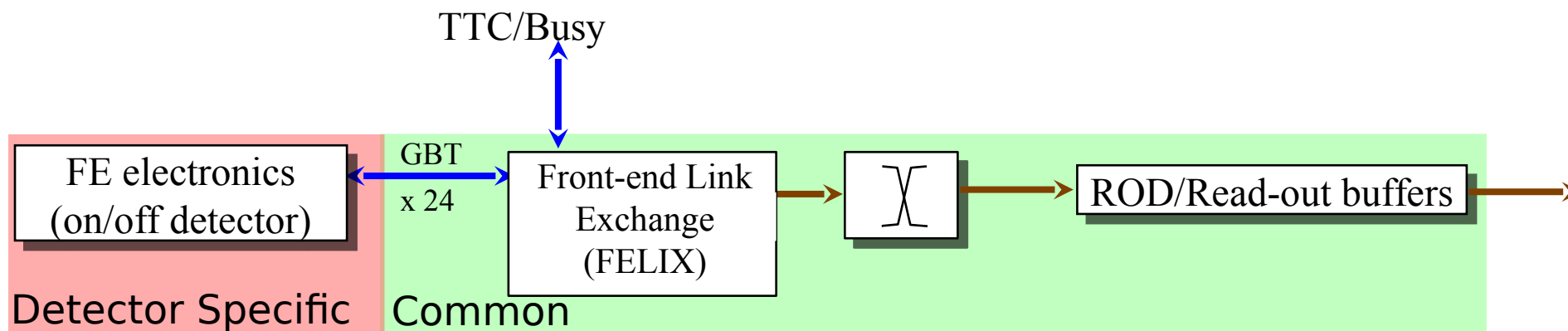
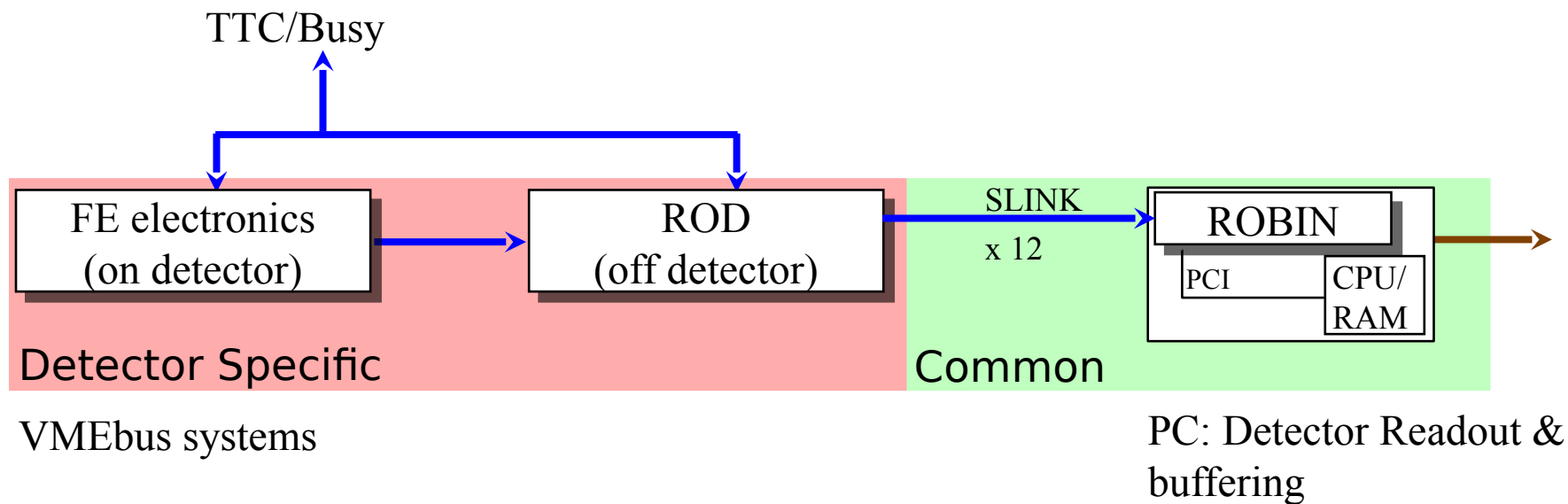


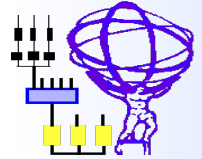
Detector Readout Run 1-2



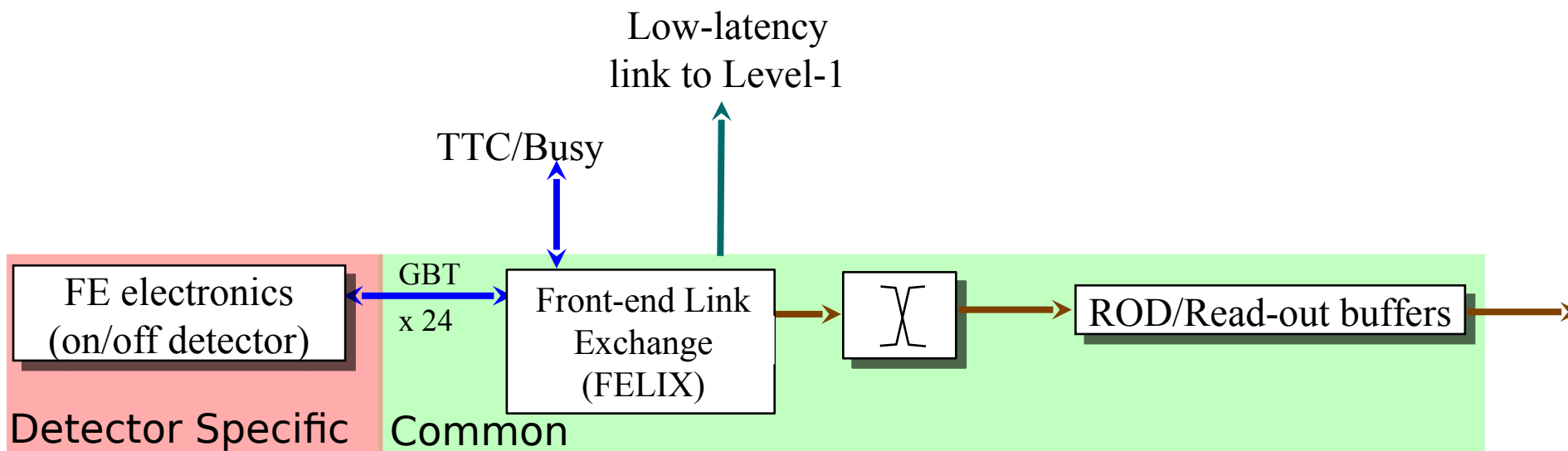


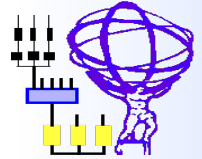
Detector Readout Run 3



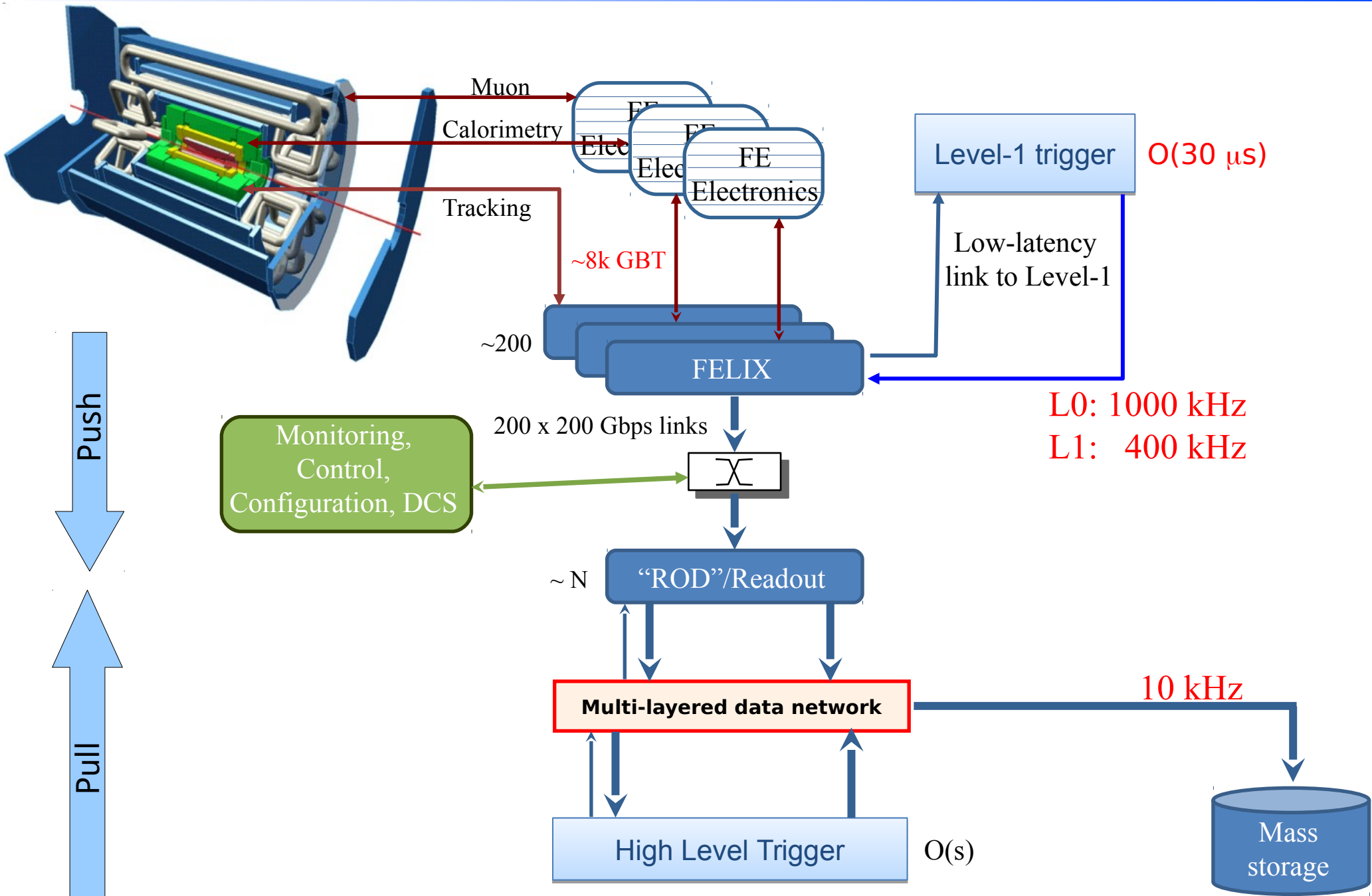


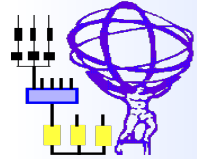
Detector Readout Run 4





Architecture in Run 4

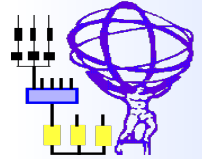




Run 4 Readout: Advantages



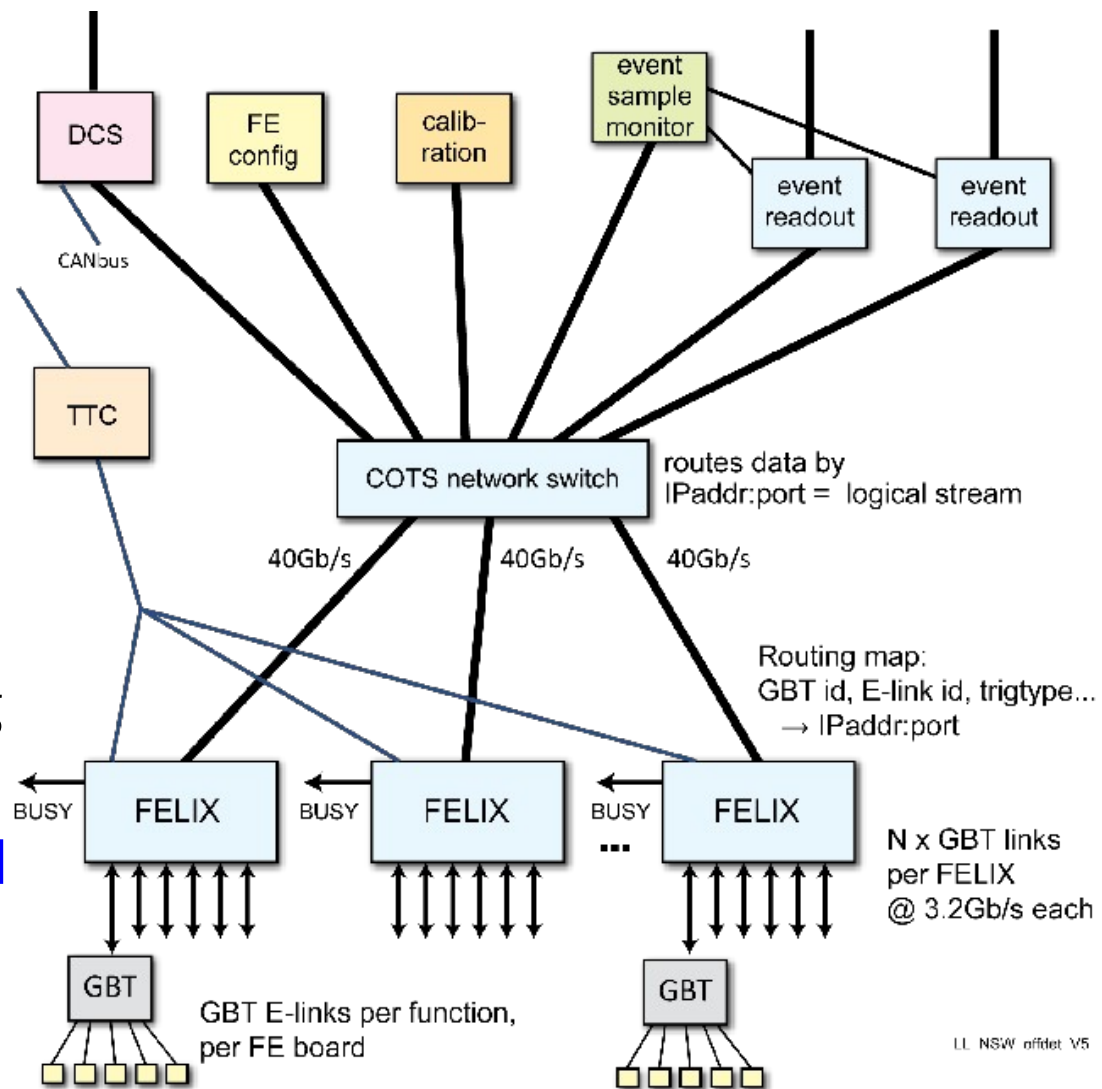
- Higher level of commonality between detectors
 - FELIX is a common object providing functionality today implemented in detector-specific back-end custom elx (ROD)
- Performance-scalability built-in
 - programmable FE-DAQ connectivity
 - e.g. able to de-populate DAQ buffers whether needed to accommodate higher requirements, like increasing L1 rate
- Increased use of COTS components
 - all ROD-like functionality (including data processing) could most likely be implemented in standard computers by Phase-II
- Capability to disentangle ROD-like functions from H/W implementation
 - different granularity for monitoring, control, data handling ...
 - DCS and DAQ traffic separation

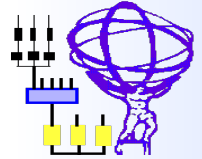


FELIX Functionalities

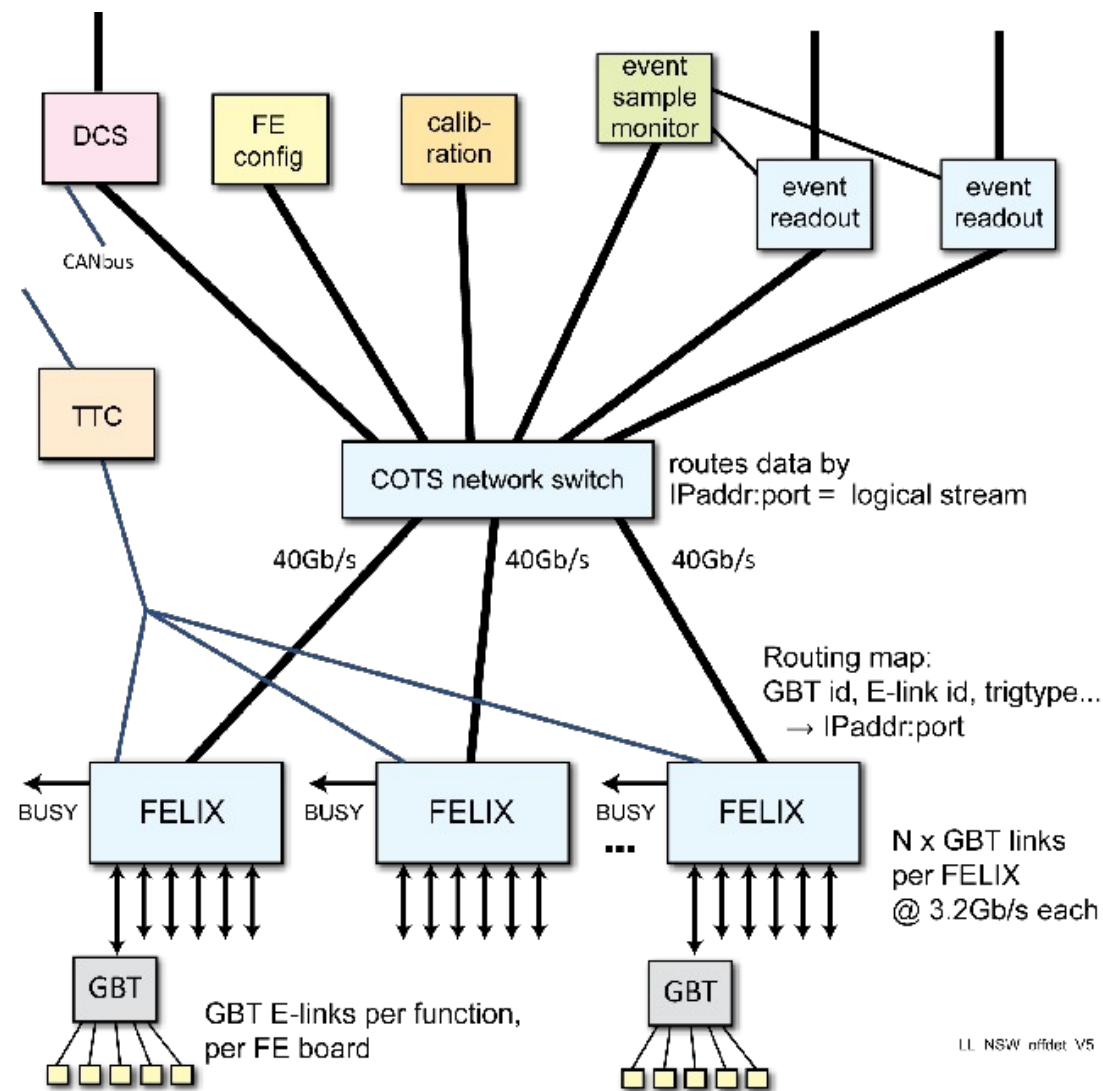


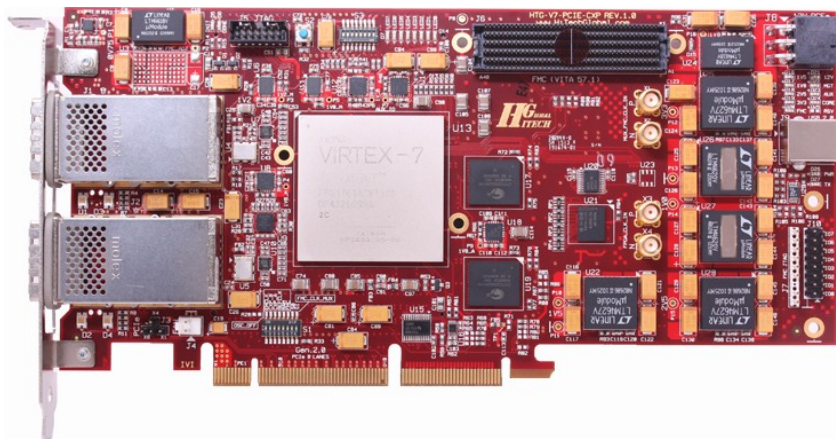
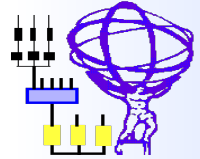
- **Configurable** data routing device
 - route data **by E-link and/or streams**
 - **advanced routing** based on L1 ID or Trigger type
 - allow for intermediate data-aggregation step
 - data duplication and sampling for monitoring
- **Handling of high-level switched protocol**
 - Infiniband/Ethernet/...
 - QoS for different traffic types





- **TTC handling**
 - busy handling (no back pressure on GBT)
 - isolates FE electronics from TTC evolution
 - may provide L1 and ECR counting
 - same implementation across ATLAS
- **Dedicated low latency path for critical data**
 - e.g. Level 1 trigger input data for L0/L1 trigger architecture
- **Command synchronisation for calibration**
 - programmable sequences
 - synchronisation through TTC



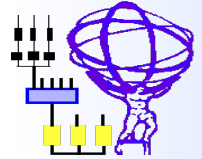


- Show feasibility, investigate technology
- Support Phase-I detector developments
 - forward compatibility with Phase II

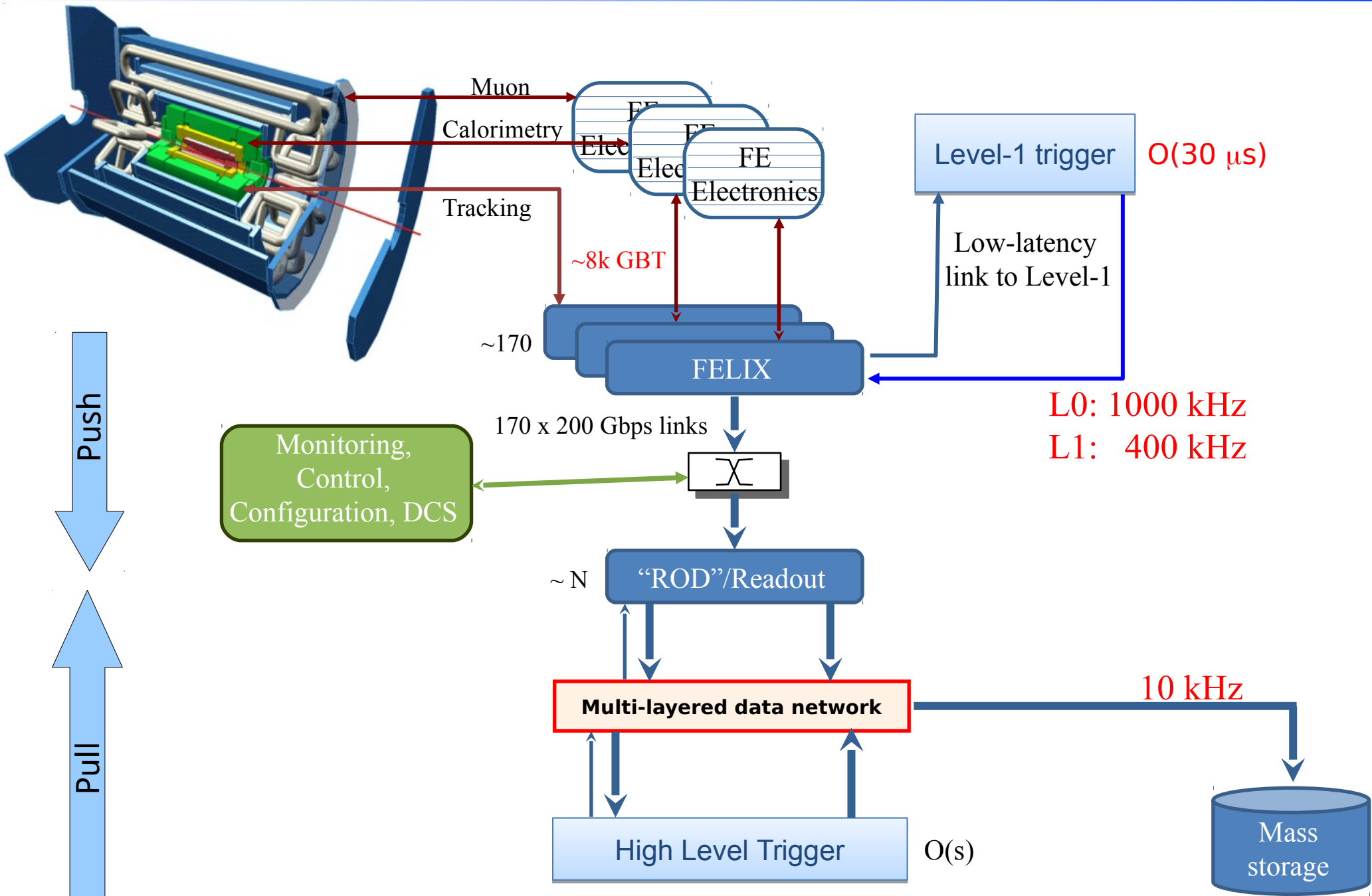
- **Hitech Global HTG-710**
 - 2 CXP cages: can connect 24 bi-directional links
 - With Virtex-7 X690T FPGA (for PCIe Gen3 8 lanes)
- **Intel server board S1600JP**
 - 3 PCIe Gen3 slots
- **Scheduled for Q1'15**
 - final design review in Q2'15

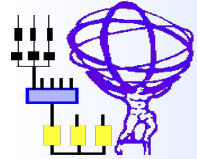


Not final solution/technology

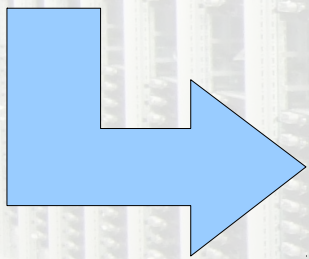


Architecture in Run 4





- Processing time extrapolations to PU = 200
 - Run 4 rejection requirements similar/better than in Run 1-2 → 1k/100k vs 10k/400k
- A factor **O(50)** in HLT compute power needed wrt to Run 1
- Moore's law on a ~10 years period predicts a **factor 100 increase**

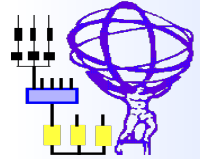


Compute power requirements within expected technology envelope → **HLT farm of similar size wrt to Run 1**

BUT

Software will have evolve to be at least as efficient as today on future technologies (GPGPU, Many-cores, ARM64, ...)

- Assume a similar packaging → **~50 racks**



HLT farm size: network connectivity



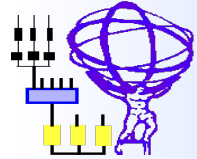
- (Temporary) Disregard RoI approach
 - worst case scenario network requirements
- 5MB@400kHz → **~20 Tbps**
- Reasonable to assume
 - 100 Gbps per CPU socket (computing unit)
 - established (>)400 Gbps technology
 - Infiniband EDR x12 → 300 Gbps

Run 2(*)	# of 10 Gbps links
ROS	400
HLT	100

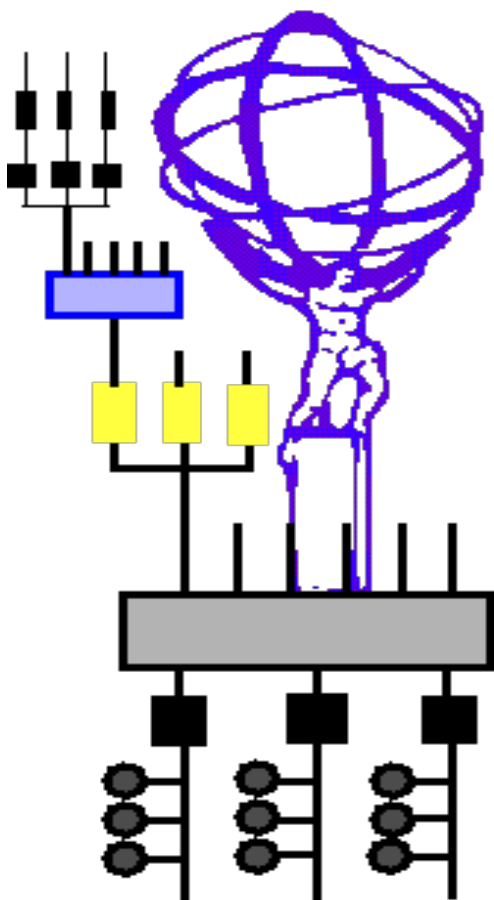
Run 4	# of 400 Gbps links
FELIX	200
HLT	50

- **Total number of ports ~unchanged**
- Network topology and link speeds mix & match depend on compute power packaging

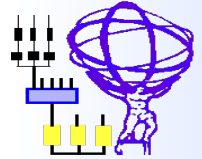
(*) Including redundancy



- **ATLAS Trigger & DAQ Technical Design Report** planned in **Q4 2017**
 - cover Level-0/1, DAQ, HLT and Trigger
- Intermediate milestone with the **Initial Design Review** in **Q1 2016**
- IDR preparation include
 - RoI-based vs full event building
 - use of distributed file systems
 - or other data-management abstraction layers
 - processing time estimates
 - technology tracking
 - especially for FELIX
 - studies on event building traffic and flow control



Extra



ATLAS Level-0 - Level-1

