ATLAS L1 Track Trigger for HL-LHC

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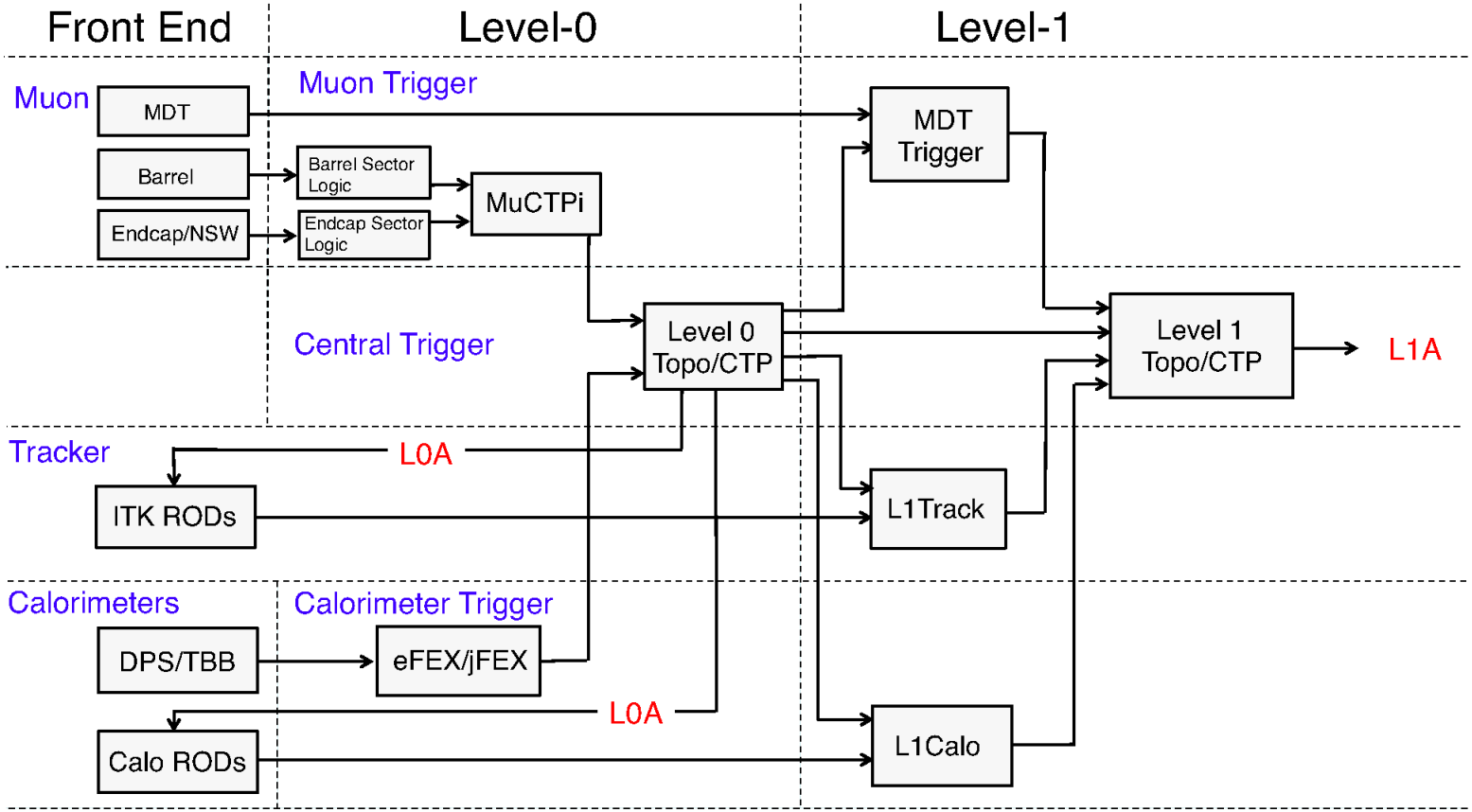
Outline

- ATLAS L0/L1 strategy and L1Track
- ATLAS Tracker upgrade (ITK) layout and readout plans
- Latency considerations for strips regional readout
- L1Track performance studies
- L1Track pattern recognition studies with the ITK layout
- Conclusions

ATLAS L0/L1 strategy and L1Track

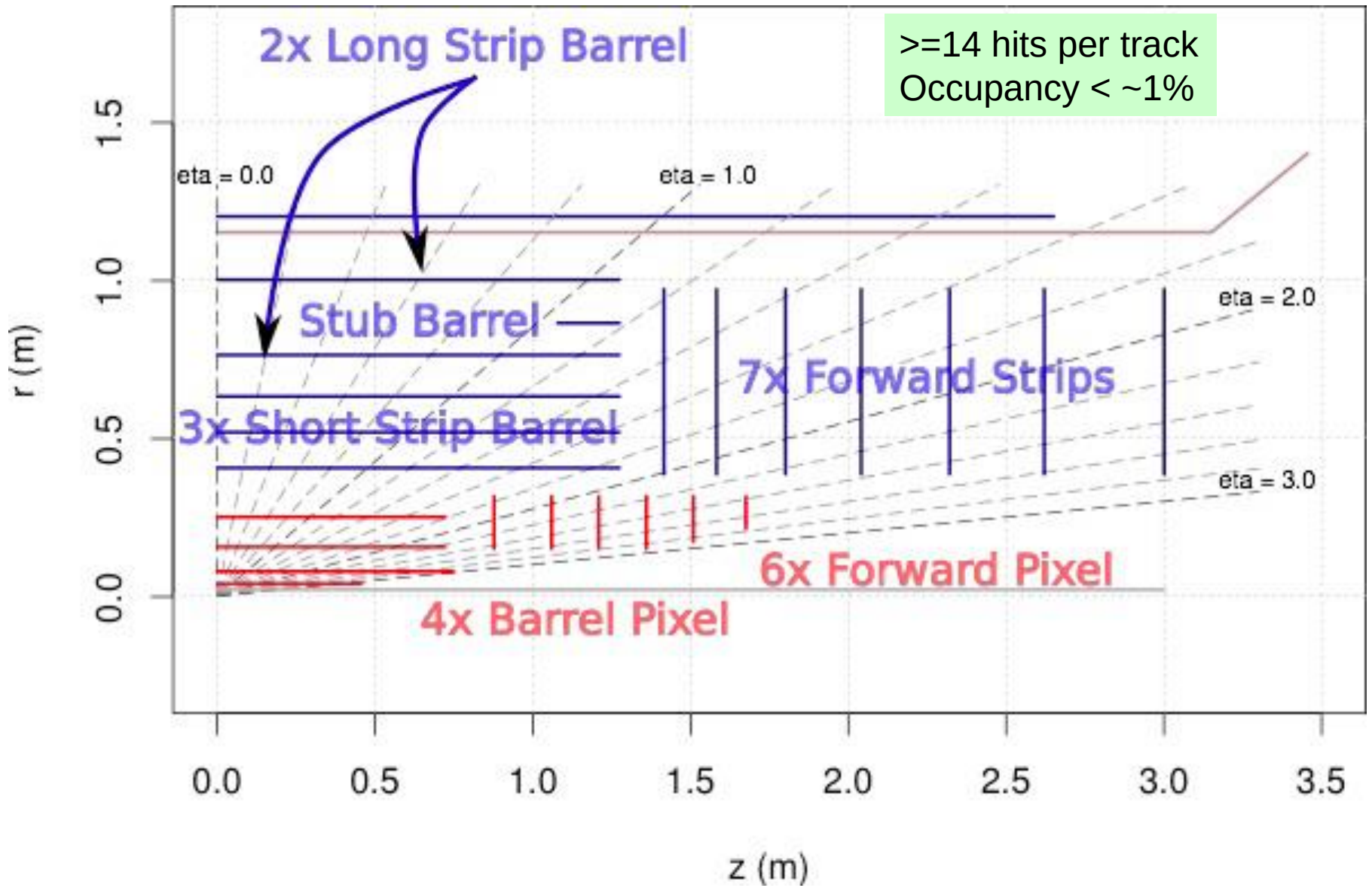
Latency<~6μs, L0A=~1MHz

Latency ~24μs, L1A<~200-400kHz



- Phase-I L1Calo/L1Muon (possibly augmented by MDT trigger) adequate as L0 Trigger at Phase-II for reducing 40MHz to ~1MHz without loss of interesting physics
- Tracking used only on L0 accepted events and optionally only in Regions of Interest (RoI)
- L0A not necessary to be used by all detectors

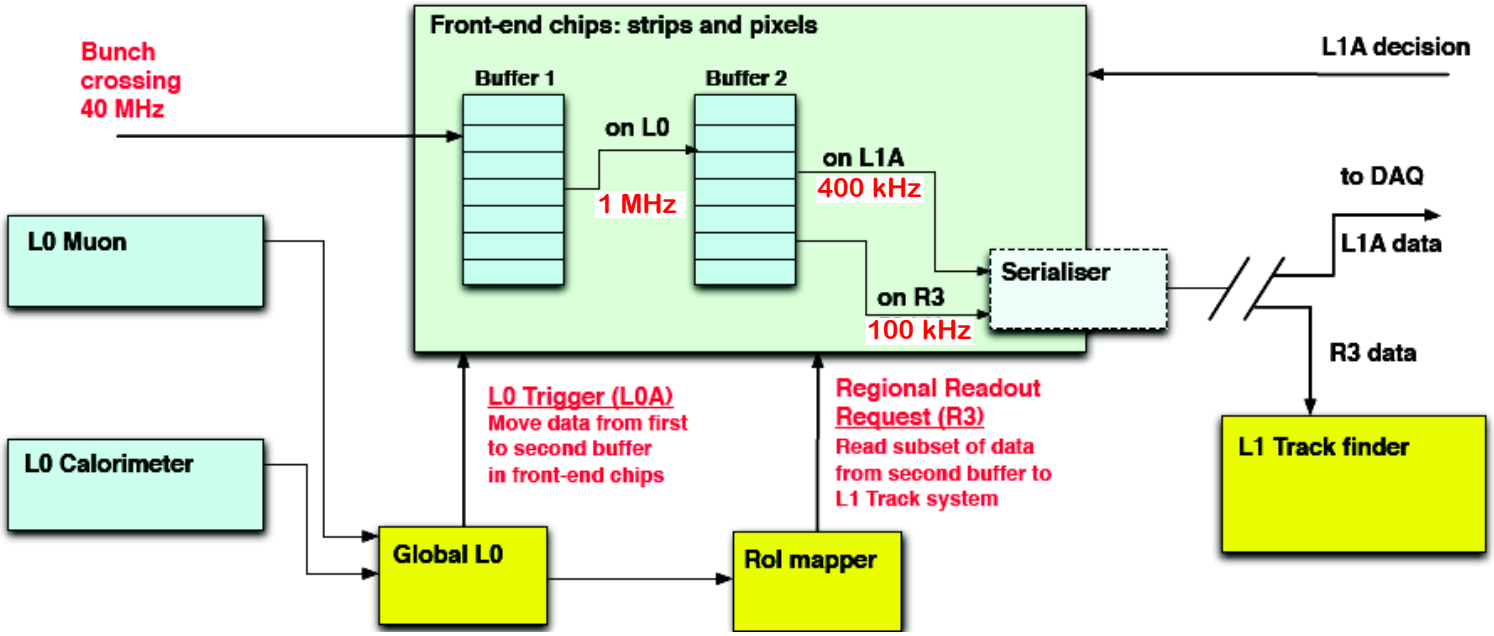
ATLAS Tracker upgrade (ITK) layout



Pixels and Strips readout plans

- The Pixel detector plans to do full readout at 1MHz (i.e. at L0A rate)
  - Provided the readout latency is low, additional flexibility for L1Track
  - So far, Pixel data have not been used in L1Track pattern recognition

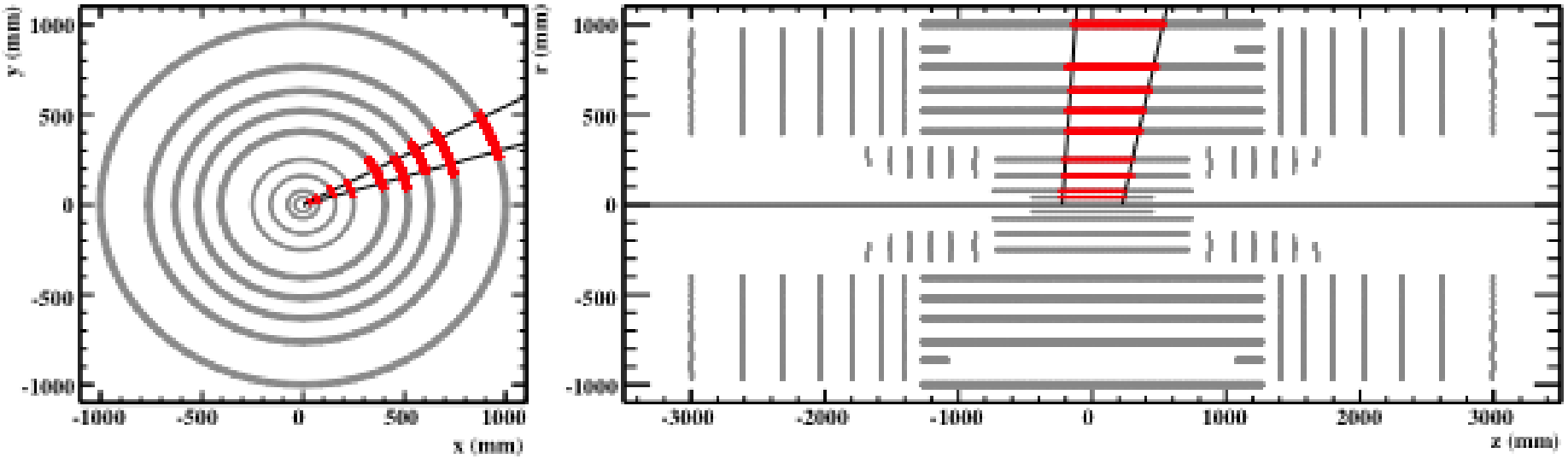
- The Strip detector has already implemented the Regional Readout concept in the recently produced version of the front-end chip (ABC130)
  - We conservatively assume that we would read out 10% of strip modules at L0A



Regional readout

- Only a small fraction of the strip data are read out per L0A
  - Potential saving in services, power, material

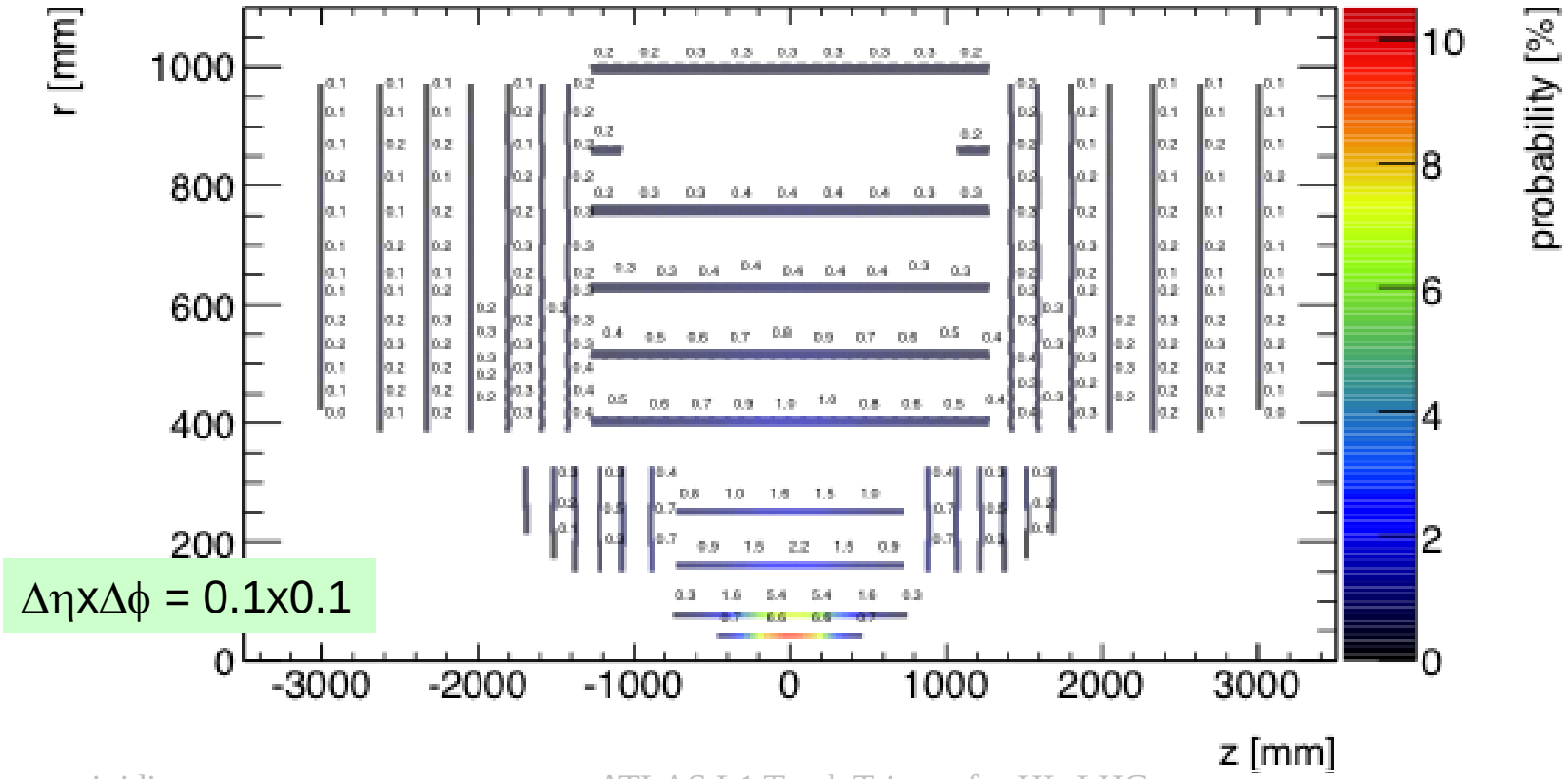
$\Delta\eta x\Delta\phi$ = 0.2x0.2, $\Delta z = \pm 225$mm



  - Opening of RoI near the beam line to account for the spread in beam spot
  - Central modules, closer to the beamline, more frequently inside RoIs

Regional readout

- Only a small fraction of the strip data are read out per L0A
  - Potential saving in services, power, material
- Plot shows the fraction of RoIs containing a given module
  - Assuming uniform distribution of RoIs



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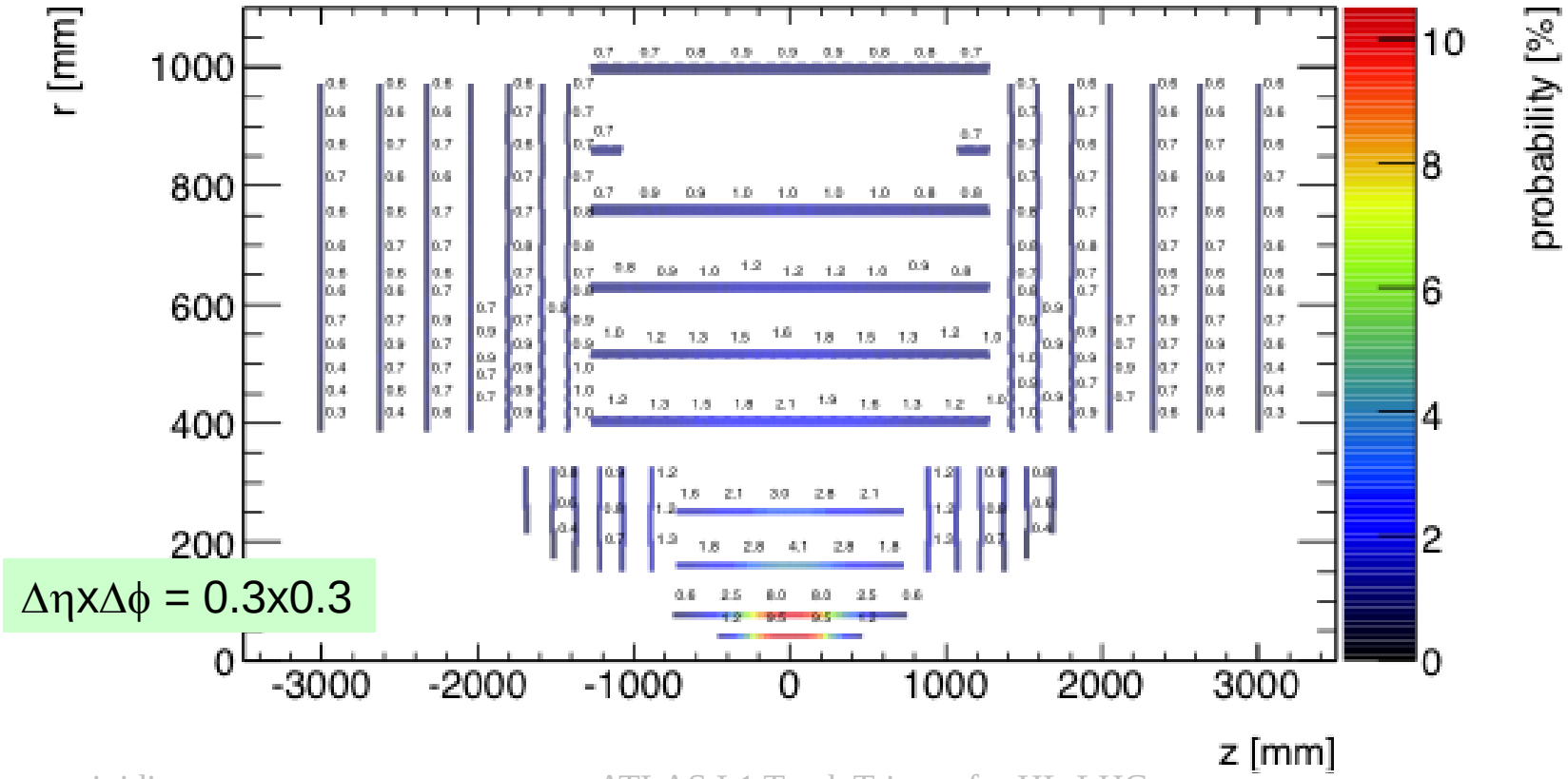
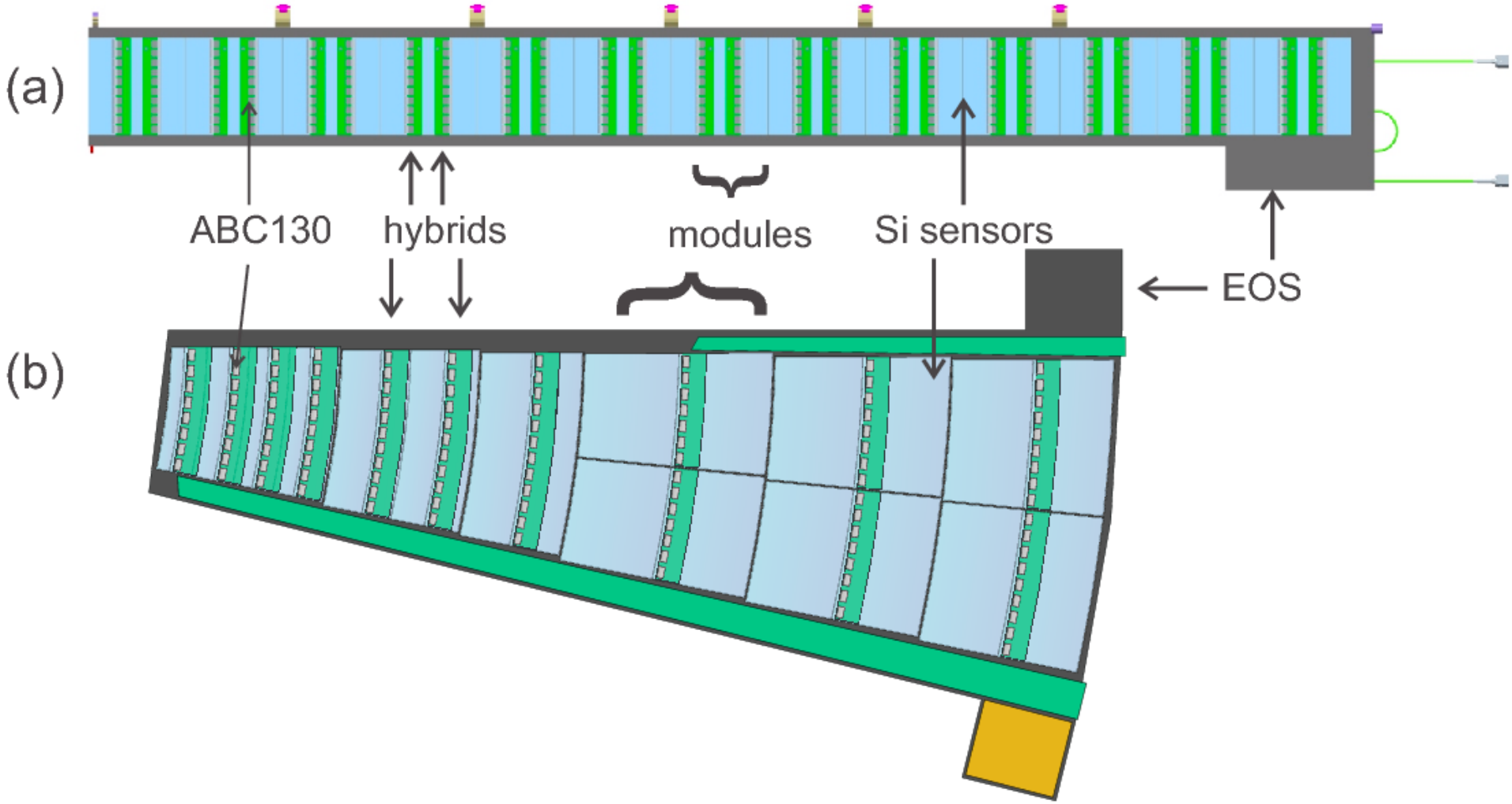


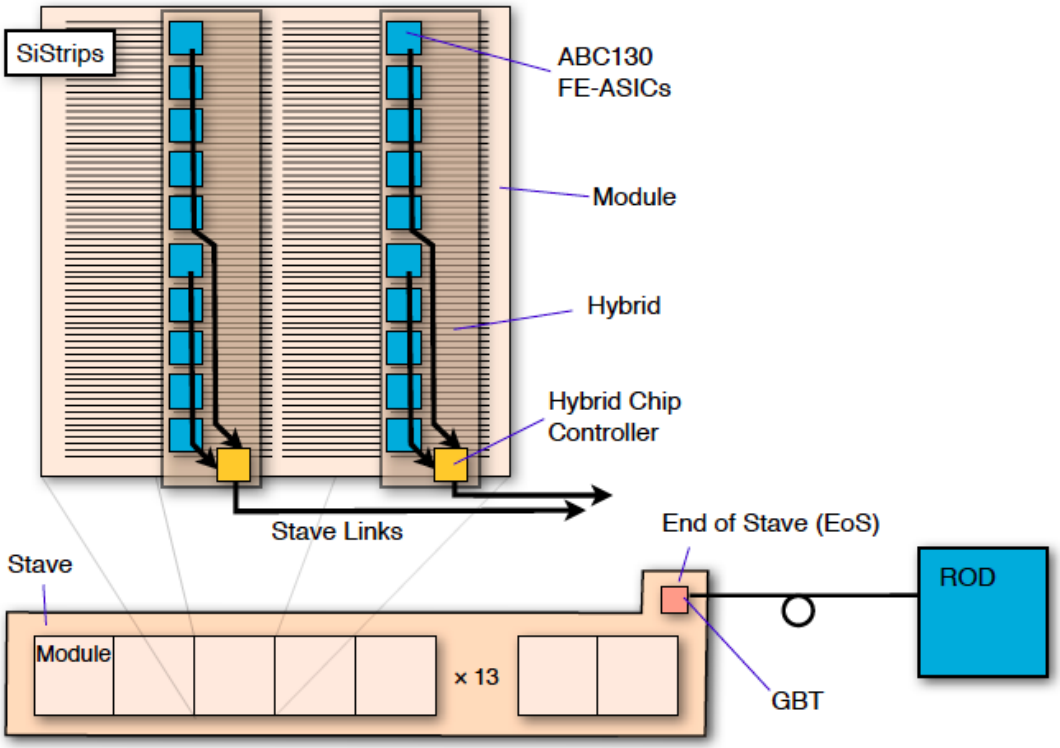
Strips: barrel and endcap structures



Module readout

- R3(/L1) Data packets (~60bits, with 4(/3) clusters) are formed in each ABC130 and propagated through the daisy chain of chips to the HCC

- Dedicated lines from each HCC to EOS/GBT (default 160Mbps, considering 320Mbps)



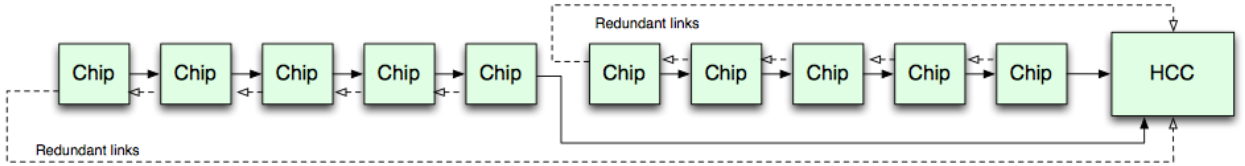
Latency constraints/targets

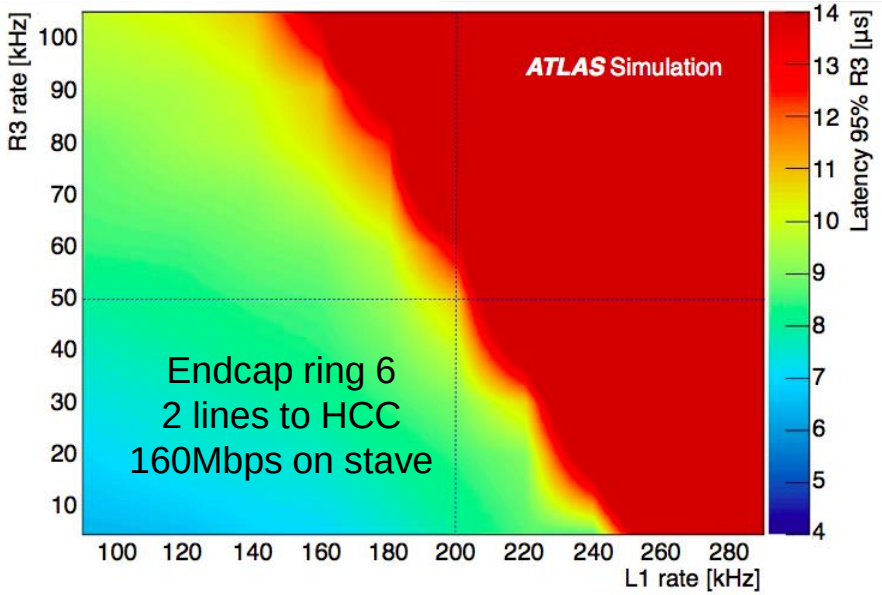
- ~24μs from L0A to L1A:
  - ~6μs for regional (R3) data readout
  - ~12-15μs for L1Track pattern recognition
  - ~3-6μs for cable times and Global L1 processing and decision

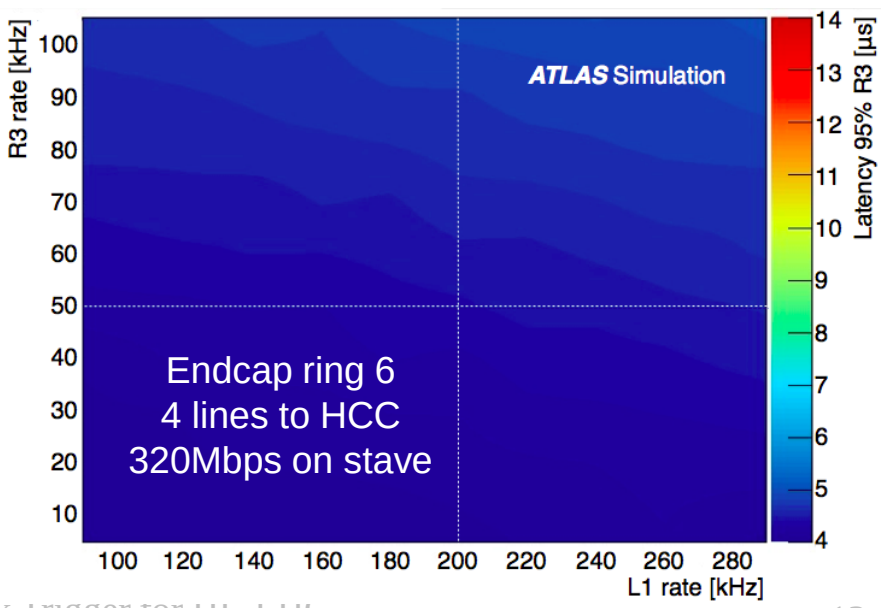
- Discrete Event Simulation framework to study R3 data latency
  - Full modelling of on-detector readout: from arrival of R3 or L1A signal at front-ends to data packets leaving the HCC
    - No queuing after that point

Latency results

- After R3 data are prioritised over L1 data at the HCC, latency target achieved in barrel
- More challenging in endcaps, due to longer daisy chains and higher occupancy
  - Requires 4 lines from FEs to HCC and 320Mbps lines on stave





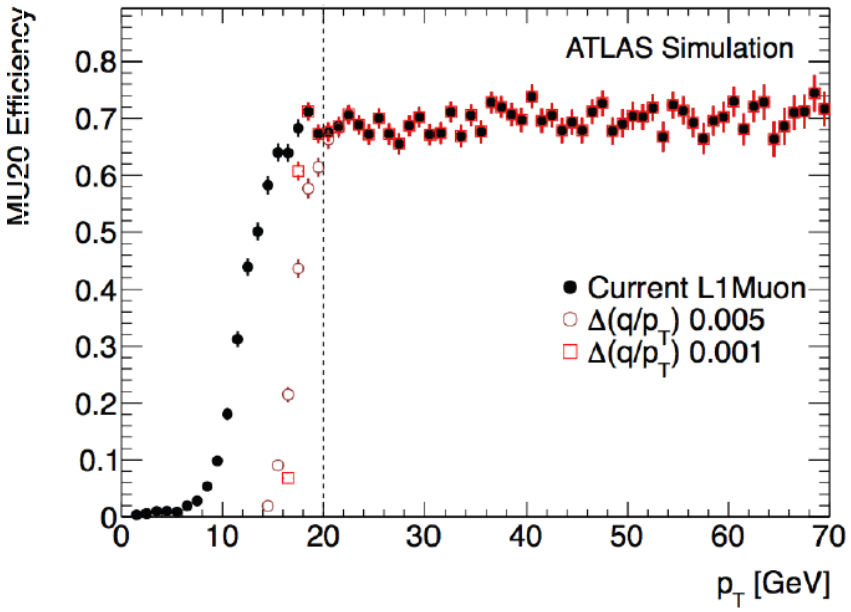


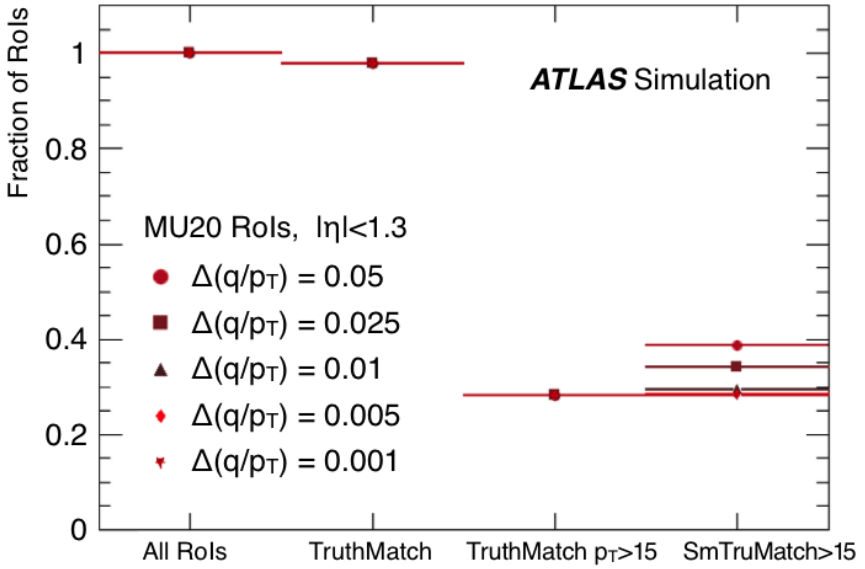
L1Track performance requirements

- Emphasis on high signal efficiency
  - Target signal efficiency = ~95% or above
- No need for very high rate reduction to go from 1MHz to a few hundred kHz
  - Target background rejection = ~5
- Next few slides show performance results using MC true charged particles or offline reconstructed tracks, with some smearing to emulate the expected resolution of L1Track

Muon performance

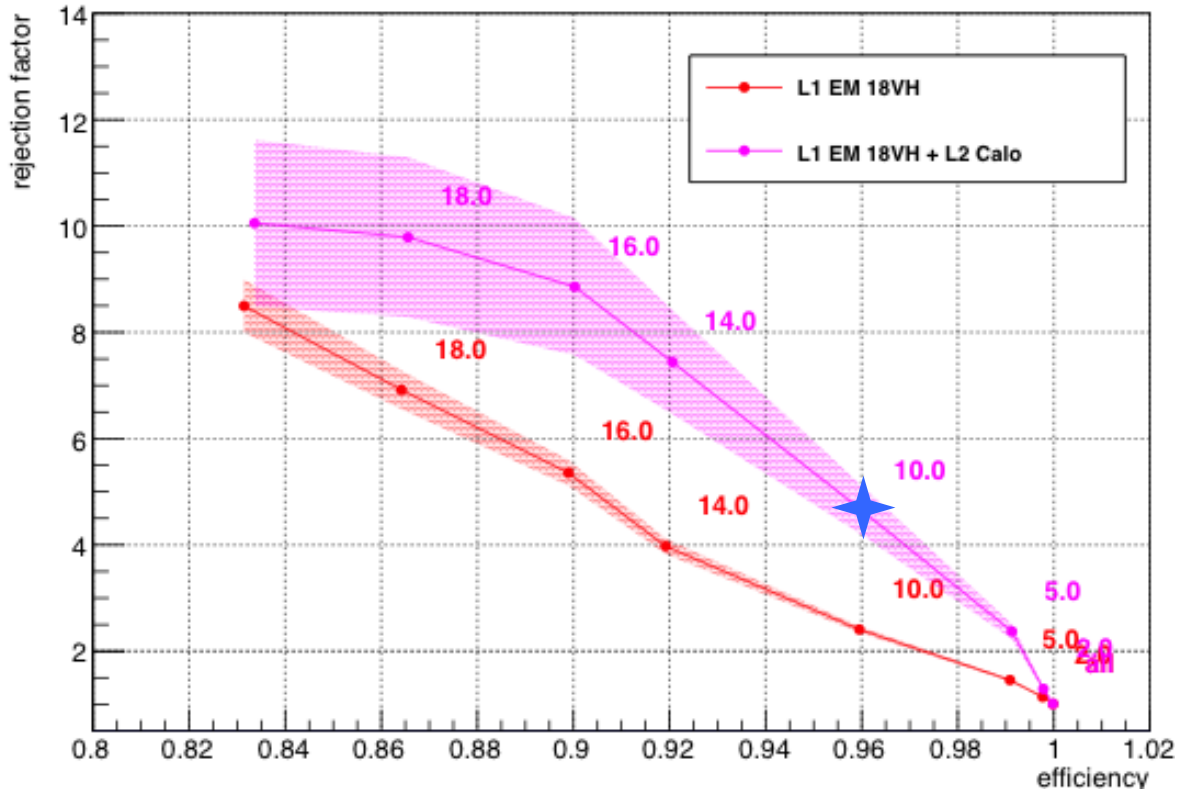
- Majority of L1_MU20 triggers are from real, low-pT muons
- L1Track tracks sharpen the L1Muon thresholds
- Factor ~4 reduction for L1_MU20 RoIs from real muons, more rejection for fake RoIs





Electron performance

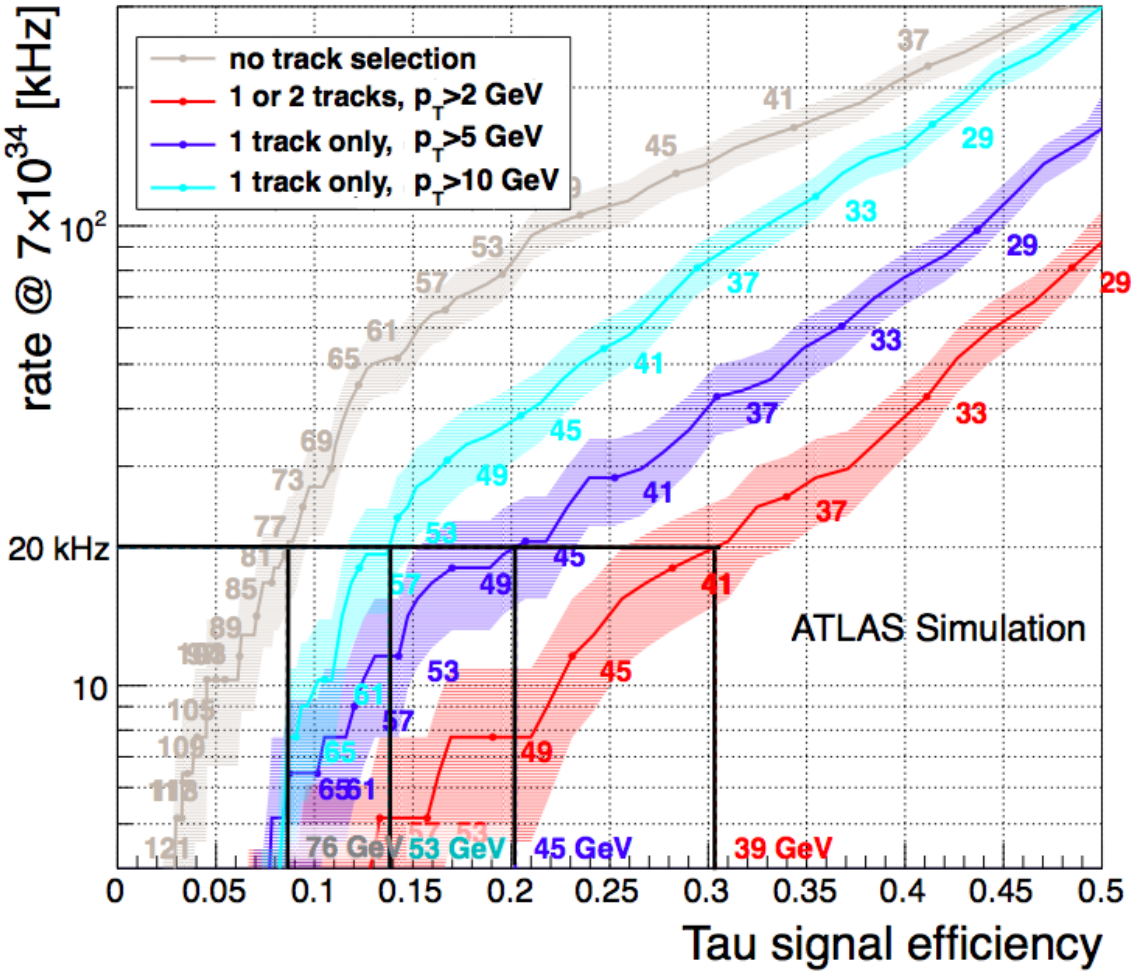
- Using offline reconstructed tracks in events with 3e34 pile-up
- For 96% signal (W→eν) efficiency, rejection factor ~5 when matching a p_T>10GeV track to the Run-1 L2Calo cluster
  - Run 1 L2Calo emulating L1Calo at HL-LHC
- Minimal impact from track smearing (emulate expected L1Track resolution)



Tau performance

Signal: single-prong hadronic taus with pT>20GeV from $H \rightarrow \tau\tau$ (m_H=120GeV)

Used offline tracks, smeared to emulate L1Track performance



Pattern recognition studies

- Preliminary results with “FTK-style” of pattern recognition
- Pattern banks generated using O(100M) muons in a small region of the detector:
  - η: [0.1,0.3]; ϕ: [0.3,0.5]; p_T: [4,400]GeV; $|z_0|$<250mm; $|d_0|$<2mm
- Using only Strip layers
  - maximum 10 hits (layers) per track
- Efficiency studied with independent sample of muons
- Fake pattern rate investigated in min-bias events with pile-up
  - μ=160 (of inelastic min-bias collisions)

Results and preliminary conclusions

	5 layers	8 layers		10 layers	
SS width	4/5 (ε_μ>99%)	6/8 (ε_μ>99%)	7/8 (ε_μ~96%)	8/10 (ε_μ>99%)	9/10 (ε_μ~94%)
32	54 (2.3M)				
64	187 (0.7M)	198 (2.7M)	16 (2.7M)		
128	537 (0.2M)	669 (0.8M)	151 (0.8M)	255 (1.3M)	36 (1.3M)

- Signal inefficiencies due to gaps between wafers
  - Ongoing work in the ATLAS tracker community to halve the size of these gaps and correspondingly the above inefficiencies will be halved
- Pattern bank sizes (in red) look achievable in an upgraded version of the FTK AM chips
  - Size can be optimized further with the "variable SS width" approach
- Number of patterns to be propagated to the track fitting stage (in blue) also achievable
  - Most are fakes; to be dropped at track fitting stage

Work/ideas in progress

- Rate of multi-jet triggers dominated by coincidences
  - Use L1Track to ensure jets are coming from the same z-position
- Use jets from the same z-position to define some kind of jet-based missing E_T, to mitigate pile-up effects
- Use Pixel layers for electron triggers (before electrons brem and before photons convert) and/or for b-jets
- A lot more to do in terms of the pattern recognition and performance studies, the latency of the pattern recognition hardware and the overall system design

Conclusions

- ATLAS constraints of L1A<~400kHz and L1 Latency<~30μs make the L0/L1 optimal/necessary and the use of RoI-based L1Track possible
  - L0/L1 approach with Regional Strip detector readout gives flexibility
  - Full Pixel readout at 1MHz may add flexibility, but not used yet
- Full discrete event simulation shows that R3 data latency of 6μs is achievable
- Studies with (smeared) MC charged particles or offline tracks indicate that rate reduction factors of ~5 are achievable for signal efficiencies ~95%
- First pattern recognition results, using Strips only, indicate that the FTK concept may work well also for L1Track at HL-LHC