



PS BGI fast digital link developments

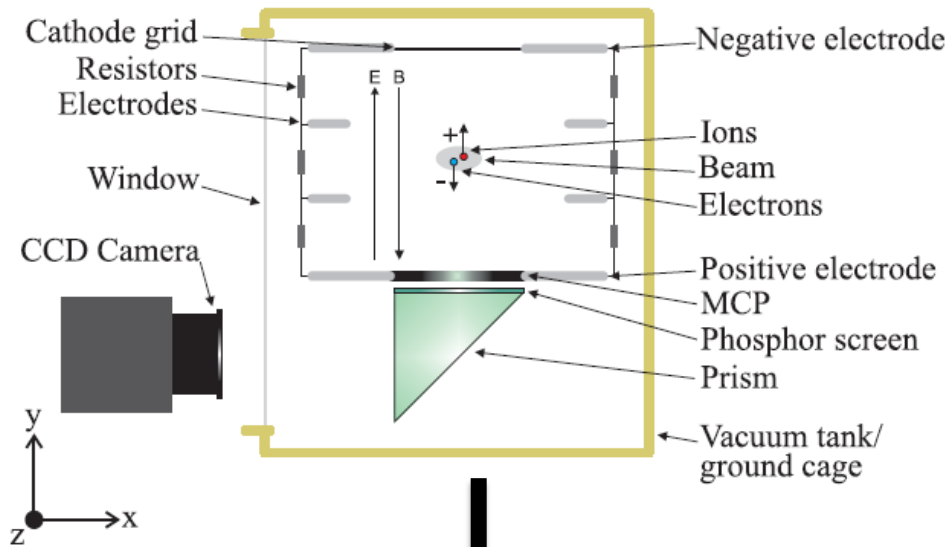
Oliver Keller, Mariusz Sapinski, Bernd Dehning

With input from: Simone Gilardoni, Dominique Bodart, Rende Steerenberg, Jose Ferreira, Xavi Llopart, Michael Champbell, Tuomas Poikela

BI technical board

July 10th, 2014

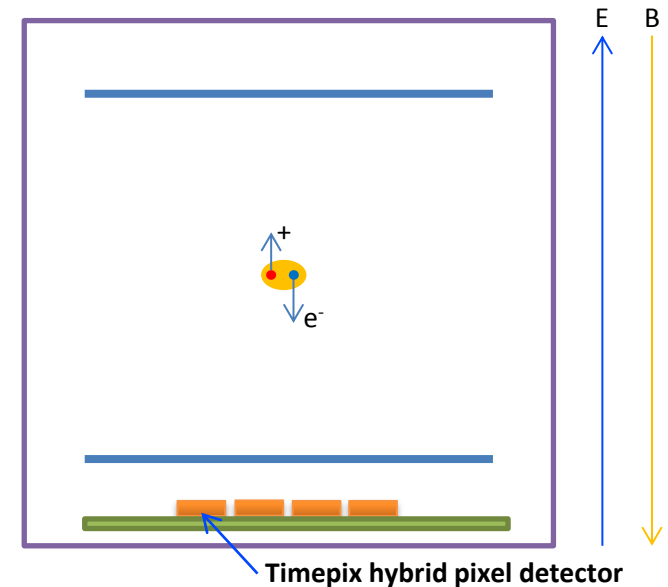
Overview of next gen. PS BGI readout



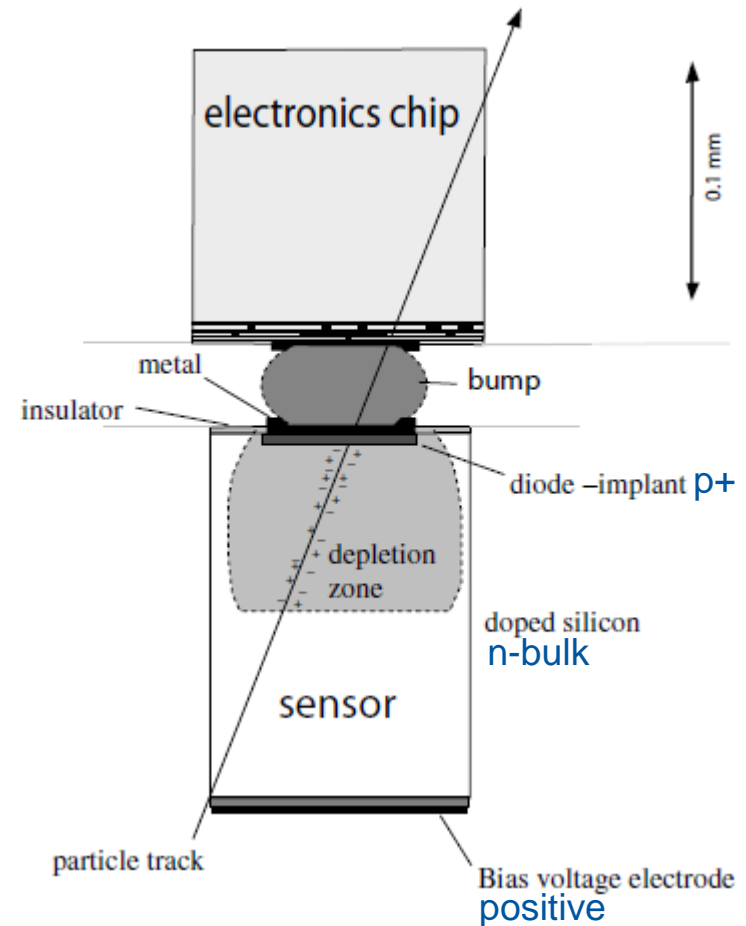
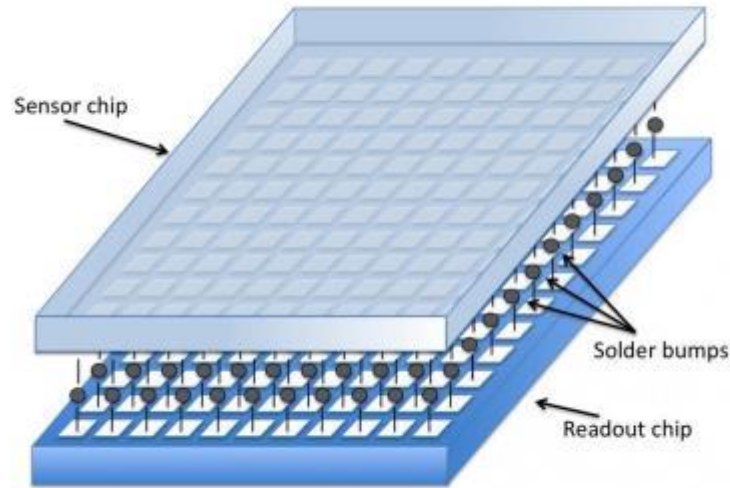
- Measure transverse beam size of LHC Beams bunch by bunch @40MHz



No Camera
No Phosphor screen
No MCPs

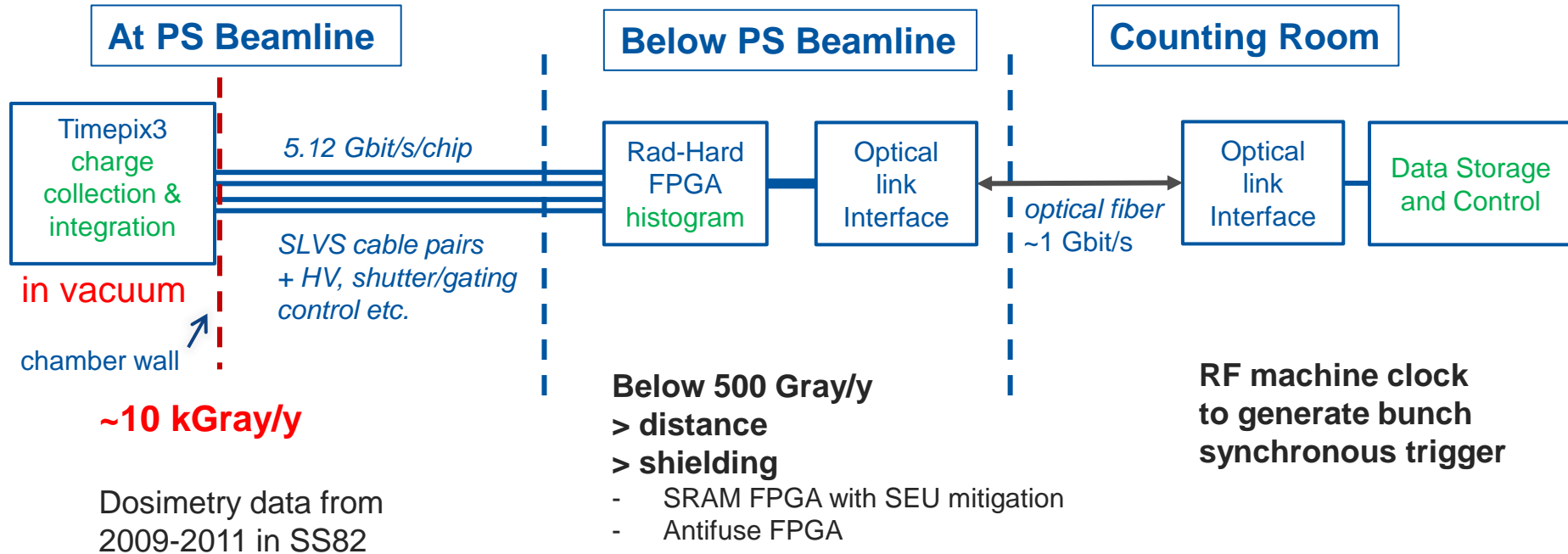


Hybrid Pixel Detector



- Pixelated Si sensor bump bonded on digital readout chip
- Small pixels: low capacitance, low noise, fast readout
- Rad-hard: several MGy (IBM 130 nm process)
- Timepix3: 2cm² (65k pixels) generate up to 5.12 Gbit/s hit data on 8 differential lines
=> **max. 80 Mhz/chip hit rate**

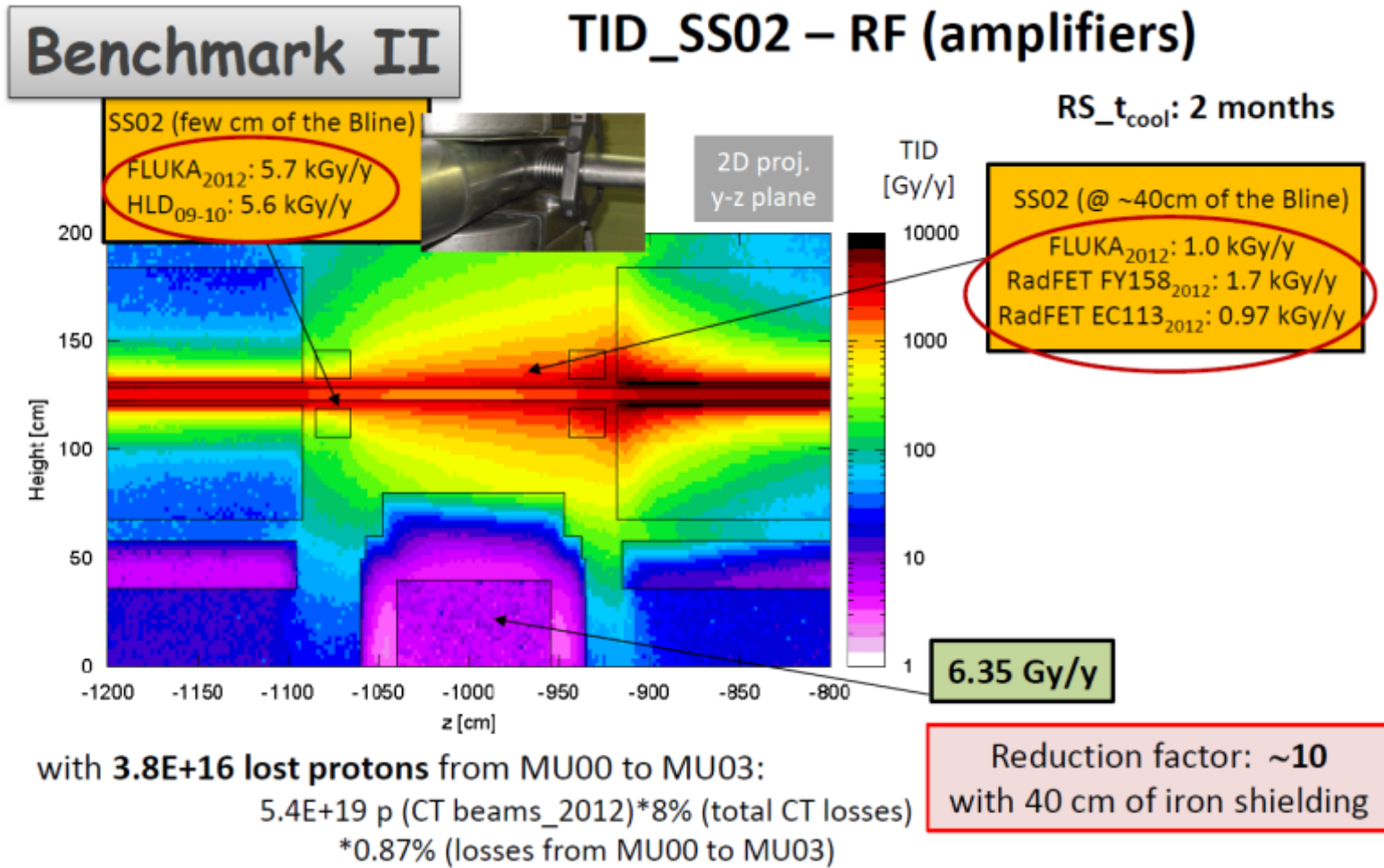
Topological Overview for PS BGI



FPGA next to the PS beam pipe

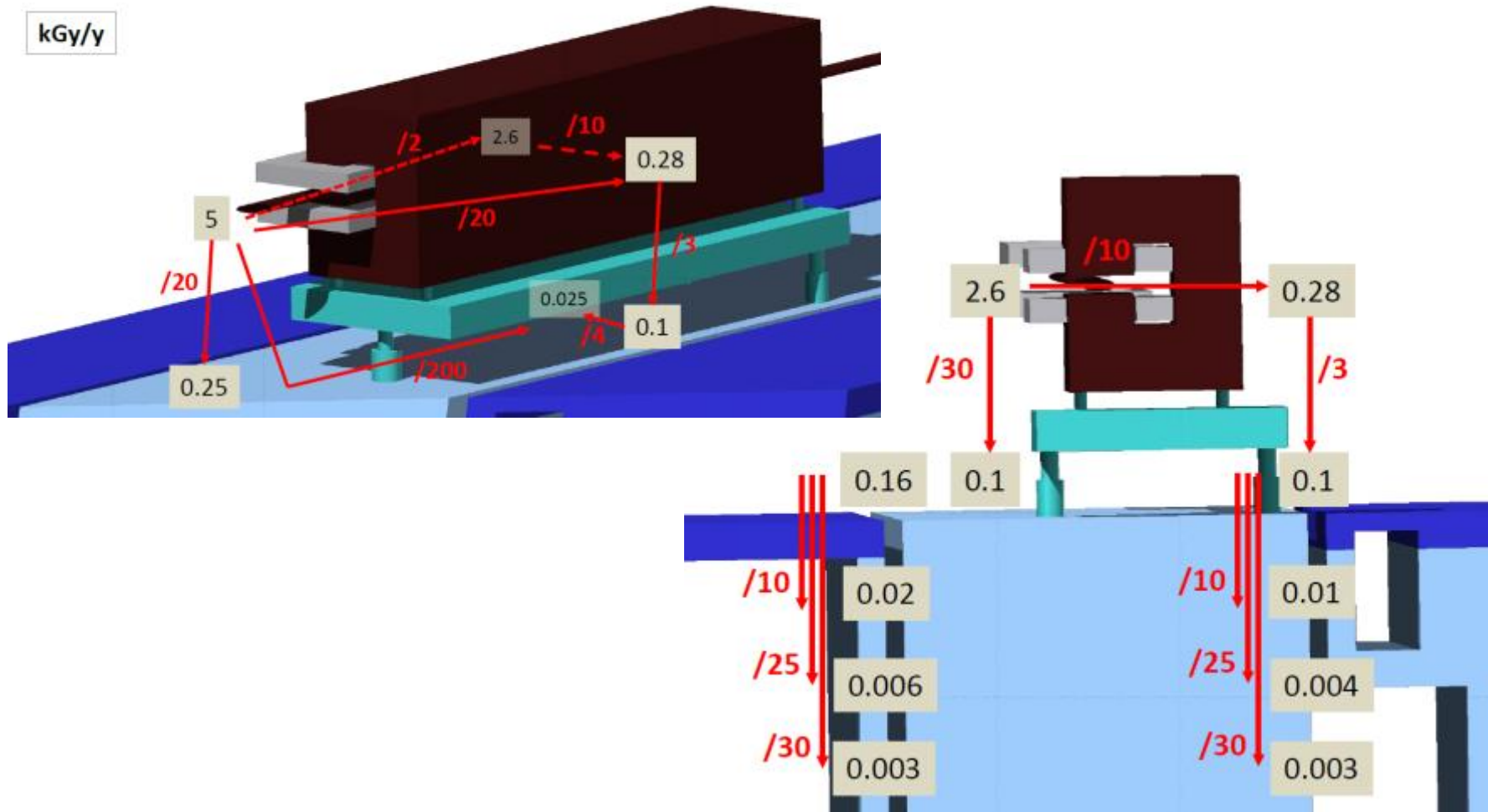
- GBT transceiver cannot handle data rates of 640 Mb/s from timepix3 (next generation LpGBT is only in planning stage)
- Digitized data from beam pipe on, data reduction on FPGA in the tunnel
- One Versatile VTRx optical duplex link towards counting room, probably using GBT protocol
- Feed-through of 9 SLVS 320 MHz DDR pairs plus HV, trigger etc. into beam pipe
- 2 m cable between Timepix 3 and FPGA already used in first chip tests
=> max. cable length limit to be tested
=> high quality, impedance matched, vacuum throughput connector

Simulation of shielding at @ SS02



Slide courtesy of João Pedro Saraiva, 2013

Distance gradient in PS @ SS77



Conclusions

- Continuous monitoring of beam emittance in PS can be achieved by BGI monitor with fast silicon pixel detector
- No existing BGI is measuring 25 ns beams bunch-by-bunch
- Proposed pixel detector readout chip will withstand radiation
- Readout FPGA is fragile and needs testing & careful implementation to mitigate radiation effects
- Staged development: start with one pixel detector, foresee more; next interesting pixel detector candidate: Velopix

Additional resources:

- TWiki:

<https://twiki.cern.ch/twiki/bin/viewauth/PSBGI/WebHome>

- Presentation at Be/Bi tech. board meeting on May 15^h, 2014
- Presentation at LIU PS meeting on February 11th, 2014
- Presentation at BI-LIU review on October 3rd, 2013

BACKUP SLIDES

Specs vs. fulfilment

Particle scheme	p (std, 50ns)	p (std, 25ns)	Pb54+ Inj.	Pb54+ Extr.
Energy [GeV]	1.4	25	15.02	1227
No of bunches/ revolution time	6 (in ~2.1 us)	72 (in 2.1 us)	2 (in 5.63 us)	2 (in 2.12 us)
Electrons per bunch/length	190 (in 180 ns)	26 (in 4 ns)	610 (in 200 ns)	120 (in 4 ns)
Readout delay per chip	2.3 us	3(+) * 2.1 us	< 5.63 us	1.5 us
Profile data output	One bunch every 2 nd turn	Every 3 turns or gas inj.	One bunch every turn	One bunch every turn
Pixel hit rate per bunch (avg.)	20 kHz	130 kHz	49.0 kHz	1.6 MHz
Timepix 3 mode	ToT & ToA	ToA only + pile-up counter, <u>gas injection for burst mode</u> (or parallel chips)	Counting & iTOT, gating in bunch or reduce detection efficiency	ToA only, gating in bunch or reduce detection efficiency

Post-LS1 LHC beams in PS – WS damage?

Beam	N (10^{11})	$\epsilon_{x,y}$ [μm]	B_l [ns]	$\sigma_{y,x}$ [mm]	N_{bunch}	$n_{\text{ch}} = \frac{N N_{\text{bunch}} d}{v t \sigma_y}$
Standard 50 ns inj	11.9	1.48	180	2.7/ 3.4	6	$1.4 \cdot 10^{12}$
extraction	1.89	1.55	3	0.81/ 3.7	36	$4.5 \cdot 10^{12}$
Standard 25 ns inj	16.84	2.25	180	3.3/ 3.9	6	$1.6 \cdot 10^{12}$
extraction	1.33	2.36	3	1.0/ 3.7	72	$5.1 \cdot 10^{12}$
LIU 50 ns inj	18.95	1.69	205	2.55/ 3.5	6	$2.4 \cdot 10^{12}$
extraction	3.0	1.77	3	0.86/ 3.7	36	$6.6 \cdot 10^{12}$
LIU 25 ns inj	28.07	1.63	205	2.5/ 4.4	3	$3.6 \cdot 10^{12}$
extraction	2.22	1.71	3	0.84/ 3.7	72	$1.0 \cdot 10^{13}$

From SPS experiments the safe value for wire is about **$5 \cdot 10^{12}$ charges/mm.**
(done for 30 μm SPS/LHC wire, no experience with multi-filament wire).

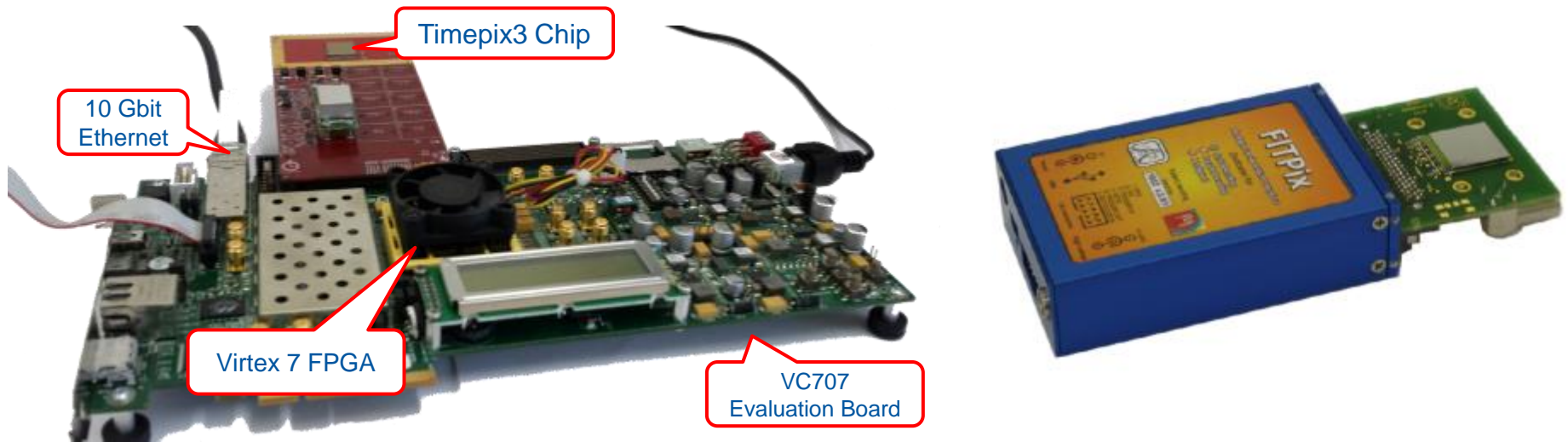
Detailed pixel detector comparison - Geometries and readout limits

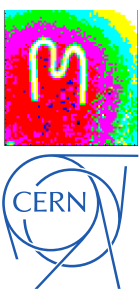
Chip	design TID [Mrad]	Pixel size [um ²]	Area [mm ²]	max. hit rate [MHz/cm ²]	max. readout rate [MHz/chip]	Data per pixel	Trigger	Output bandwidth (incl. line encoding)	Application	Available
FE-I4	300	50x250	20x19 3.8 cm ²	400	0.2	ToT	external	30 bits via 1 LVDS @ 160Mb/s	ATLAS	2012
ToPix	10	100x100	11.6x11.4 1.32cm ²	6	6.1	ToT	internal	50 bits @ 400Mbit/s (DDR, GBTx compatible)	PANDA experiment, GSI	2012
TDCpix	>10	300x300	12 x 13.5 1.62cm ²	80*	130*	ToT, ToA	internal	60 bits via 4 CML @ 3.2 Gb/s (optical link compatible)	NA62 experiment, Gigatracker	2013
Timepix 3	400	55x55	14 x 14 2cm ²	40	80	ToT, ToA, Counting & iToT	internal	60 bits via 8 SLVS @ 640 Mb/s (DDR)	particle tracking, HEP, Medical etc.	2014
Velopix	400	55x55	14 x 14 2cm ²	400	800	ToA	internal	~18 Gbit/s	LHCb VELO detector	2016?

- All based on IBM 130 nm manufacturing process
- no rad-hard optical transceiver chip for >320 MB/s
- GBTx successor: LpGBT only in planning phase
=> currently FPGA needed to read out Timepix3

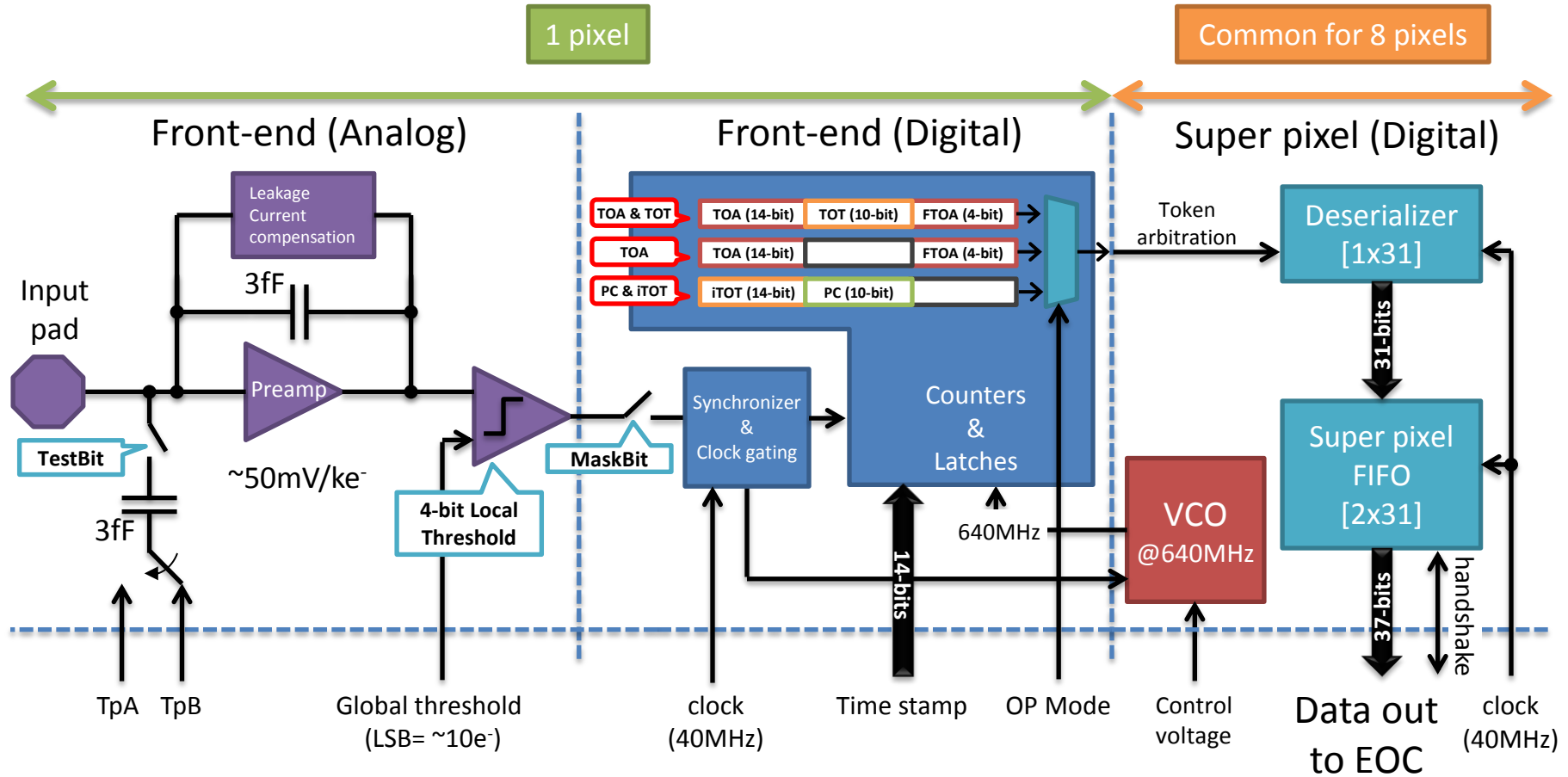
Timepix development HW & SW

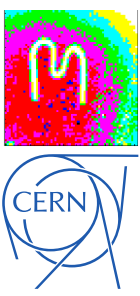
- SPIDR readout platform, based on Xilinx Virtex 7 board
- SVN code repository developed by NIKHEF, several users at CERN
- Up to four Timepix 3 chips with 10 Gbit/s Ethernet connection to PC
- PC GUI application development in progress
- CERN chipboards with 300 μm Si on Timepix 3 just arrived
- Sensor qualification with 100 μm Si on Timepix 1, FITpix USB module from Widepix



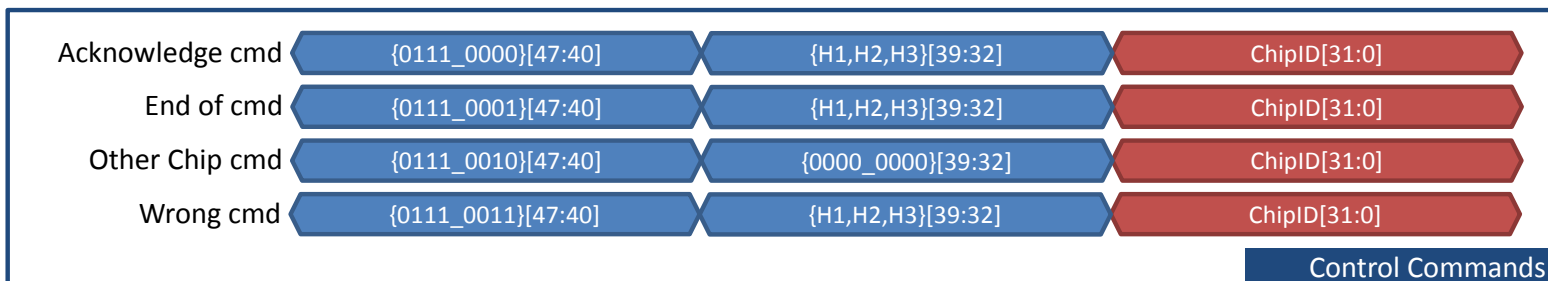
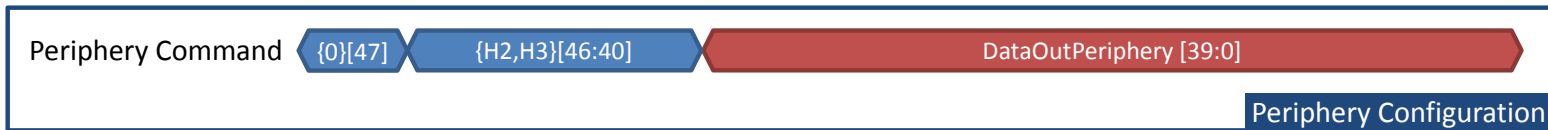
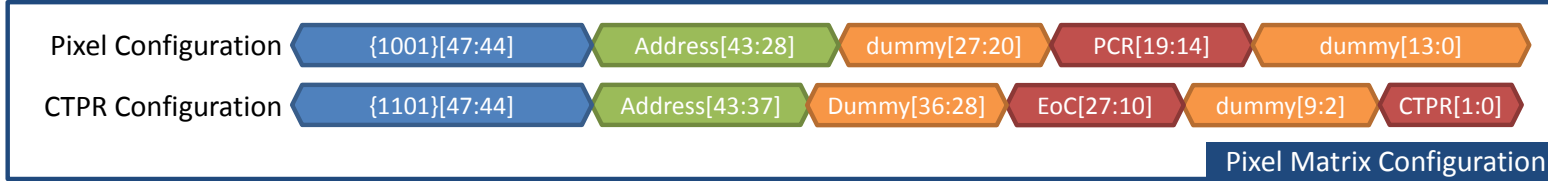
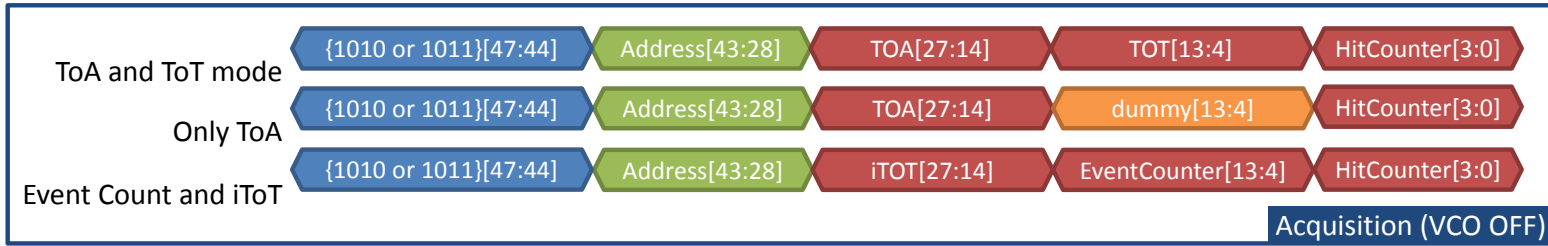
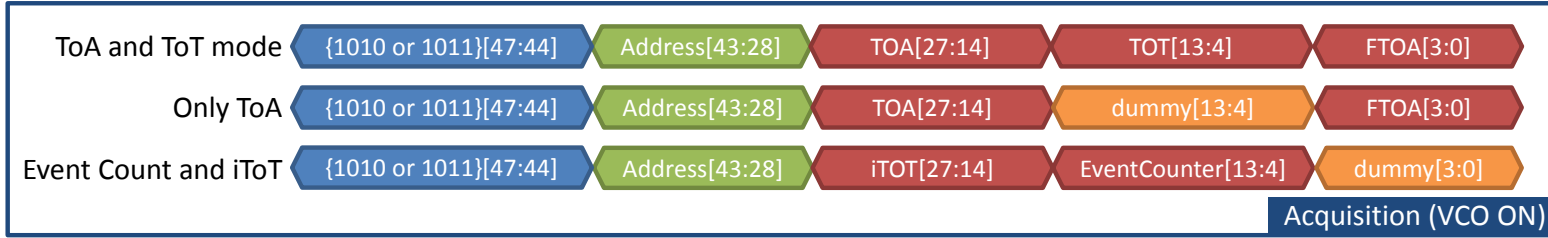


Timepix3 Pixel Schematic





Data output packet types



Workshop on FPGAs for High-Energy Physics



FPGA Options Summary

	TID limit	Configuration Tolerant to SEUs	SEUs in functional blocks	Notes
MicroSemi ProAsic Flash	20-40 krad (very dependent on dose rate & refresh conditions/annealing)	Yes	Use TMR, embedded blocks should be tested (eg PLLs)	Already tested
MicroSemi SmartFusion2 Flash	?	Yes	Use TMR, embedded blocks should be tested (eg PLLs)	Very new and not tested much
AntiFuse	? (but higher than Flash. PINT was tested good to 150 krad)	Yes	Use TMR, embedded blocks should be tested (eg PLLs)	One shot only!
SRAM FPGA	100s krad	No: needs scrubbing	Use TMR, embedded blocks should be tested (eg PLLs)	Needs careful testing & scrubbing implementation

FPGAs in LHCb,
 Thomas O'Bannon
<http://indico.cern.ch/event/300532/timetable>

Mar 21, 2014

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Broken EGA from LHC BGI

- EGAs have same operating conditions as MCPs

