TTC
Commissioning Plan
April 2008
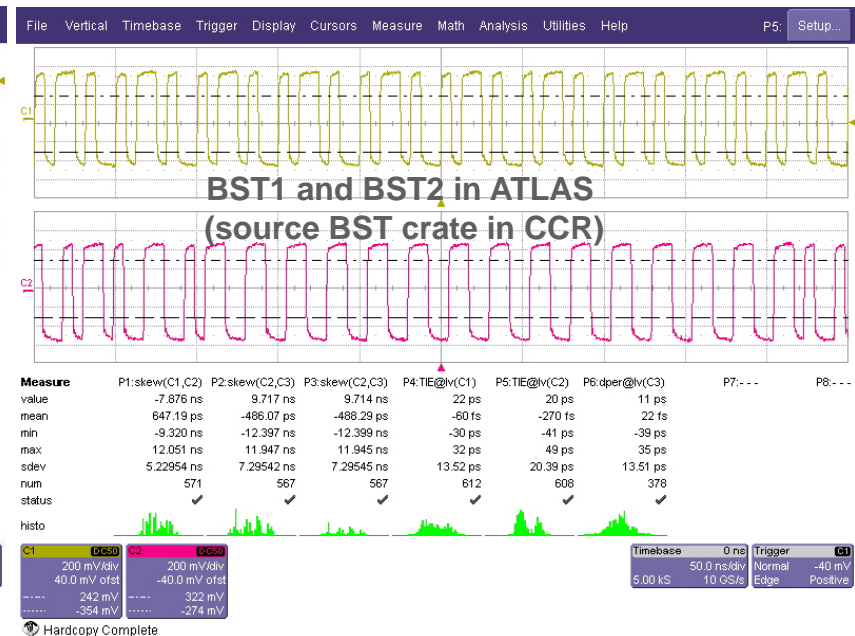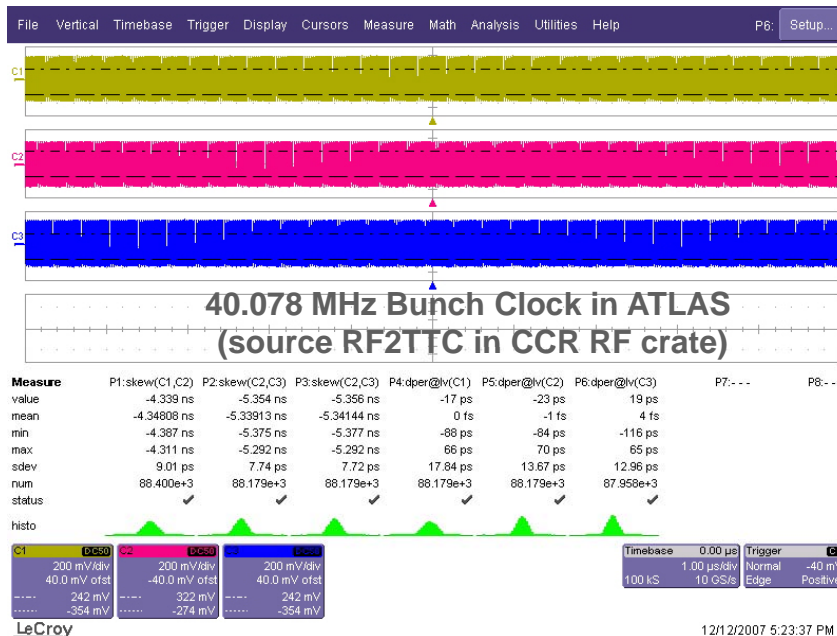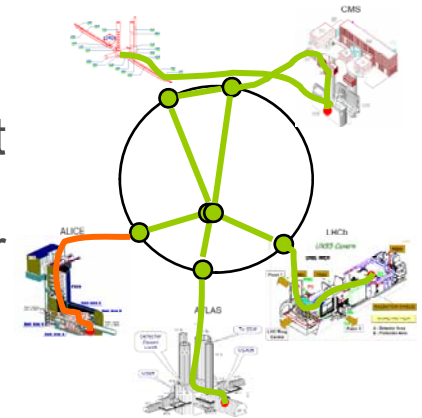
- Status
- What's next?

STATUS [Equipment & Network - 1]

- **Equipment distributed**
  - o TTC VME crates
  - o Crate controllers
  - o Optical receivers (produced by AB/RF and tested by PH/ESE)
  - o RF2TTC (produced and tested by PH/ESE)
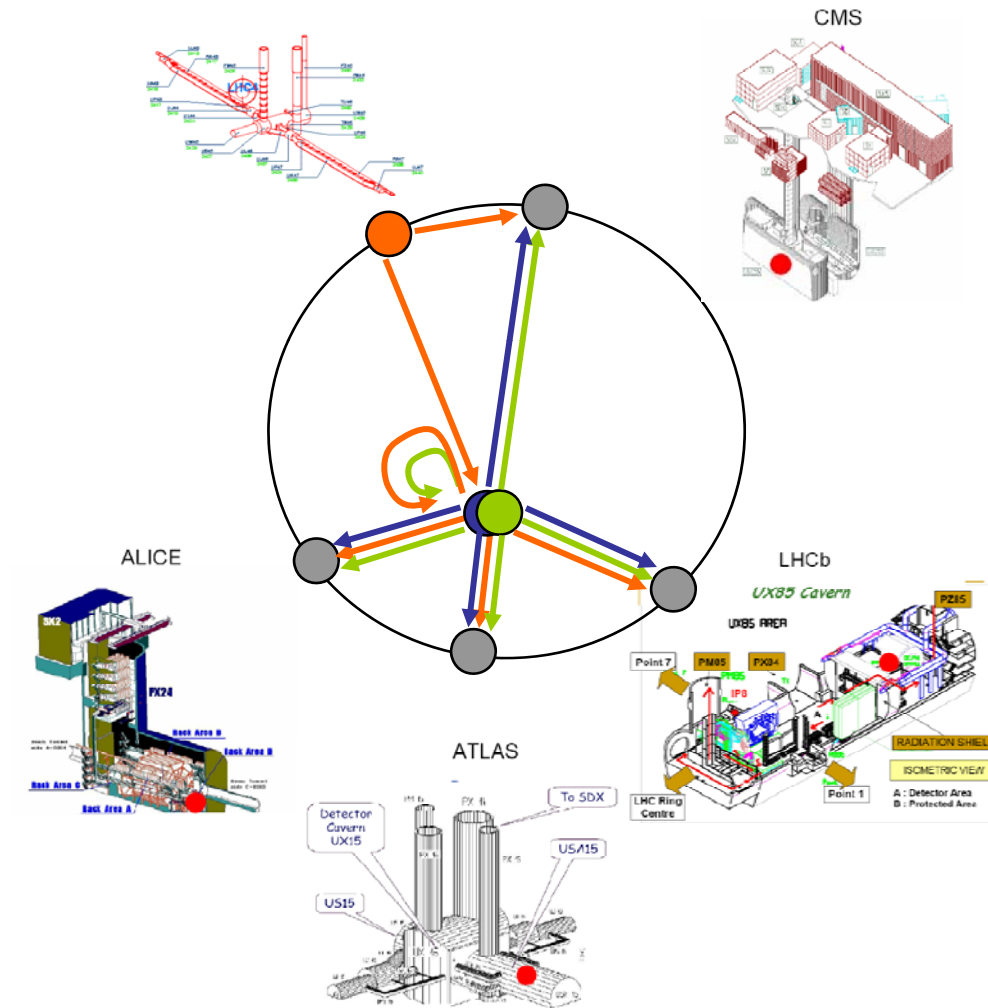 - o TTC fanouts (produced and tested by PH/ESE)

- **Optical Network Quality (almost) fully tested in December**
  - o Jitter and optical power loss tested at reception point for ATLAS, CMS and LHCb with fake Bunch Clocks.
    - Optical signal level:-12dBm for TTC signals, -6dBm for BST
    - Cycle to cycle jitter of received clocks ~15ps
  - o Alice (from SR2 to UX25) installed (and tested) by TS/EL, but not tested by us.

40.078 MHz Bunch Clock in ATLAS (source RF2TTC in CCR RF crate)

Measure	P1:skew(C1,C2)	P2:skew(C2,C3)	P3:skew(C2,C3)	P4:dper@lv(C1)	P5:dper@lv(C2)	P6:dper@lv(C3)	P7:- - -	P8:- - -
value	-4.339 ns	-5.354 ns	-5.356 ns	-17 ps	-23 ps	19 ps		
mean	-4.34808 ns	-5.33913 ns	-5.34144 ns	0 fs	-1 fs	4 fs		
min	-4.387 ns	-5.375 ns	-5.377 ns	-88 ps	-84 ps	-116 ps		
max	-4.311 ns	-5.292 ns	-5.292 ns	66 ps	70 ps	65 ps		
sdev	9.01 ps	7.74 ps	7.72 ps	17.84 ps	13.67 ps	12.96 ps		
num	88.400e+3	88.179e+3	88.179e+3	88.179e+3	88.179e+3	87.958e+3		
status	✓	✓	✓	✓	✓	✓		
histo								

BST1 and BST2 in ATLAS (source BST crate in CCR)

Measure	P1:skew(C1,C2)	P2:skew(C2,C3)	P3:skew(C2,C3)	P4:TIE@lv(C1)	P5:TIE@lv(C2)	P6:dper@lv(C3)	P7:- - -	P8:- - -
value	-7.876 ns	9.717 ns	9.714 ns	22 ps	20 ps	11 ps		
mean	647.19 ps	-486.07 ps	-488.29 ps	-60 fs	-270 fs	22 fs		
min	-9.320 ns	-12.397 ns	-12.399 ns	-30 ps	-41 ps	-39 ps		
max	12.051 ns	11.947 ns	11.945 ns	32 ps	49 ps	35 ps		
sdev	5.22954 ns	7.29542 ns	7.29545 ns	13.52 ps	20.39 ps	13.51 ps		
num	571	567	567	612	608	378		
status	✓	✓	✓	✓	✓	✓		
histo								

12/12/2007 5:23:37 PM   Hardcopy Complete

BST

TTC (3BC & 2Frev)

RD12

CMS

ALICE

LHCb

ATLAS

- **BST signals:**
  - o Ready since November
  - o 2 BST signals (BST1 and BST2) transmitting BST telegrams.
  - o Not yet synchronized with BC1 and BC2
  - o Tested in December at all experiments (except ALICE)
- **RD12 signal:**
  - o Encoded BCref and Frev using the previous rd12 TTC system
  - o Hardware ready (needs just to be configured)
- **RF signals (next slide)**

- ## RF Signals:
  - o RF modules installed at SR4 2 weeks ago
  - o (Fake) Signals transmitted since Monday 21st April
    - 2 synchronized Bunch Clocks on BC1 and BC2 (40.08MHz for the moment), with their respective Revolution Frequencies (BCx/3564) as 5ns pulses.
    - 1 separate Bunch Clock as a Reference BC at 40.0799MHz.
  - o Tested on the CCR TTC support rack last week
    - Jitter is as expected
      - – BC: Cycle-to-cycle jitter <15ps rms
      - – Frev (orbit): period jitter ~= 23ps rms, width jitter <50 ps rms
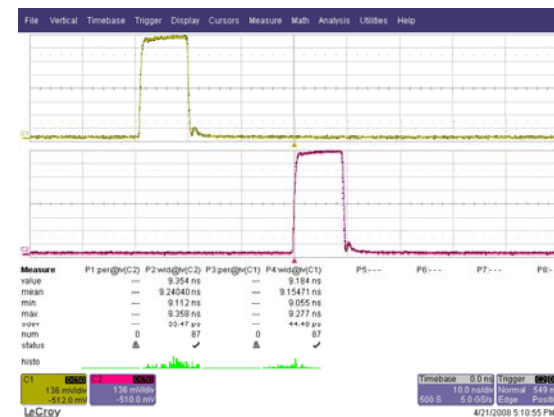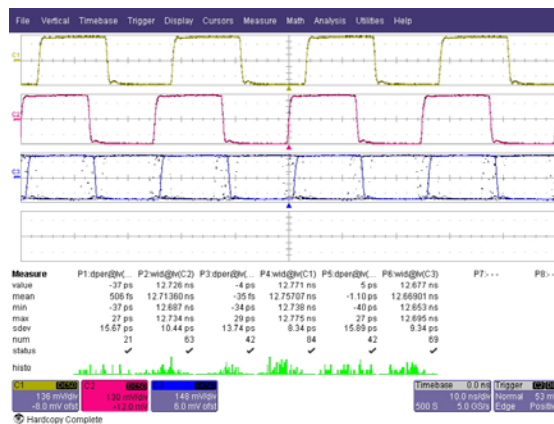
- **RF Signals:**
  - First tests made at CMS last week with remote status monitoring
    - Example:

RFRXD "RFRX Beam 2" (Slot=56, lid=51)

RFRXD
http://vmepcs2b16-05.cms:1972
urn:xdaq-application:lid=51

[RFRXD Control] AutoRefresh

RFRXD Control (*RFRX Beam 2*)

WARNING: Errors/warnings detected!
WARNING: No signal detected on channel 1

RFRXD State Machine	**Ready**

		Channel 1	Channel 2	Channel 3
EDA ID	0x1382 (4994) (OK)			
CERN Board ID	0x016c (364) (OK)			
Firmware version	20080327			
DAC value		0x30 (48)	0x30 (48)	0x30 (48)
Frequency raw value		0xffffffff (4294967295)	0x000002bf (703)	0x00263561 (2504033)
Frequency MHz		6.55651e-06 (0..6.55651e-06) MHz	40.0569 (40.0284..40.0854) MHz	0.0112459 (0.0112459..0.0112459) MHz
signal present		NO	yes	yes
		new DAC value (0..255): 48 [Set] Set to pulse value Set to clock value	new DAC value (0..255): 48 [Set] Set to pulse value Set to clock value	new DAC value (0..255): 48 [Set] Set to pulse value Set to clock value

General Info
Software: Version 6.06.02 (Released: 2008-04-03 10:32:17, Built: 2008-04-23 08:08:35+0000)
RFRXDLocation: 56 (Actual slot = 56)

RFRXD Library Version 6.06.02 (Released: 2008-04-03 10:32:17, Built: 2008-04-23 08:08:35+0000);
Authors: Tim Christiansen, Emlyn Corrin and André Holzner
RFRXD Manual XDAQ Web site

- Status
- What's next?

- **Signal quality test:**
  - o Spend half a day with each experiment to
    - Check the final optical power
    - Configure the receiver to optimize the quality of the received signals
    - Measure the signals quality
    - Identify the signals one from each other (3BCs, 2 Orbits)

- **Practice on the TTC system:**
  - o Once the BST message definition is stable, set-up with AB/BI a sequence of "typical" consecutive machine modes being transmitted over the BST to allow the experiments to practice the clock switching according to the machine state

- **Firmware update following remarks and suggestions**
  - o In July

- **Prepare the regular publication of the signal status on DIP:**
  - o Ex: CMS/RF_Rx/F40.B1 => "40.078MHz"

- **TTC support organisation:**
  - o List of persons involved in RF piquet has been sent to the Glimos of each experiments
    - They will receive this week the list of
      - – Safety Courses they have to follow (4A, 4b, 4C)
      - – specific access requests they have to do on EDH
  - o A visit of each point is being organized with the TTC responsible of each point and the persons involved in the piquet.
  - o The procedure is being defined now for an eventual intervention of the RF piquet on experimental sites. Documentation will be provided and the TTC site updated.
  - o During the summer, an oscilloscope with Ethernet access will be installed in the CCR TTC support rack to permanently analyze the quality of the signals.