UNIVERSITY OF LIVERPOOL

Comparison of the AC and DC coupled pixels sensors read out with FE-I4 electronics

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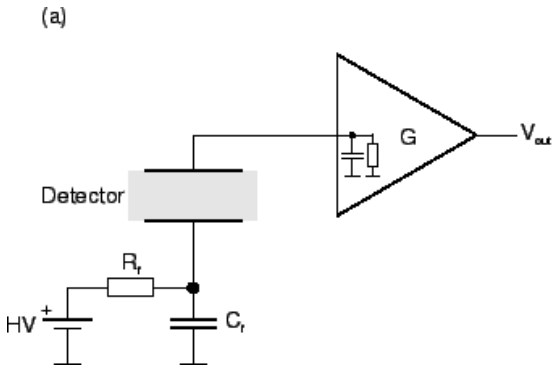
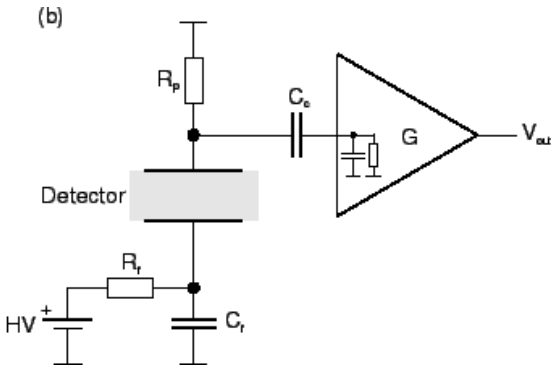
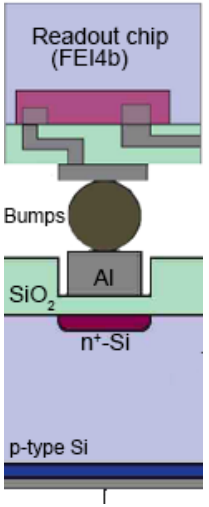
Motivation





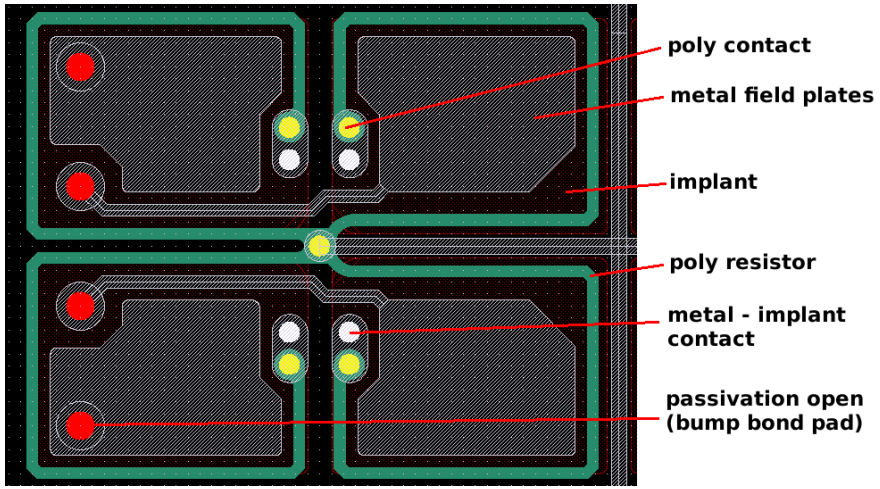


- High leakage current of DC coupled sensors is the source of shot noise in FE electronics. High amplifier currents distort signal shape and affect linearity and dynamic range of analogue circuits.
- AC coupling between implants and front-end is one possible solution to improve on these issues, especially after irradiation, as it blocks the leakage current from the detector to the amplifier.
- Integration of coupling capacitances is performed in standard planar process and is basically the same as for strip sensors, by depositing SiO_2 with a thickness of around 100 nm on top pixelated implants.

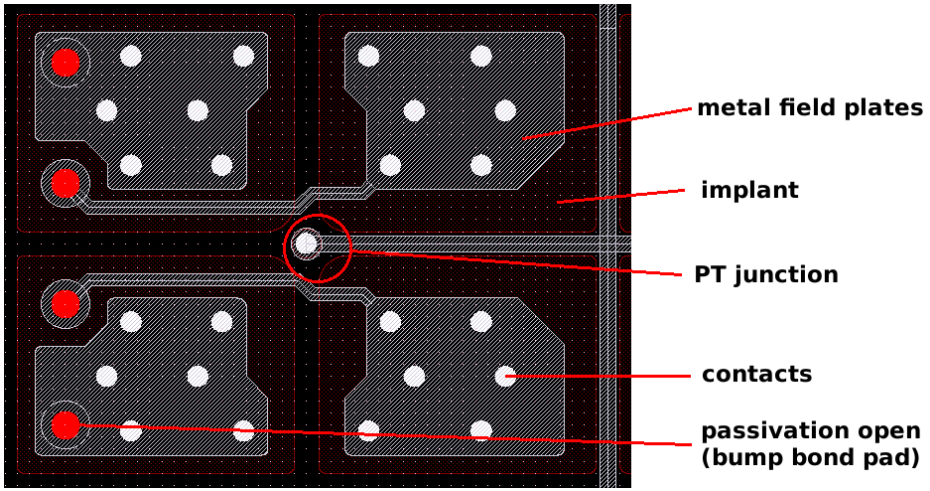
Production: CERN Pixel V – AC & DC coupled devices

- The bias current is shunted by resistors, either made of polycrystalline silicon or implemented as a PT junction.

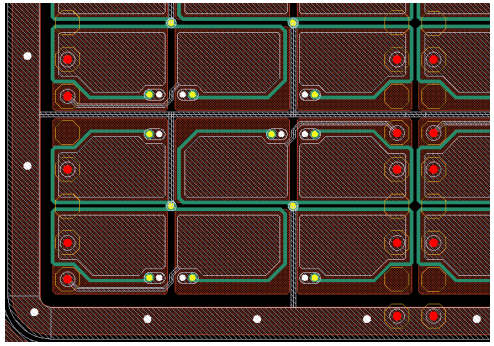
125x100 AC:



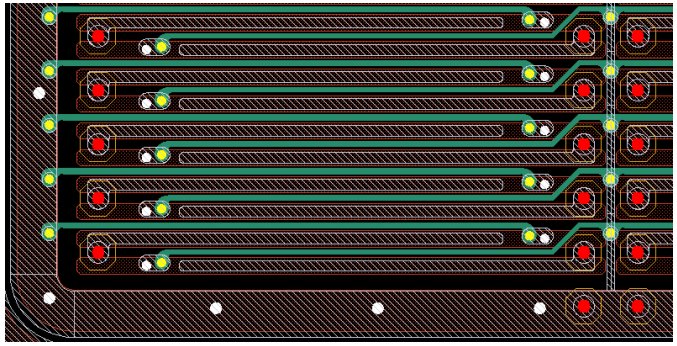
125x100 DC:



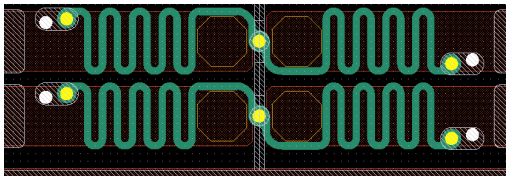
167x125 AC:



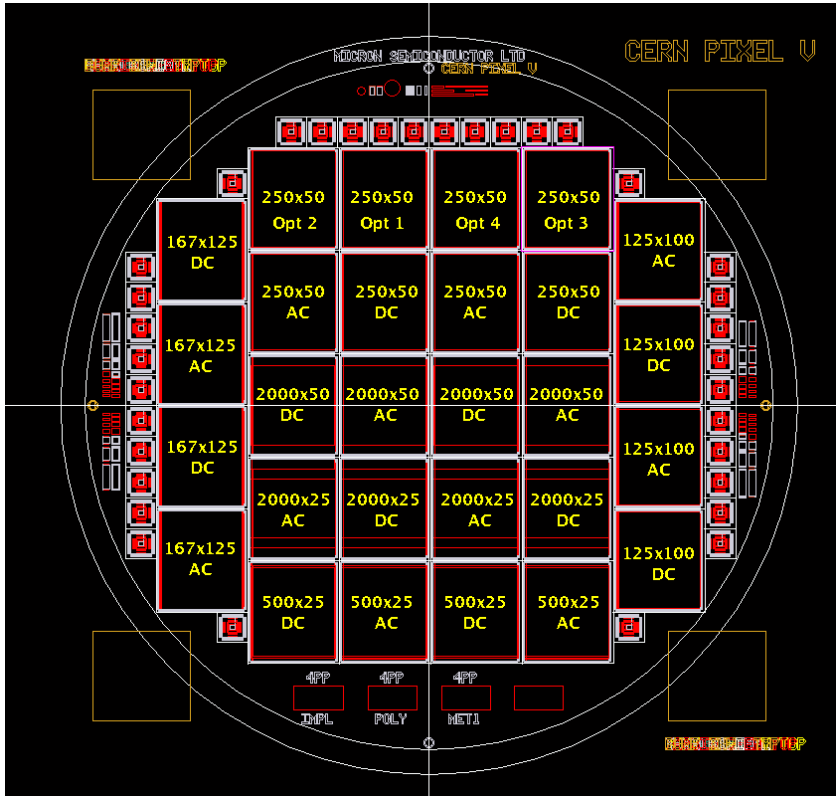
500x25 AC:



2000x50 (strixel) AC:



CERN Pixel V – 2873-25 (310um) AC wafer (10kΩ/cm)



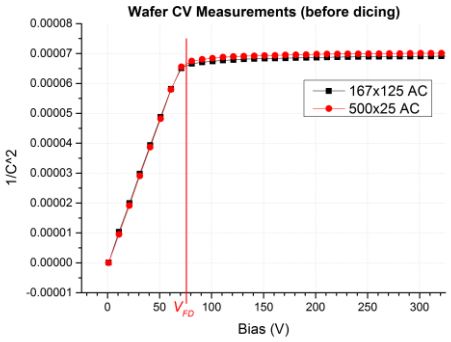
- Single FE-I4 chip compliant sensors with alternative pixel geometries

Segmentation:

125x100 µm (square)	26880 channels (100%)
167x125 µm (square)	16080 channels (60%)
250x50 µm (standard)	26880 channels (100%)
500x25 µm (elongated)	26880 channels (100%)
2000x25 µm (strixel)	6720 channels (25%)
2000x50 µm (strixel)	3660 channels (12.5%)

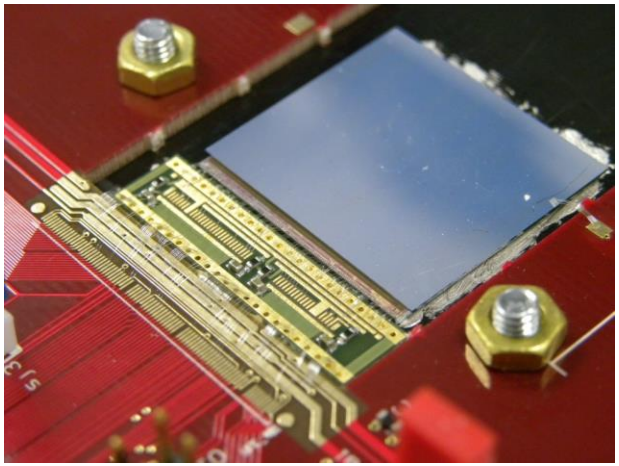
- Features both AC and DC coupling, poly-silicon/Punch Through Bias
- Production of 300, 200, 150, and 100 µm
- 4/10/13 kΩ bulk resistivity

2873-25-S9 2000x50 DC → ADV2000x50-DC-4
2873-25-S17 500x25 DC → ADV500-DC-4
2873-25-S18 500x25 AC → ADV500-AC-1
2873-25-S23 167x125 DC → ADV167-DC-4
2873-25-S24 167x125 AC → ADV167-AC-1

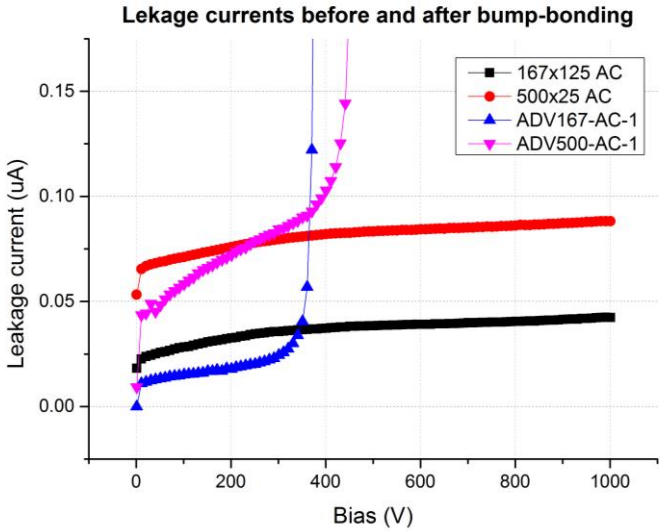


Full depletion voltage ≈ 75V

Assembling and Testing

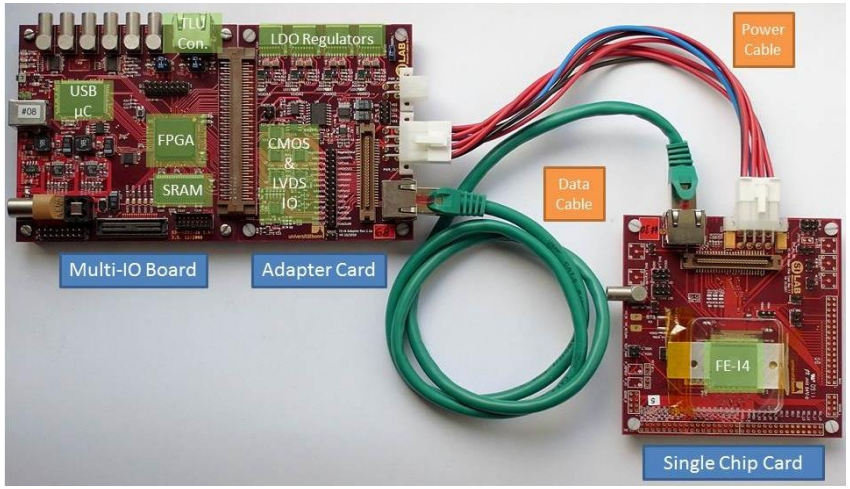


- The devices were bump-bonded at Advacam and assembled into modules using FEI4b Single Chip Cards (V1.1), PA5s and carbon-fibre support.
- Both chip LDOs are now supplied from VDDD at 1.8V.
- IVs were taken and show the breakdown voltage to be between 400 and 450V.

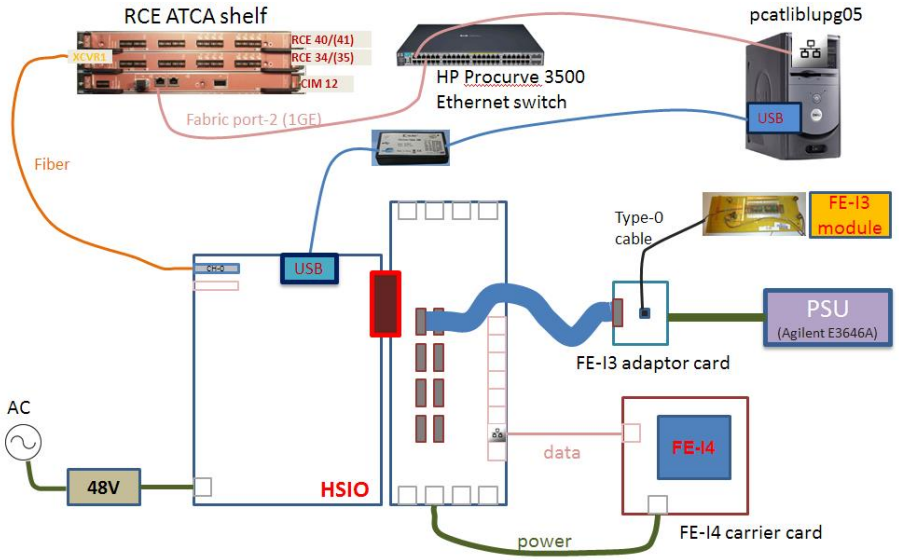


DAQs

USBPix

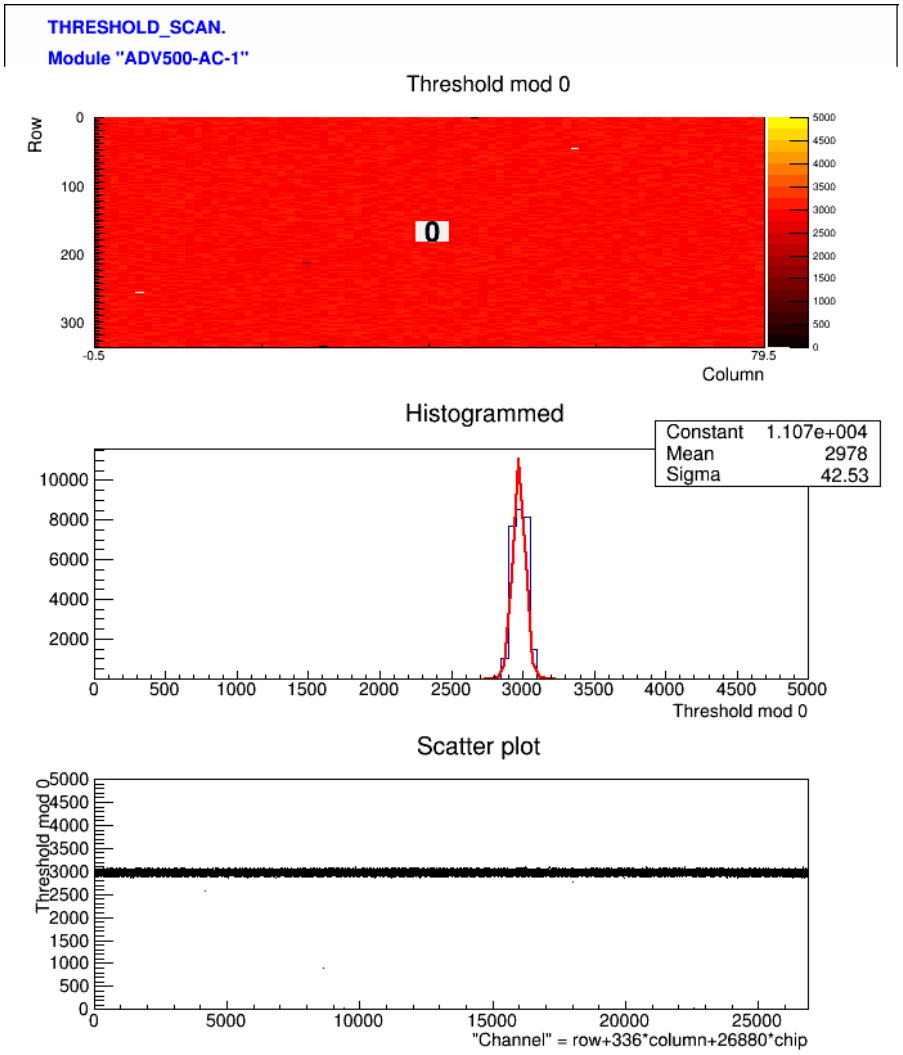


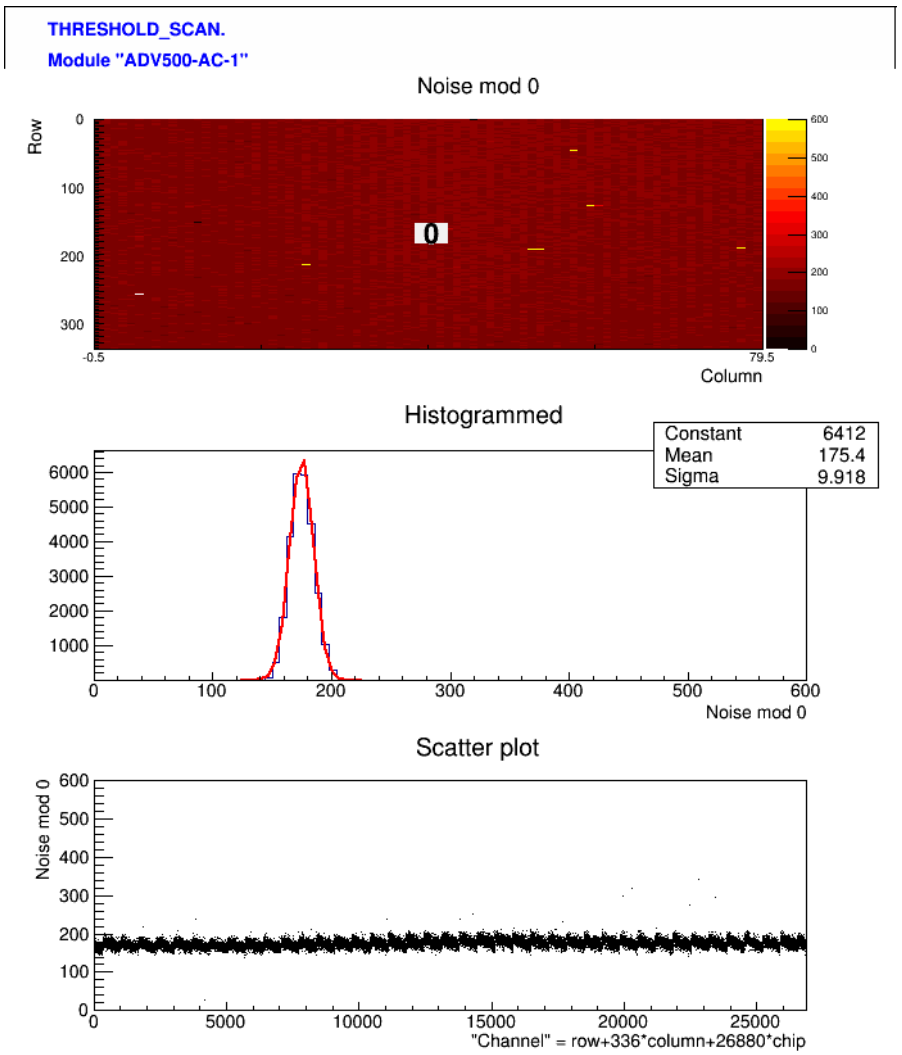
RCE



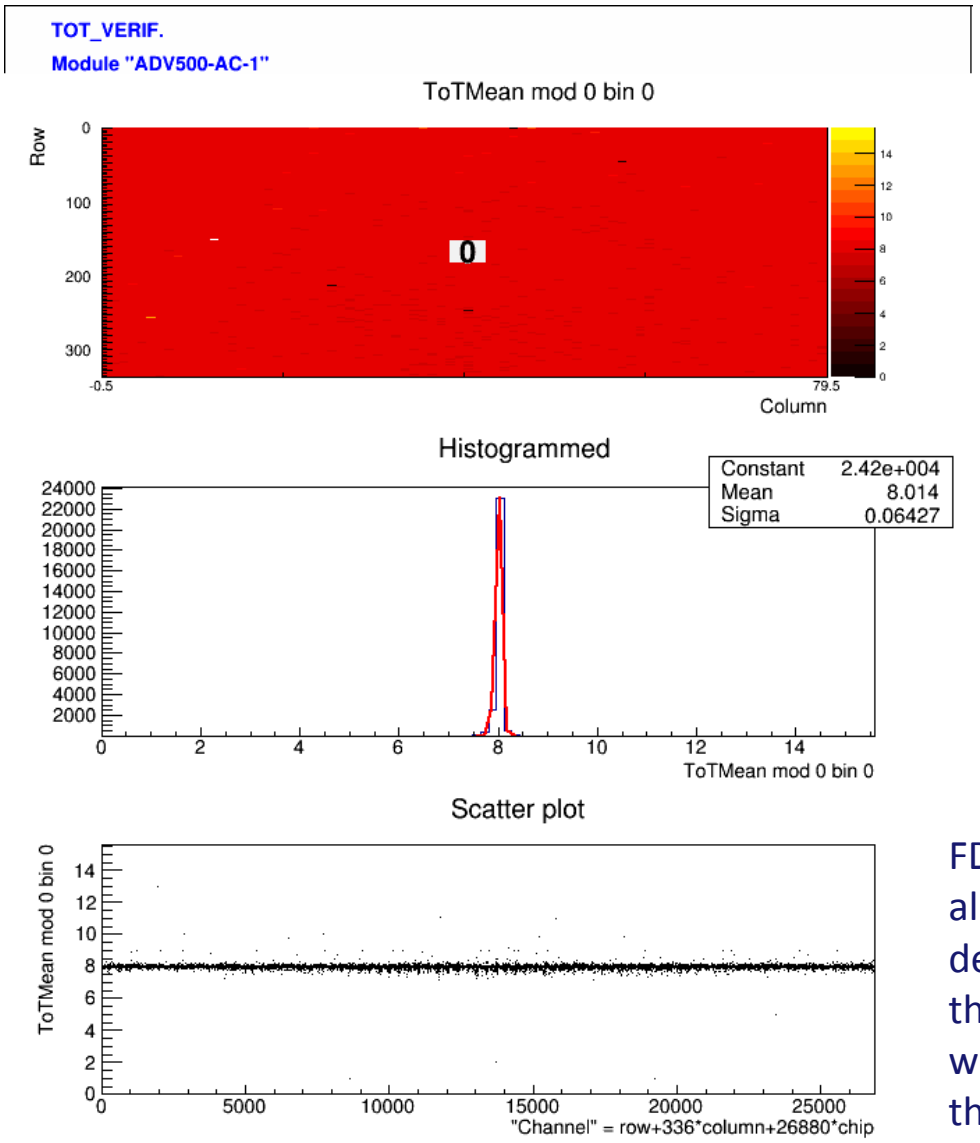
- All the devices were tuned (from 3000e to 1400e threshold, to 8ToTs@20ke) with both USBPix and RCE using standard or IBL primlists at 100V sensor bias.
- Since the USBPix showed better results in terms of noise and threshold dispersion, these were used in this talk, while the Source Scans were performed mostly with RCE in Selftriggering mode (2000s) using a Strontium-90 source (370MBq).
- Since data acquisition is still under way (24/7), some results are incomplete, however still good for relative estimation and comparison.

ADV500-AC-1 – 3000e, 8ToT@20ke (100% ch.used)



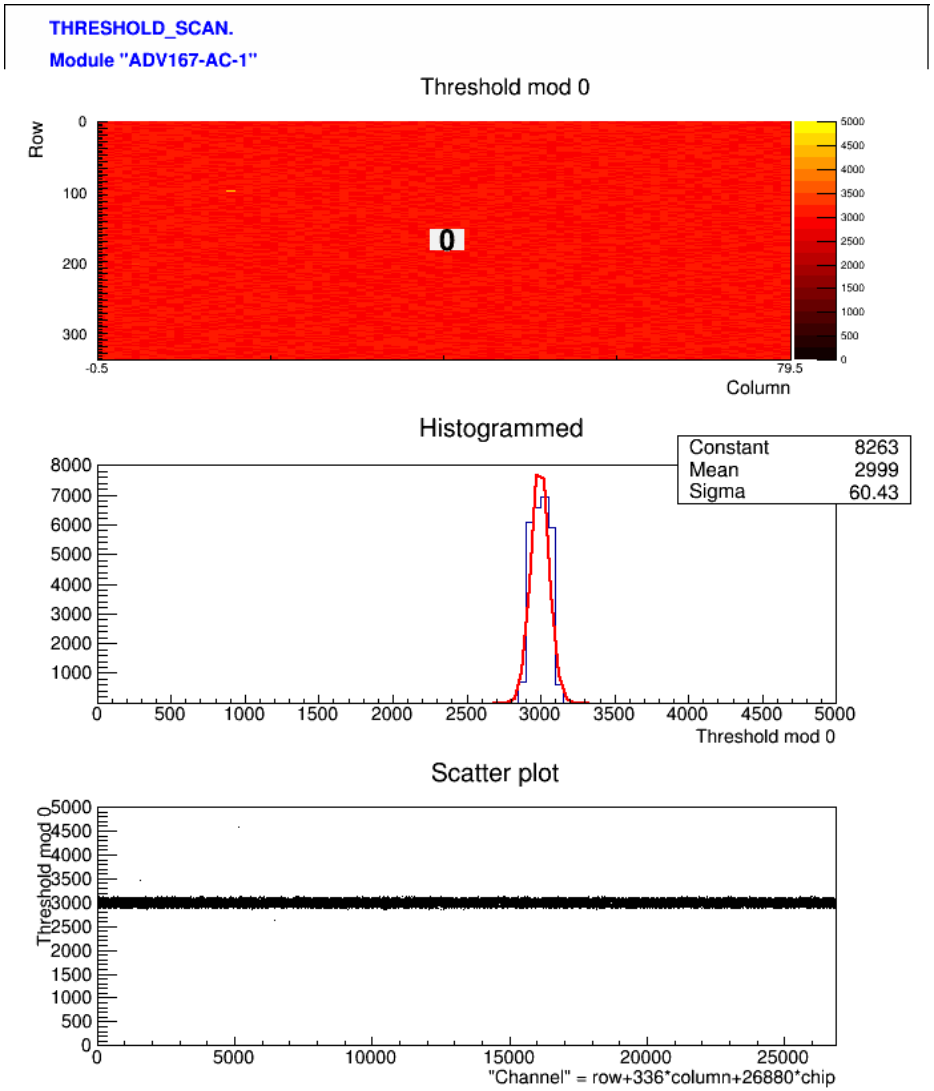


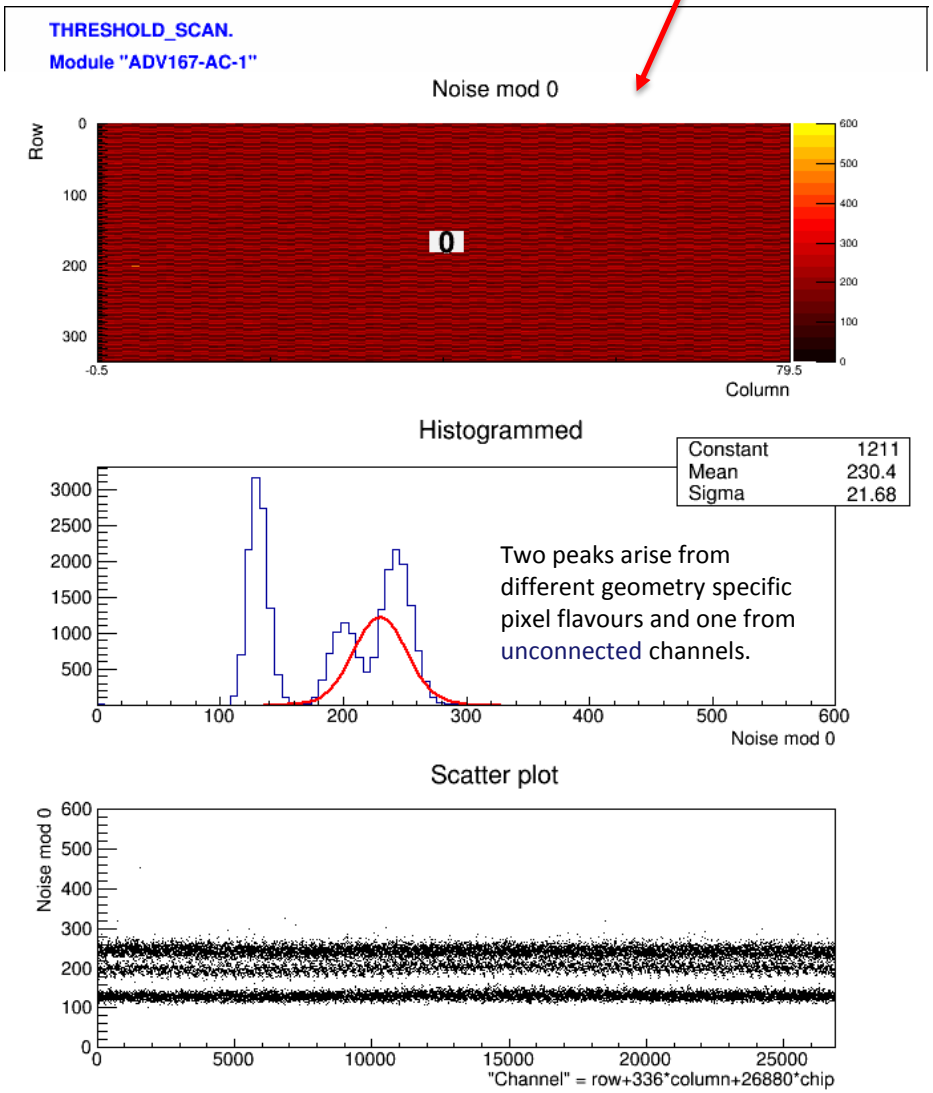
ADV500-AC-1 – 3000e, 8ToT@20ke (100% ch.used)



FDAC tuning performance was almost the same for all the devices, regardless of the threshold/noise and therefore will not be shown anymore in this talk.

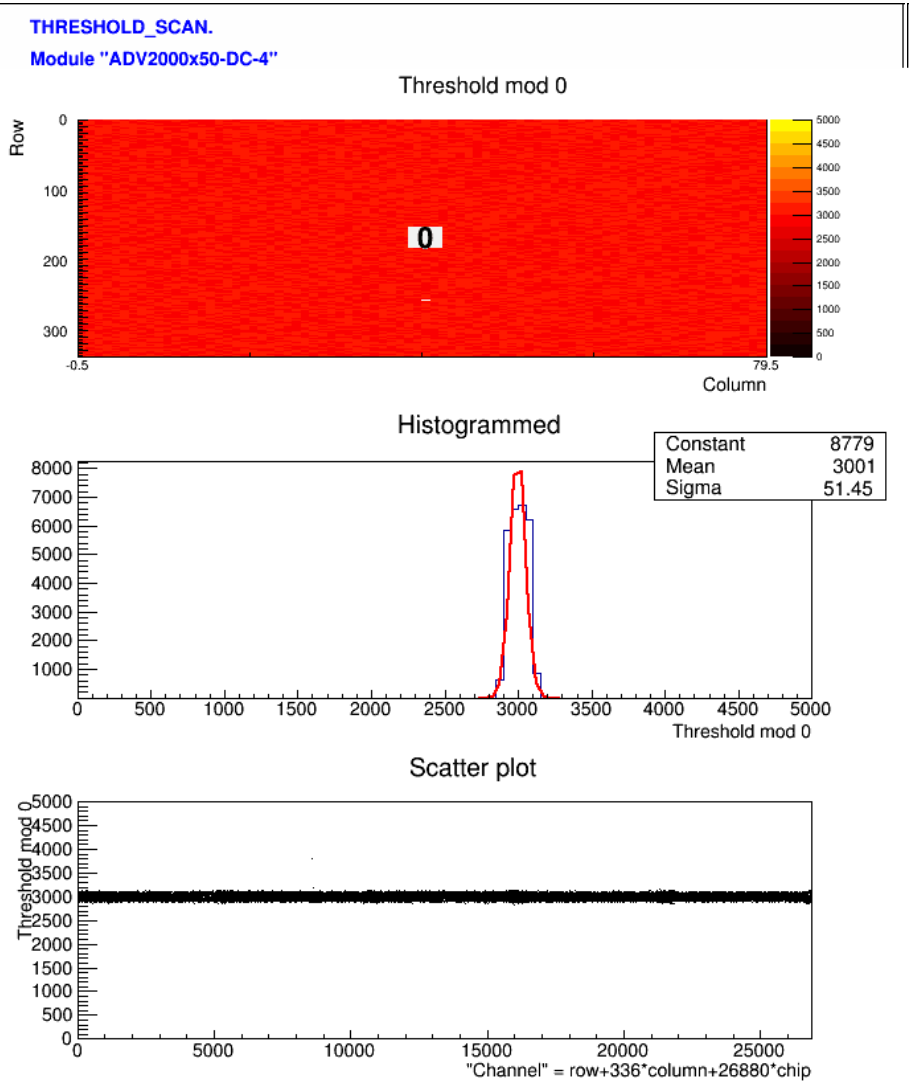
ADV167-AC-1 – 3000e, 8ToT@20ke (60% ch.used)

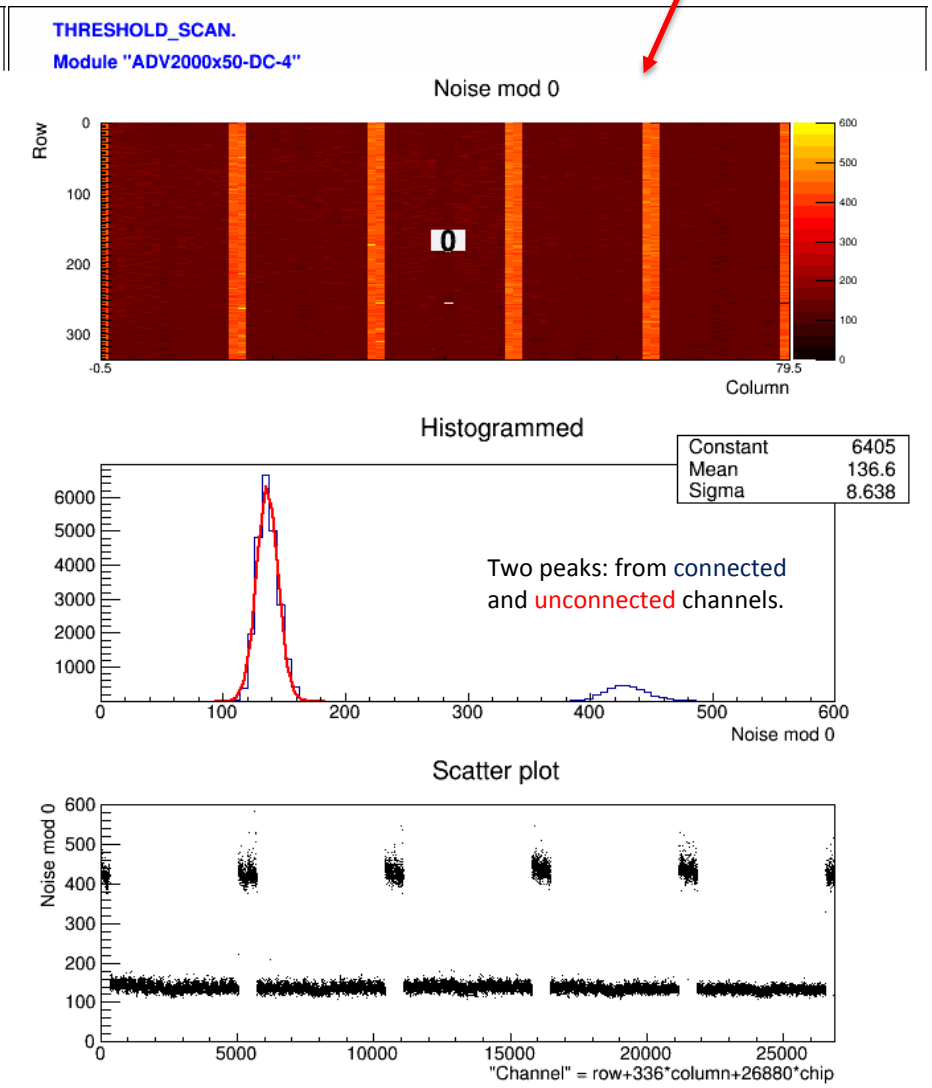




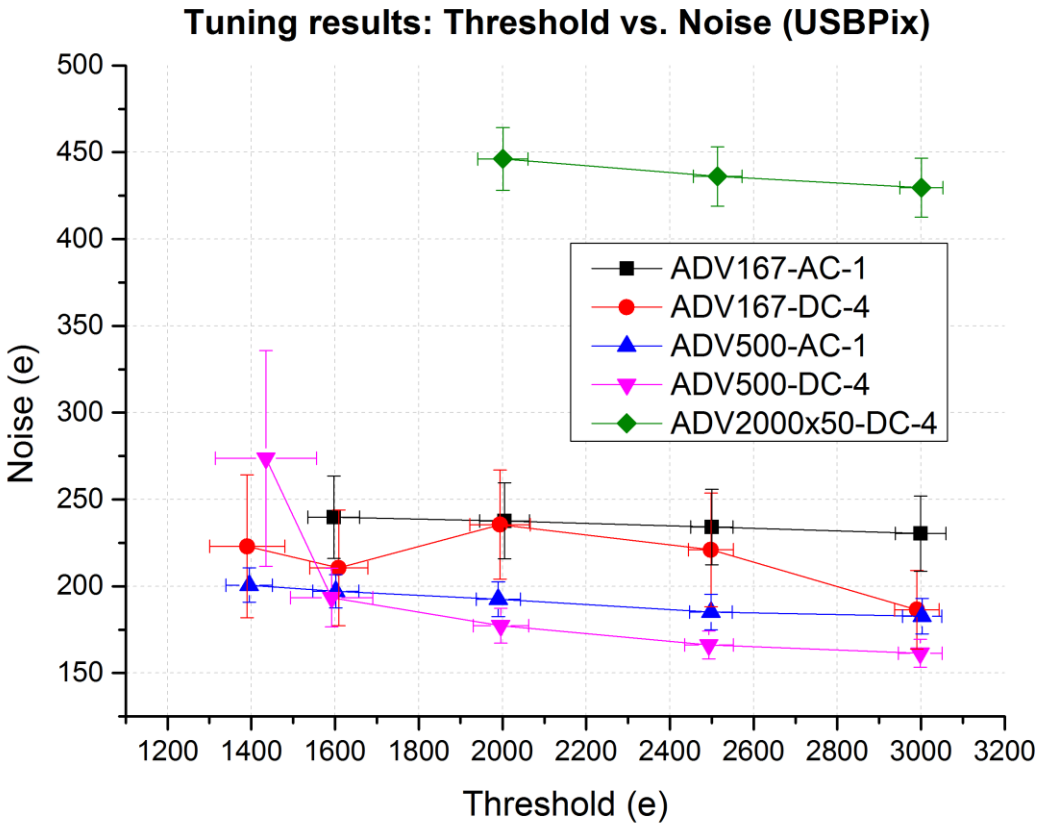
*Look at the backup slides for more details on specific pixel geometry!

ADV2000x50-DC-4 – 3000e, 8ToT@20ke (12.5% ch.used)



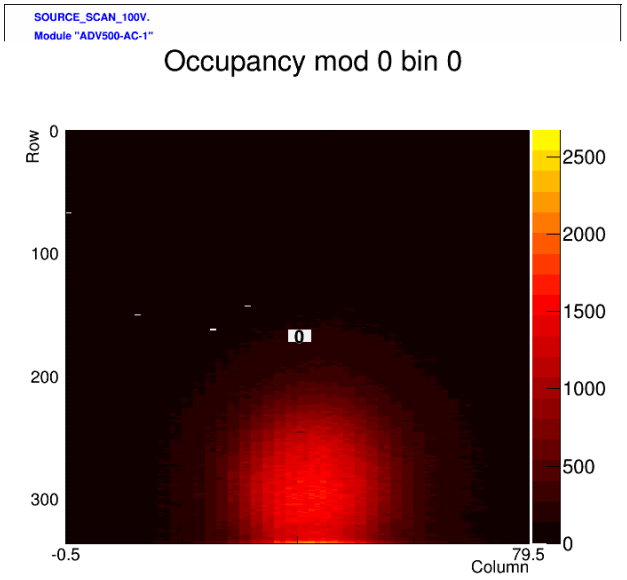


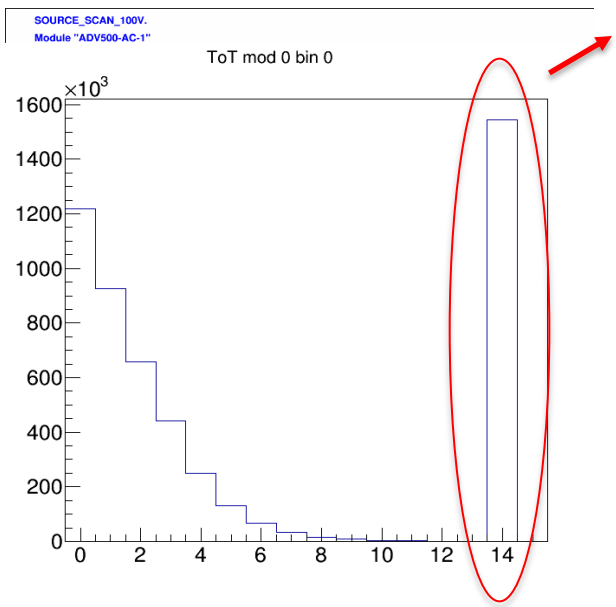
Threshold tuning summary for all DUTs



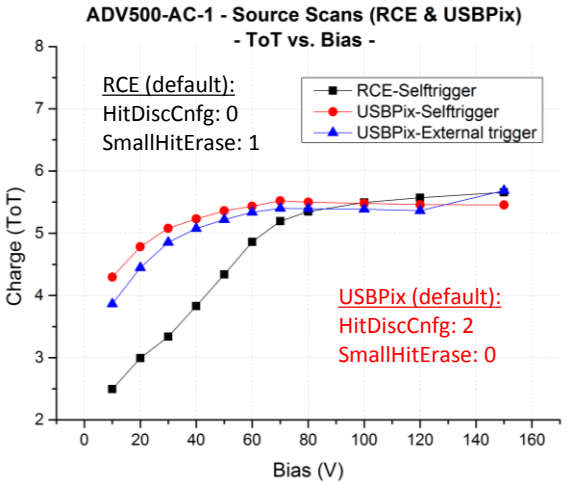
- Mean of double peak for connected pixels used for 167x125 geometry devices. Only connected pixels included for the strixel (2000x50) device.
- DC devices show slightly lower noise than AC coupled devices, however less stable.
- The strixel DC device shows much higher noise due to very long strips/interconnected pixels.

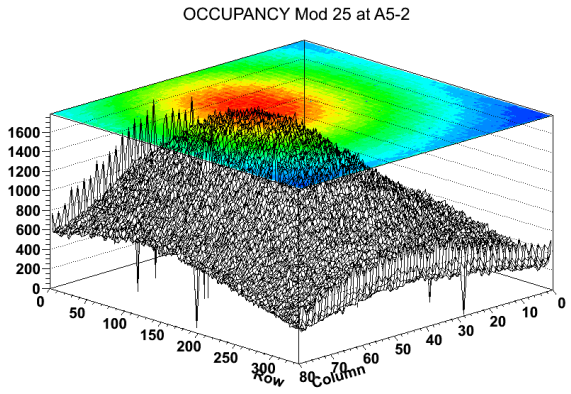
ADV500-AC-1 – ^{90}Sr Source Scans@100V bias, 3000e threshold, 8ToTs@20ke (USBPix&RCE)

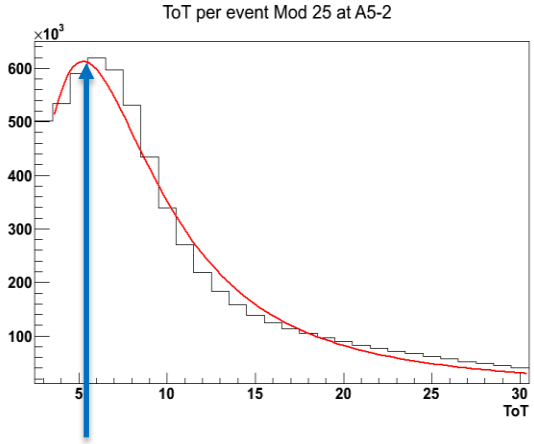


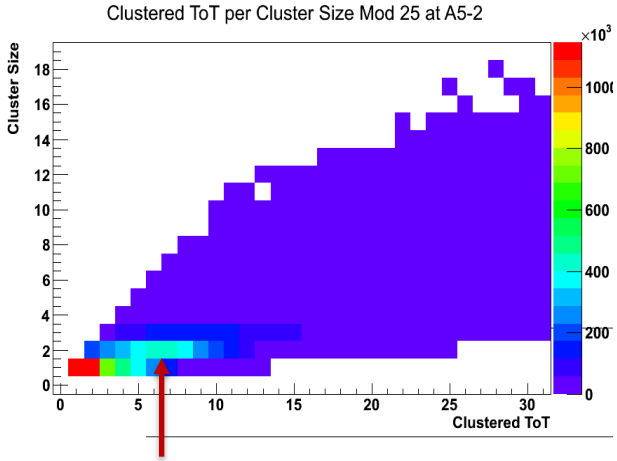


Charge deficit due to 'time-walk' (small charge induced in pixels giving rise to late hits) –by default, FEI4b discards these hits (tot<3) by encoding them as tot=14!

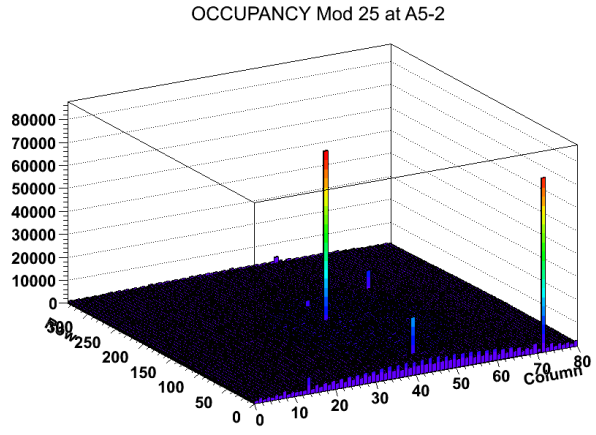


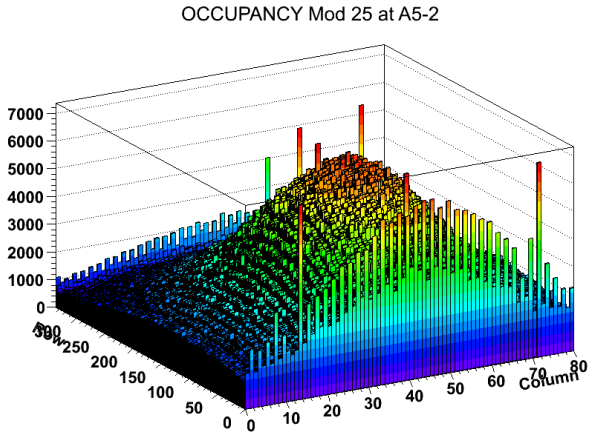


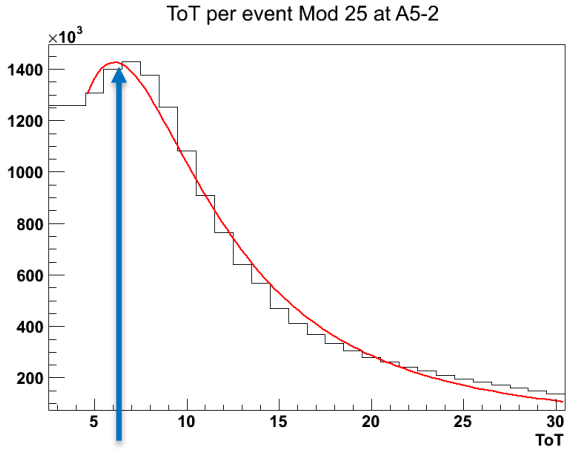


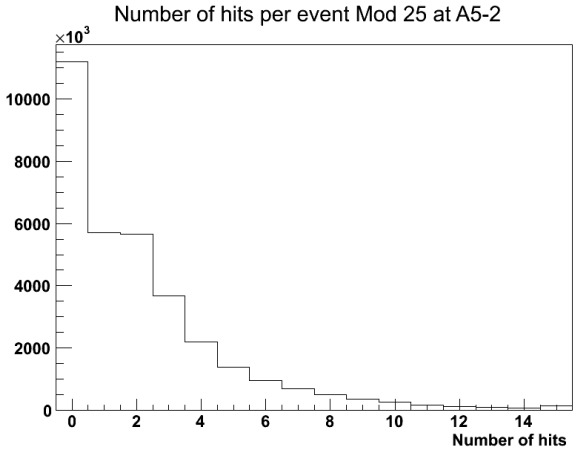


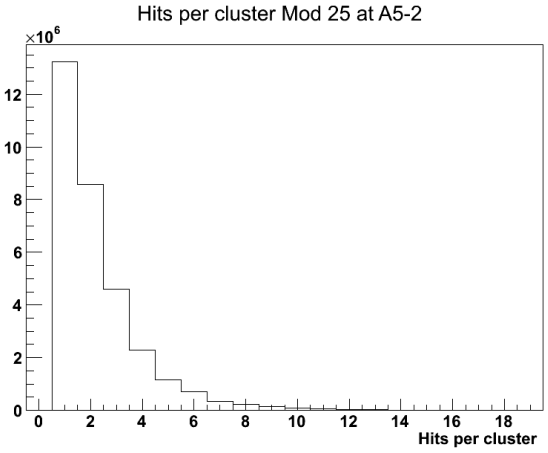
ADV500-DC-4 – ^{90}Sr Source Scans, TH:3000e, 8ToTs@20ke (RCE)

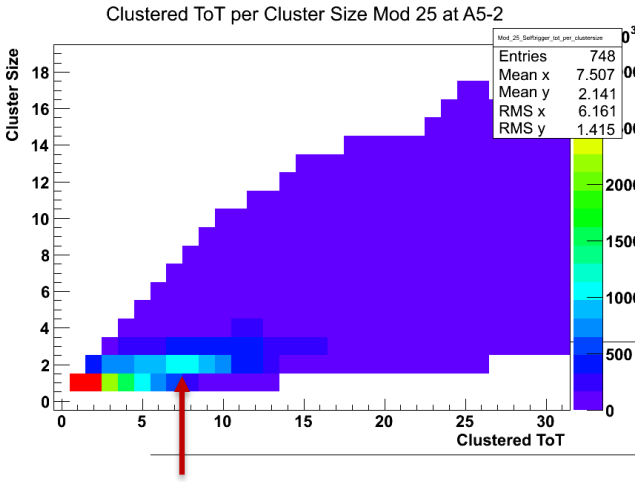




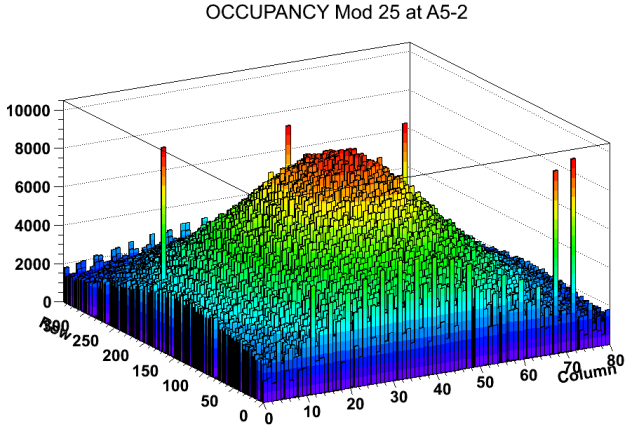


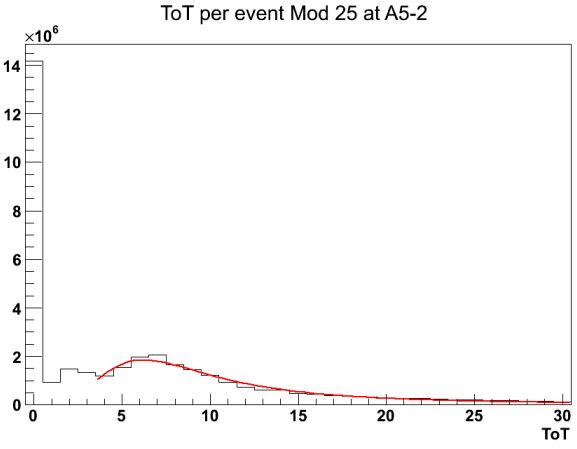


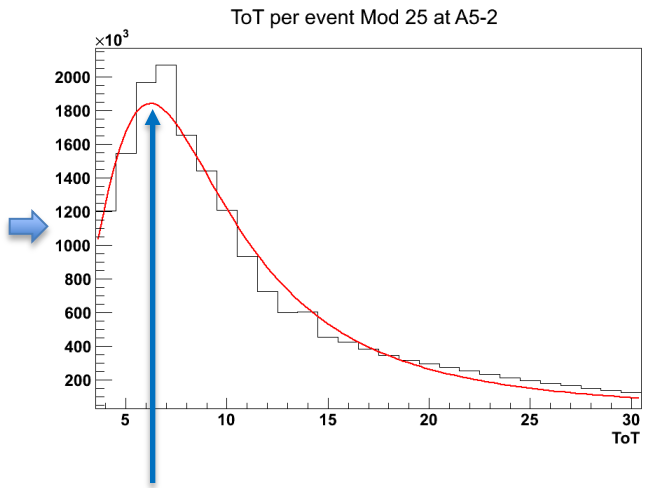




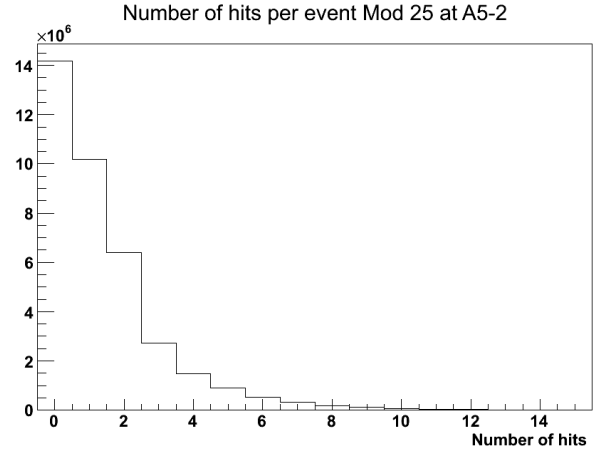
ADV167-AC-1 – ^{90}Sr Source Scans, TH:3000e, 8ToTs@20ke (RCE)

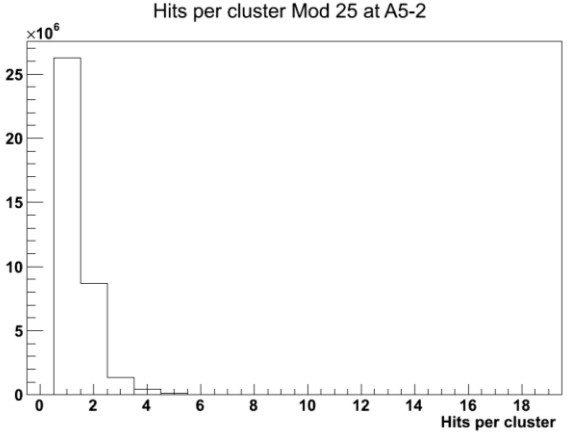


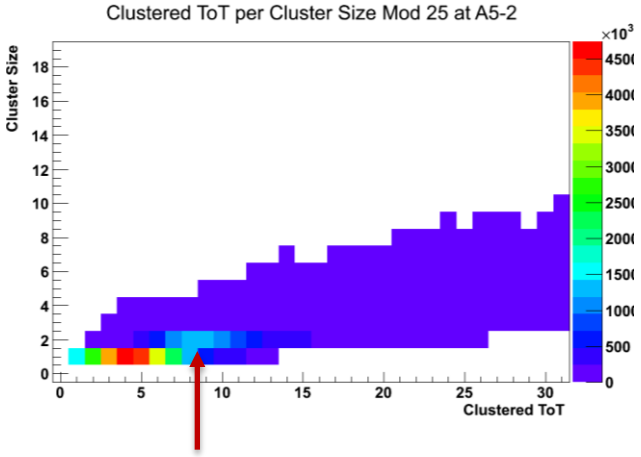




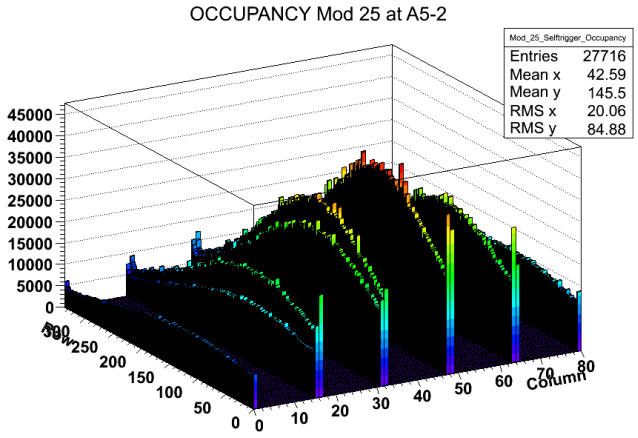
The smaller the cluster size, the smaller observed charge deficit!

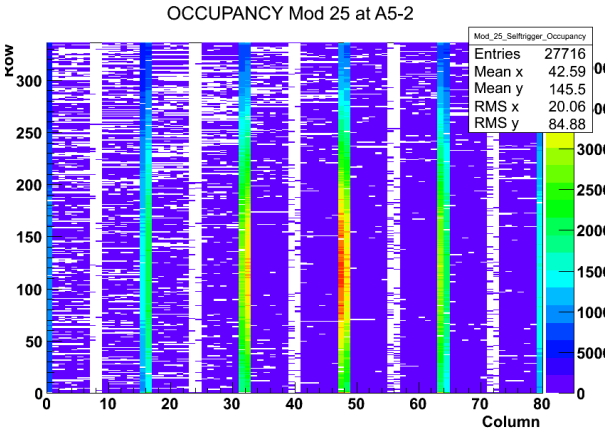


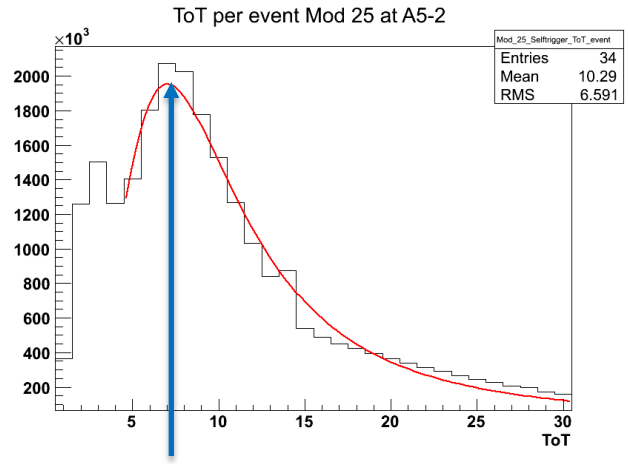




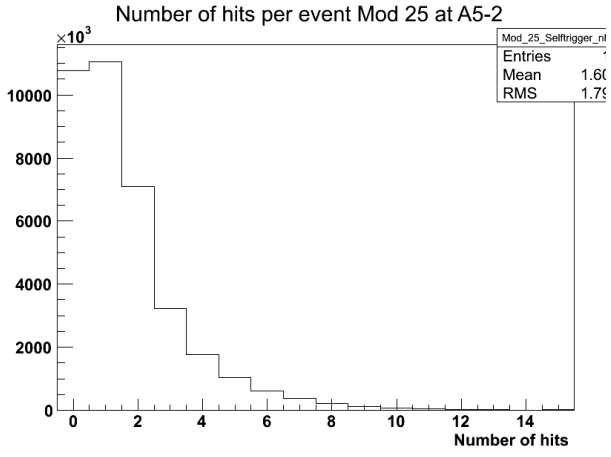
ADV2000x50-DC-4 – ^{90}Sr Source Scans, TH:3000e, 8ToTs@20ke (RCE)

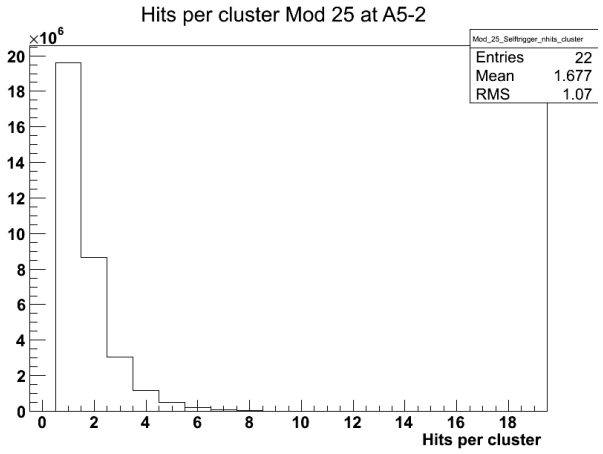


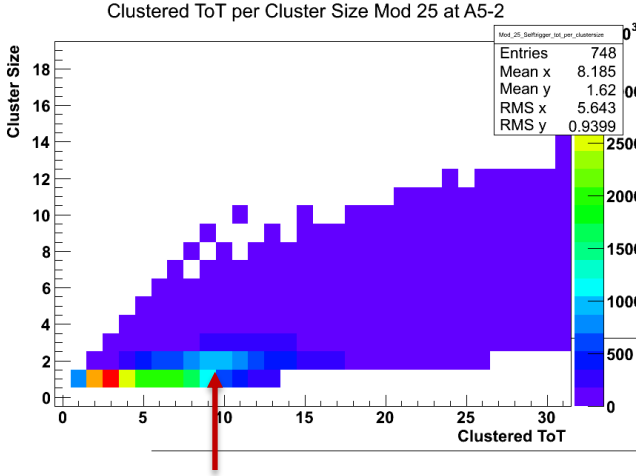




The strixel device has slightly larger clusters than 167x125 device due to long pixels.

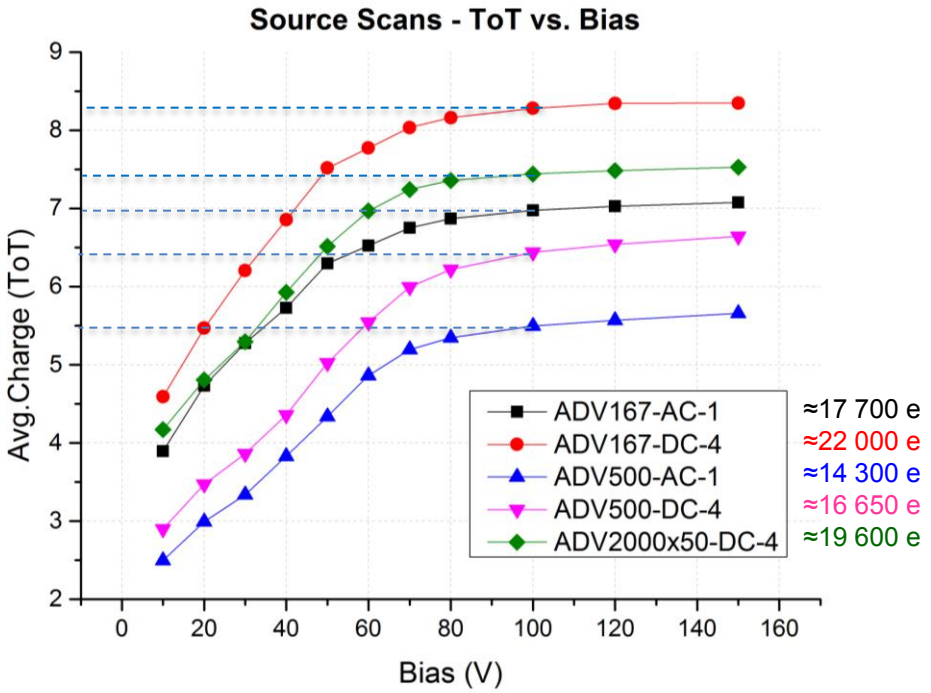


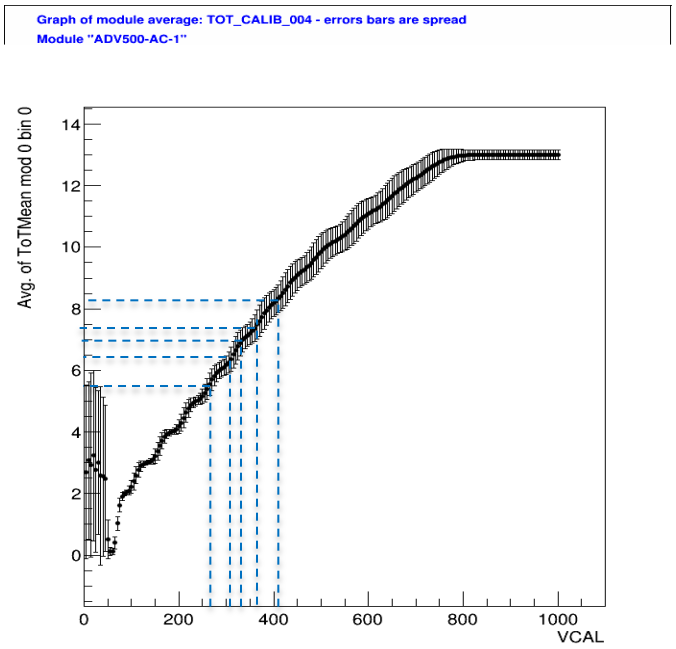




*The geometry specific pixel matrix of ADV167 can be found in backup slides.

Source Scans Summary





- Although absolute ToT/charge measurements are not available at the moment, it is possible to make relative charge collection comparison same geometry structures.
- The collected charge for AC coupled devices is only ≈10-20% less than for the DC ones.
- Still to test 125x100 AC and DC, as well as 2000x50 AC and resolve charge deficit issue.

Summary

AC coupled detectors show, before irradiation, significant charge collection efficiency and lower noise wrt DC coupled sensors with identical geometry. This is promising in view of possibly using this technique for improved performance of the sensors after irradiation. This can be further optimise if the design of the readout chip (FE-I4 in this case) is taking this type of coupling into account.

Backup

BACKUP SLIDES

Capacitances & SiO_2 thickness calculation

- Two different test structures (C-DIF and C-SUB) were employed to calculate the gate and the field oxide thicknesses.

C-DIF test structure

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implant area: 1020 x 1670 µm² (1.70 · 10⁻⁶ m²)
metal area: 1000 x 1450 µm² (1.45 · 10⁻⁶ m²)

Depleted PN-junction capacitance = 0.7pF @50V (0.4 pF / mm²)
MOS capacitance = 250 pF (170 pF / mm²)

Gate oxide thickness = 0.2 µm

C-SUB test structure

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metal area: 1000 x 1450 µm²

MOS capacitance = 50 pF (35 pF / mm²)

Field oxide thickness = 1 µm

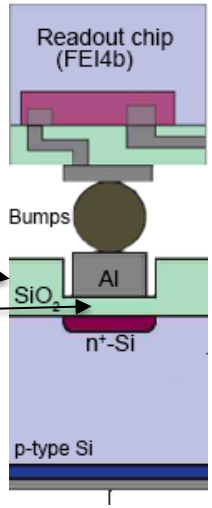

Photo-diode measurements

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implant area = 4300 x 4300 µm² (1.85 · 10⁻⁵ m²)

Depleted PN-junction capacitance = 14 pF @50V (0.75 pF / mm²)

167 x 125 um pixel AC single chip sensor measurement

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implant area = 167 x 125 x 120 x 138 µm² + (20000 + 17300) · 2 · 38 µm² (3.5 · 10⁻⁴ m²)

Depleted PN-junction capacitance = 250 pF @50V (0.72 pF / mm²)

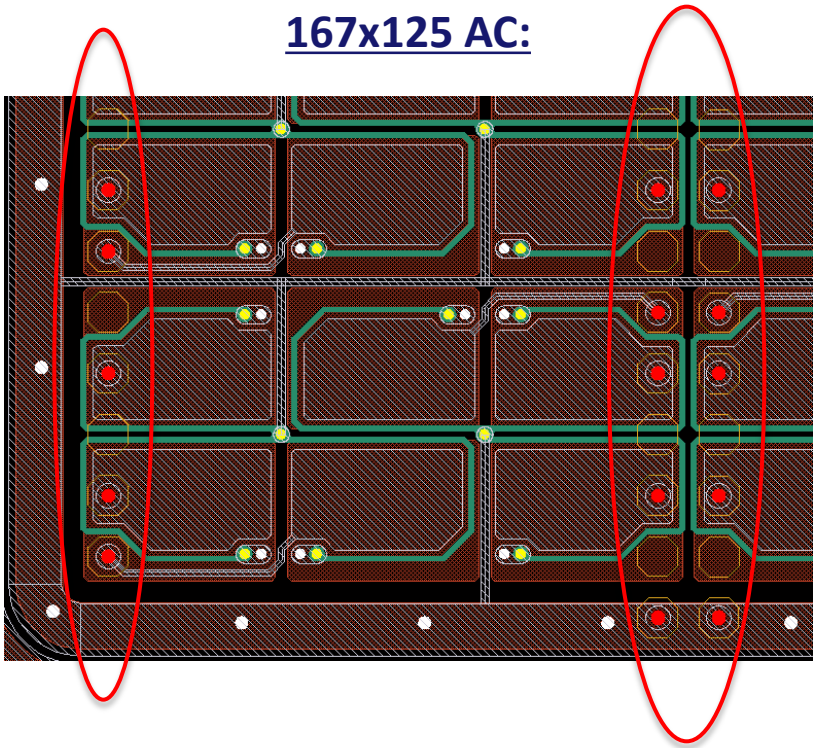
Inter-strip/pixel capacitance

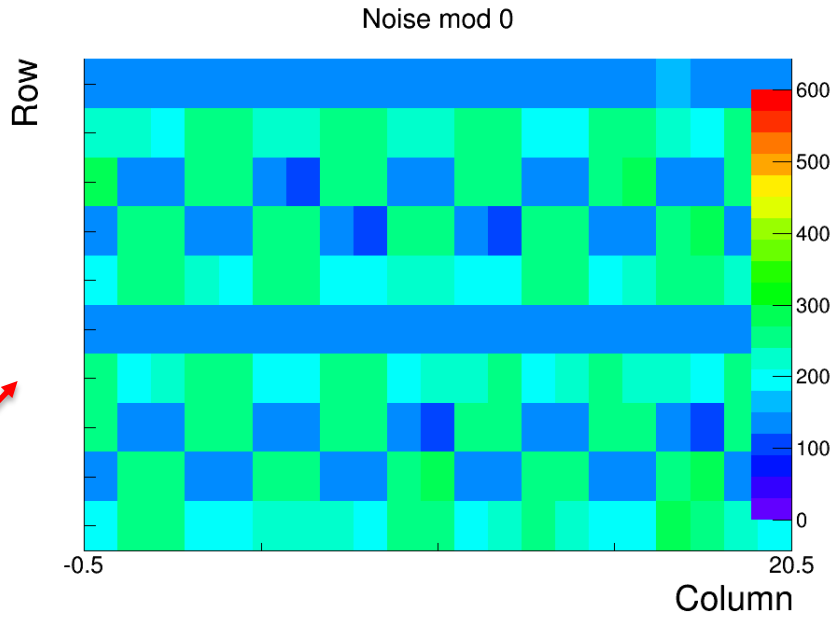
Bulk capacitance: 35 µm x 10500 µm = 0.37 mm² x 0.7 pF/mm² = 0.25 pF

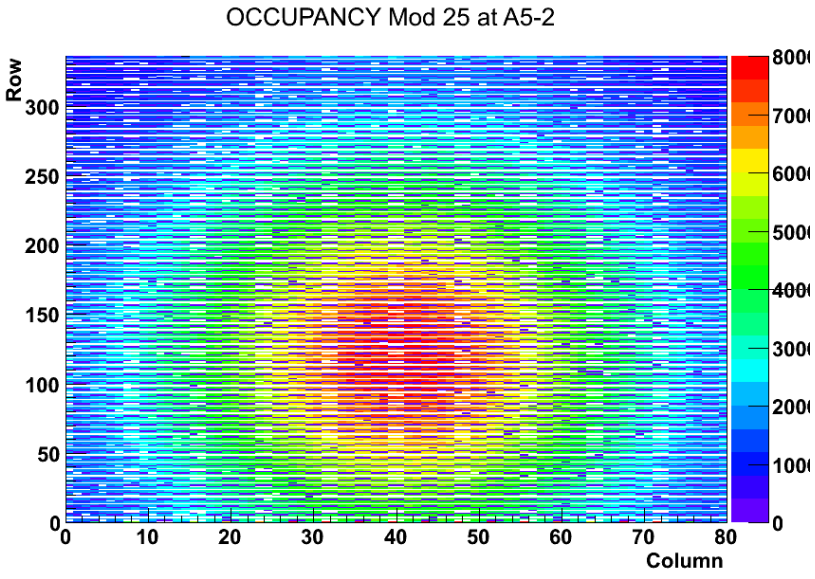
Inter-strip/pixel capacitance ≈ 0.5 pF/cm²

ADV167 pixel structure

167x125 AC:

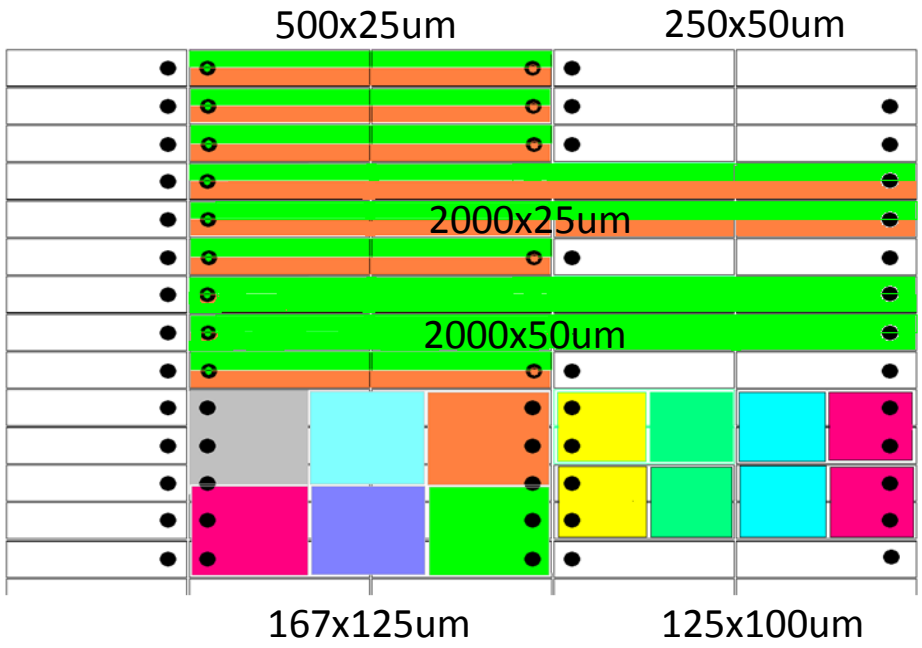




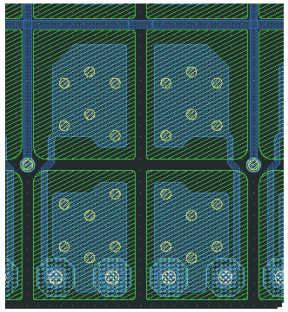


CERN Pixel V alternative geometries – adaptive pixel size

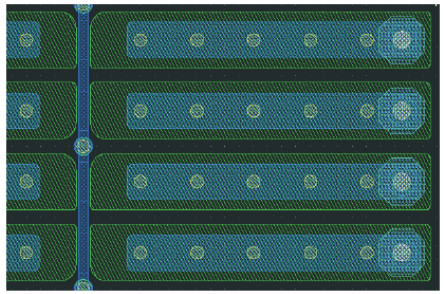
- Compatible with FE-I4 UBM pads.
- Various pixel sizes, punch through/polysilicon biased, AC and DC coupled



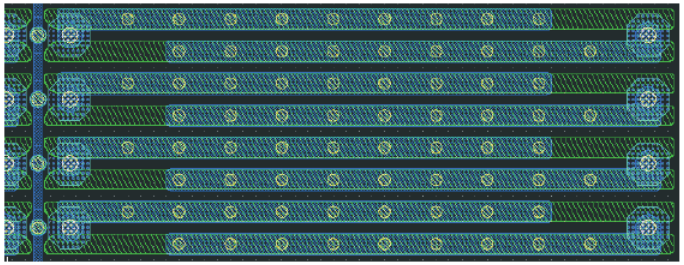
125x100



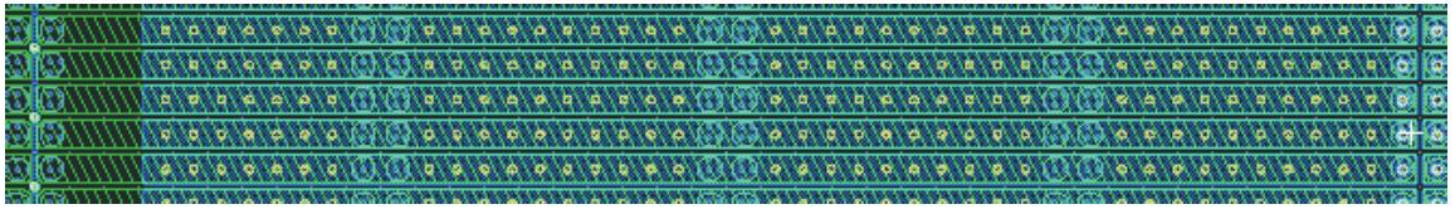
250x50



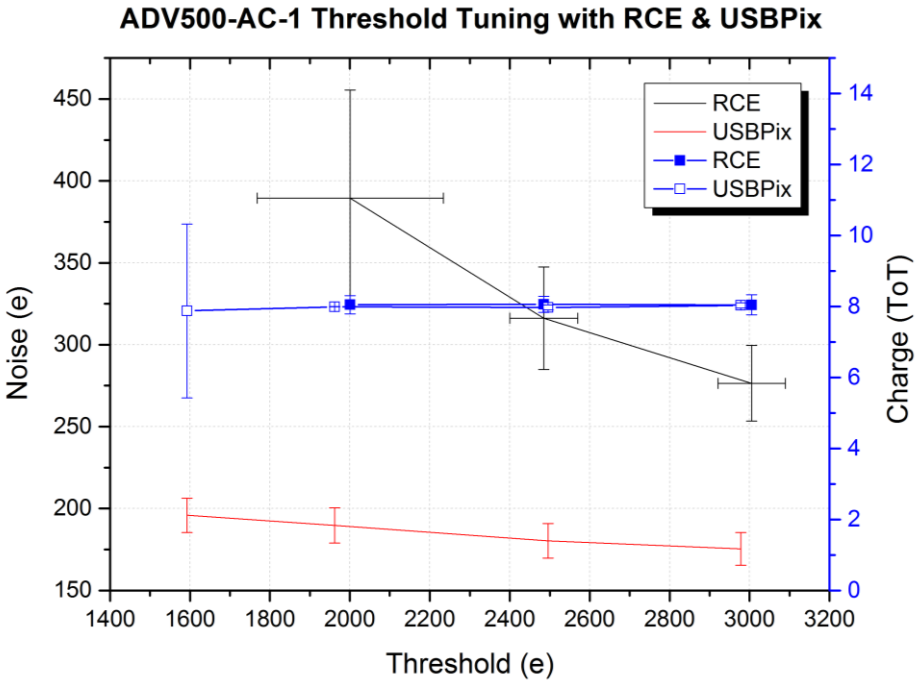
500x25

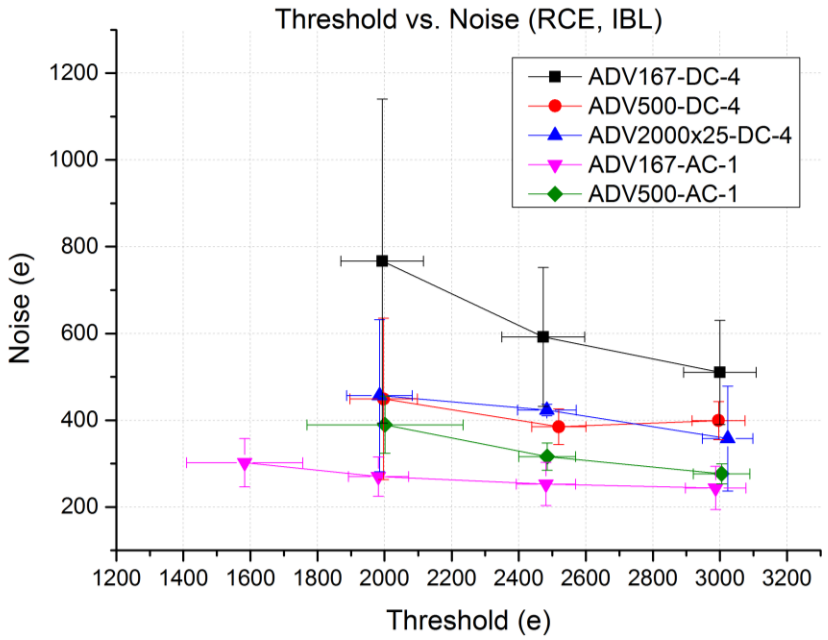


2000x50 (strixel)



Threshold tuning results comparison: USBPix vs. RCE





- It was not possible to tune below 2000e for most of the devices using RCE.