New Technological Capabilities at CNM

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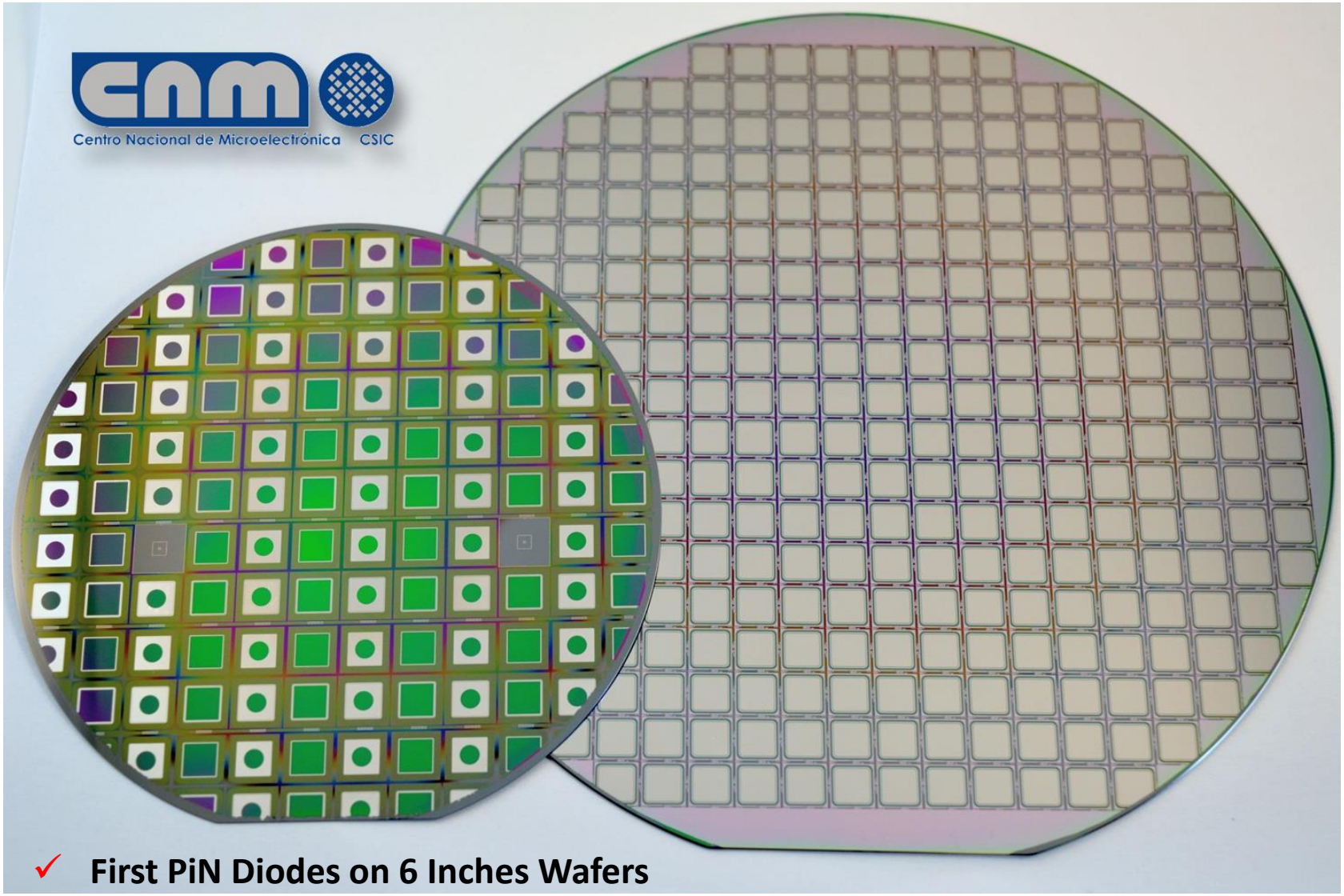
Outline

- Available Technologies in 4” and 6” Developments
- Automated Layout Generation
- Reverse Engineering Analysis Procedures
- Automatic Electrical Characterization

Technology Status

Name	Geom.	Substr.	Double Metal	Thikness (µm)	Double Side	Wafer Size
DC Detectors (Nuclear app.)	Planar	N	Yes	10-1000	Yes (>200 µm)	4”
DC Detectors (HEP)	Planar	N/P	Yes	10-1000	Yes (>200 µm)	4” (6”)
AC Microstrips (HEP)	Planar	N/P	Yes	10-1000	Yes (>200 µm)	4” (6”)
LGAD	Planar	P	Yes	10-1000	Yes (>200 µm)	4” (6”)
3D Double Side Detectors	3D	N/P	Yes	200-300	Yes (>200 µm)	4”
U3DTHIN	3D	N	Yes	5-300	No	4”
Microdosimeter	3D	N	No	5-300	No	4”
Fan-in	Planar	-	Yes	300-1000	No	4” (6”)

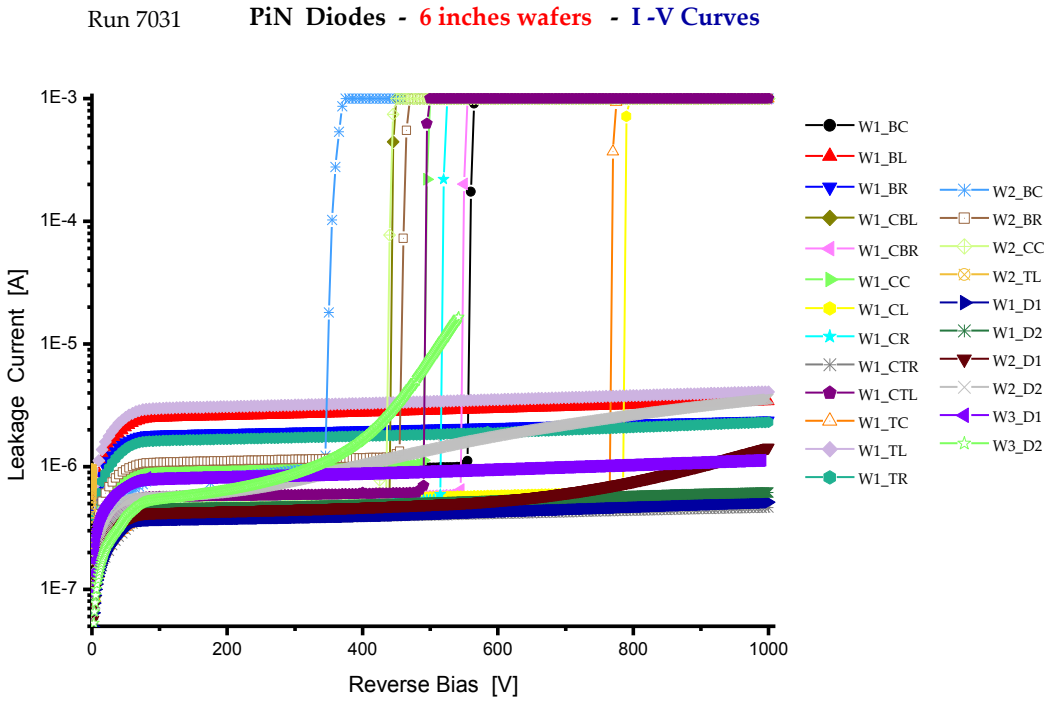
6 inch Technological Process

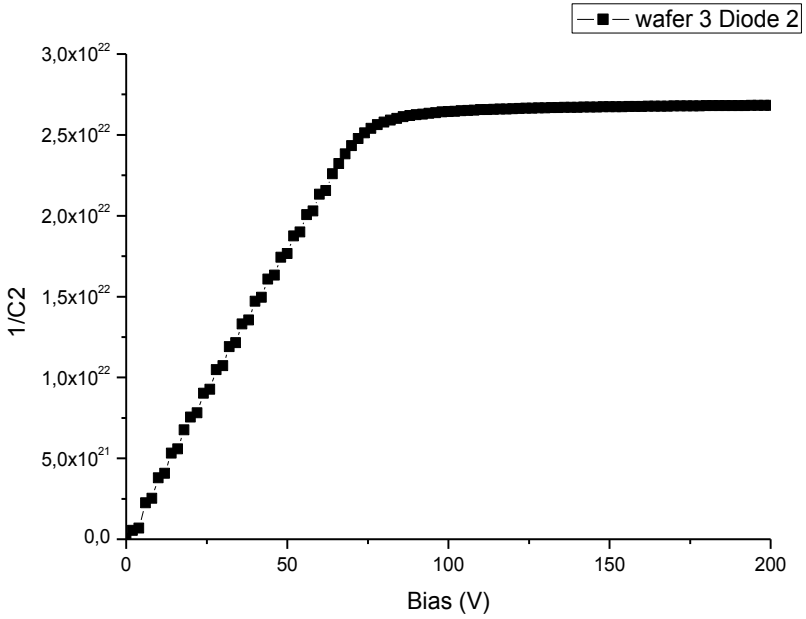


✓ **First PiN Diodes on 6 Inches Wafers**

6 inch Technological Process

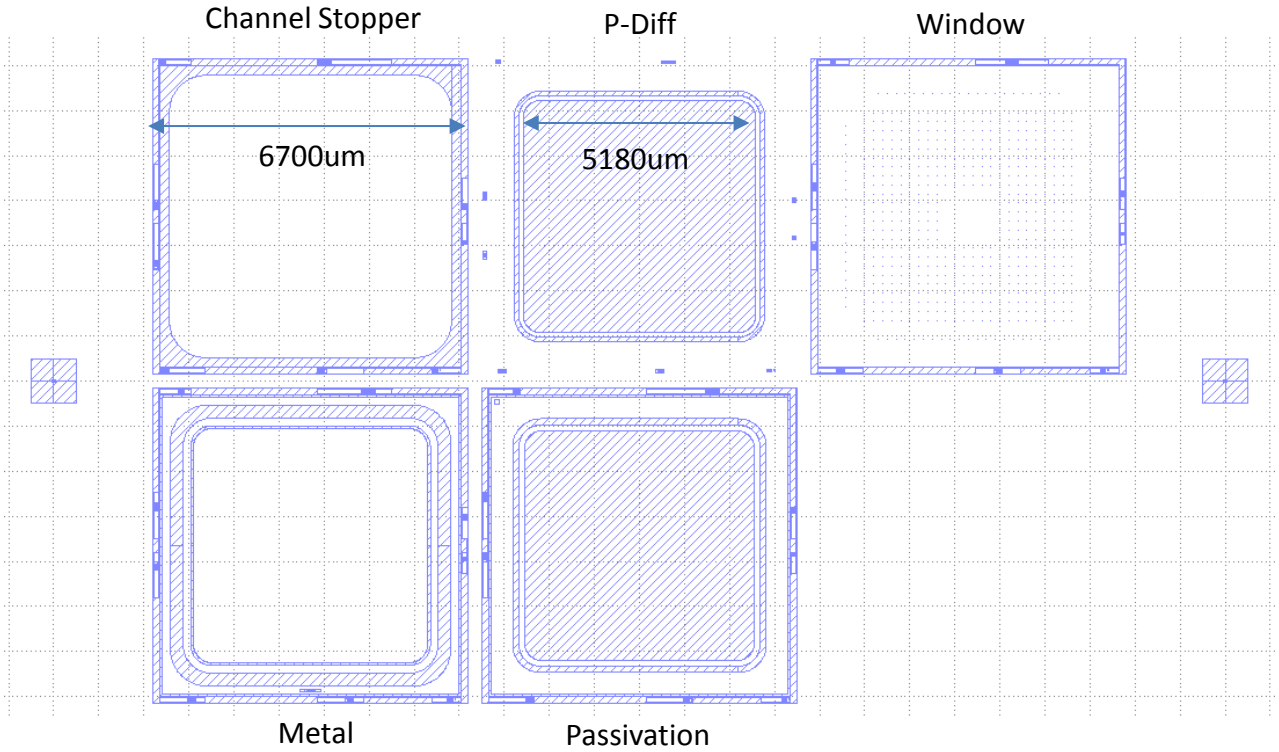
- **First Results:**
  - ✓ Good electrical performance (leakage, full depletion, etc)
  - ✓ Comparable to 4 inch technology PiN diodes





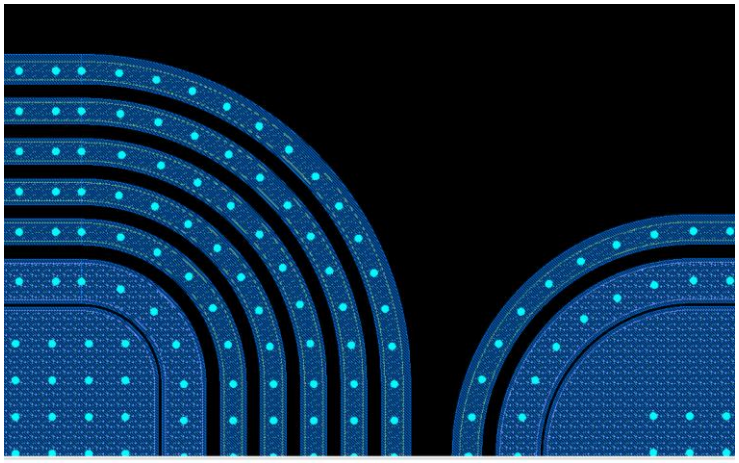
6 inch Technological Process

- **Photolithography with Stepper:**
  - ✓ All layers designed in one single stepper crystal. Standard in CMOS technologies. Minimum resolution 0.25 µm
  - ✓ Contact masks can also be used to produce large size (whole wafer) detectors.

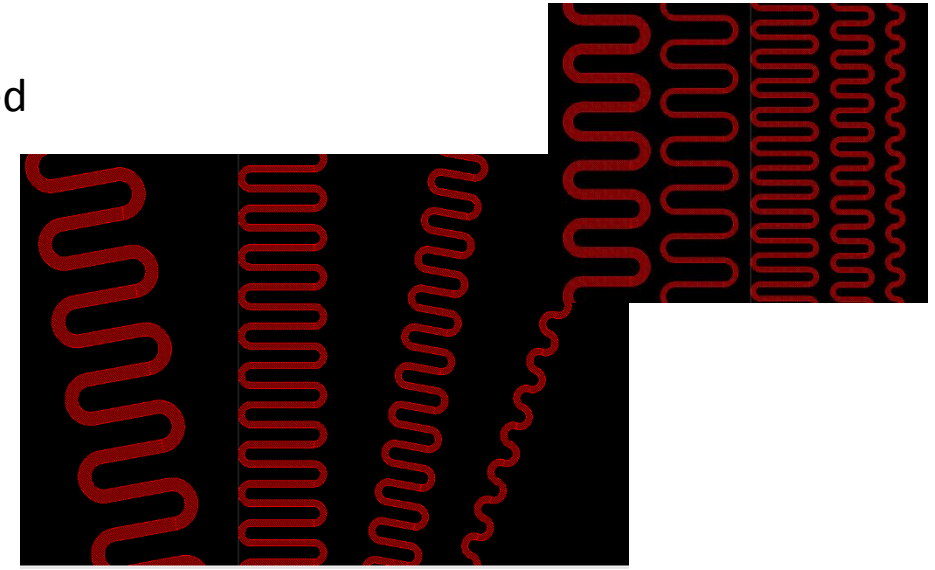


Automatic Layout Generation

- **Fast and efficient automatized layout generation with Glade/Python:**
  - ✓ Freeware IC layout editor: **Glade** (Gds, Lef and Def Editor) by Peardrop Design Systems capable of reading GDS2, OASIS, LEF and DEF plus a few other formats. Currently available for Windows, Linux, Mac OS X and Solaris.
  - ✓ Glade is extendable using **Python** scripting and parameterized cells (Pcells).
  - ✓ We can design complex layout using a complete library of simple parameterized functions.

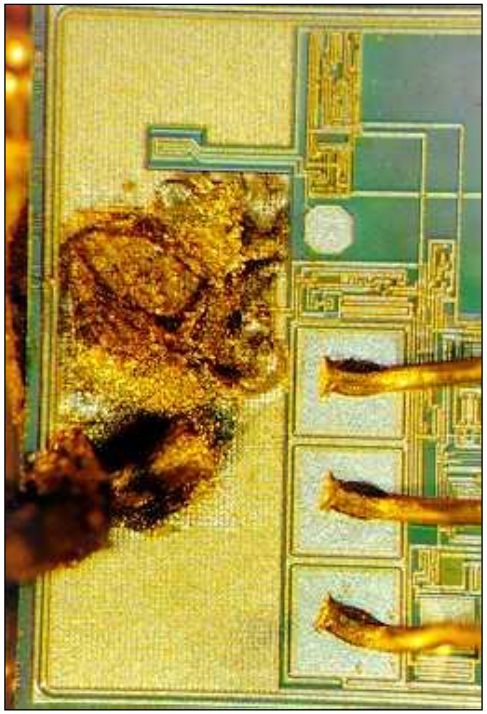


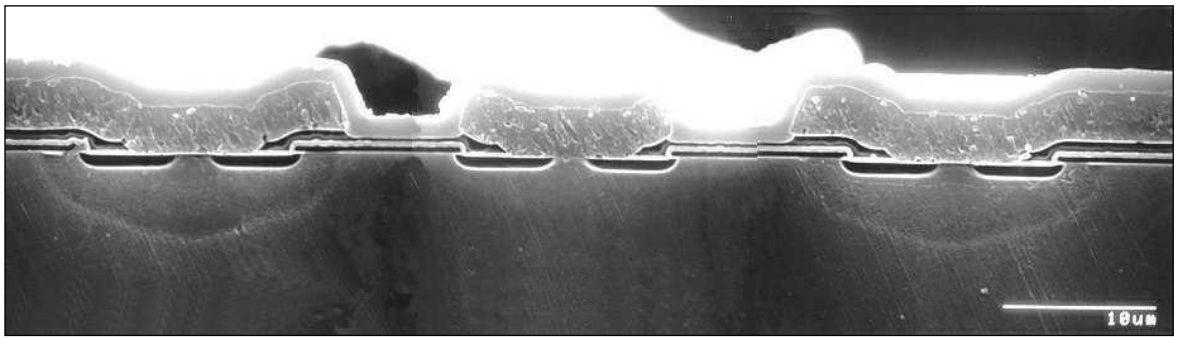
- **Full sensor layout generation:**
  - ✓ Strip rows generation
  - ✓ Stereo angle
  - ✓ Bonding pads
  - ✓ Bias resistors
  - ✓ Bias and guard rings

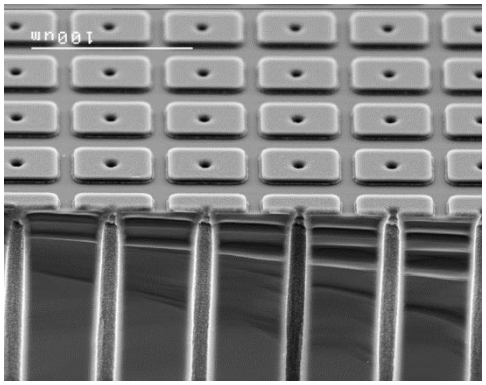


Reverse Engineering on Microelectronic Devices

- The **Reverse Engineering Group** was created by the **Physical Characterization** and the **Design & CAD** staff with a high skills in the **integrated circuit analysis and reconstruction**.
- Expertise in the study of the procedures and the techniques which help to **determine the origin of the failures** (malfunctions, destruction) on a wide range of electronic devices and circuits, providing the **actions to be taken to eliminate the failures and to increase the reliability**.
- The Reverse Engineering **covers from the analysis to the top-down reconstruction** of discrete devices and integrated circuits.
  - ✓ Process technology characterization
  - ✓ Identification of building blocks
  - ✓ Layout errors
  - ✓ Etc.

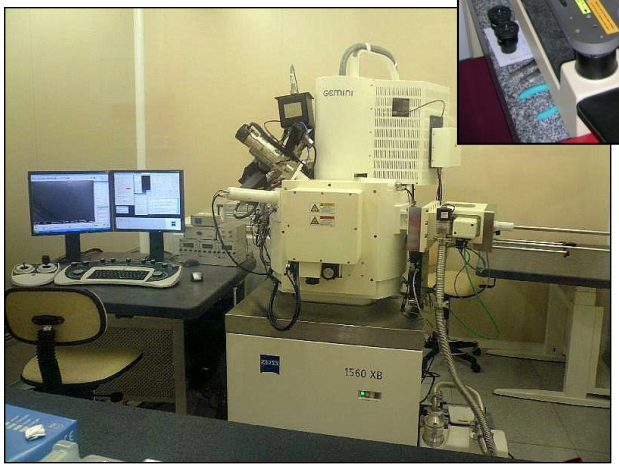






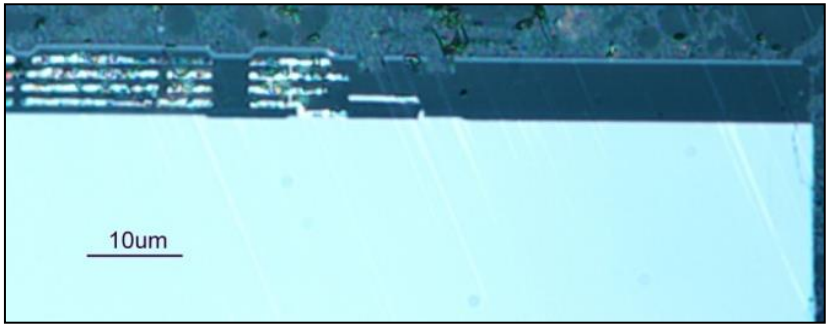
Reverse Engineering

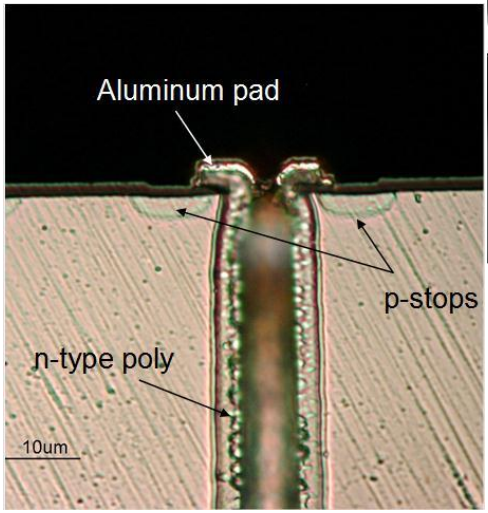
- **Equipment. Physical Characterization**:
  - ✓ Focus Ion Beam (**FIB**)
  - ✓ 2 Atomic Force Microscope (**AFM**)
  - ✓ 3 Scanning Electron Microscope (**SEM**)
  - ✓ Automatic **polishing** machine with multi-sample head
  - ✓ Automatic **polishing** machine with two heads suitable for micro-sections
  - ✓ Diamond **saw**
  - ✓ **Optical microscopes** (micro-measurement, dark field and interferential contrast)
  - ✓ **Photo** microscope
  - ✓ **Plasma** equipment for layer removal
  - ✓ **Probe system** with submicron needles and **laser cutting** facility
  - ✓ **Die attach**. Wedge and ball **bonding** facilities.

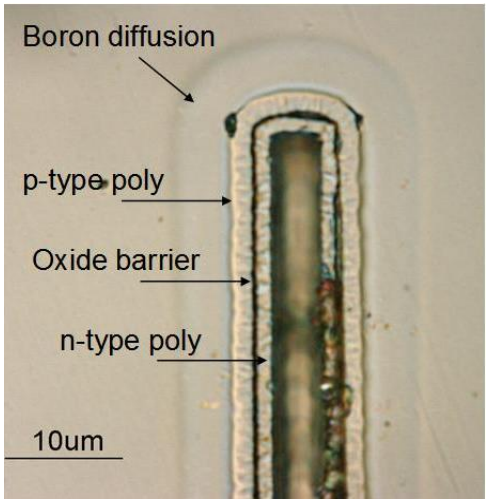


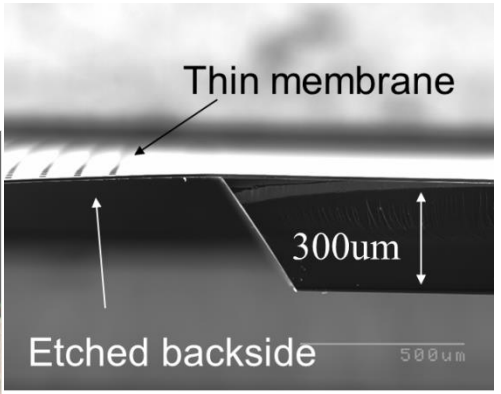
Reverse Engineering

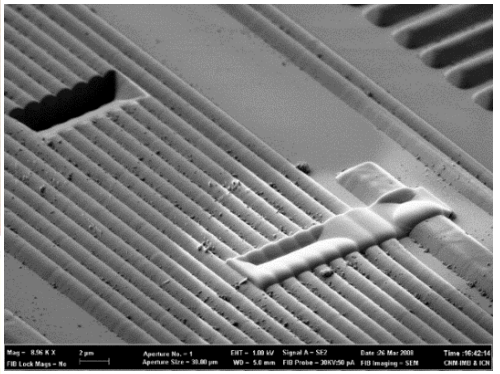
- **Techniques**:
  - ✓ Decapsulation
    - ✓ **Die recovery**
  - ✓ Microsection Procedure
    - ✓ **Technology Information**
  - ✓ High precision mechanical layer removal
    - ✓ **Bottom-up** circuit analysis
    - ✓ **Top-down** circuit analysis
  - ✓ Chemical stain of high doped diffusions
    - ✓ **Memory contents** identification
  - ✓ FIB-based circuit edition
    - ✓ **Layout edition** and **rerouting**
    - ✓ **Security disabling**
  - ✓ Laser-based circuit edition

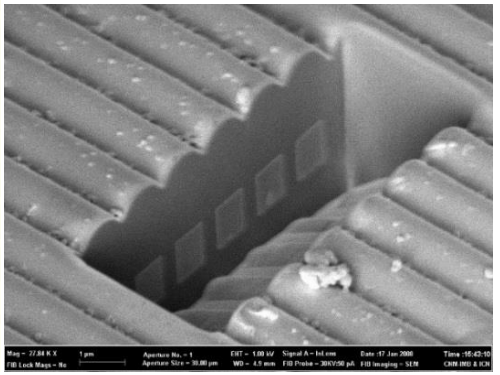








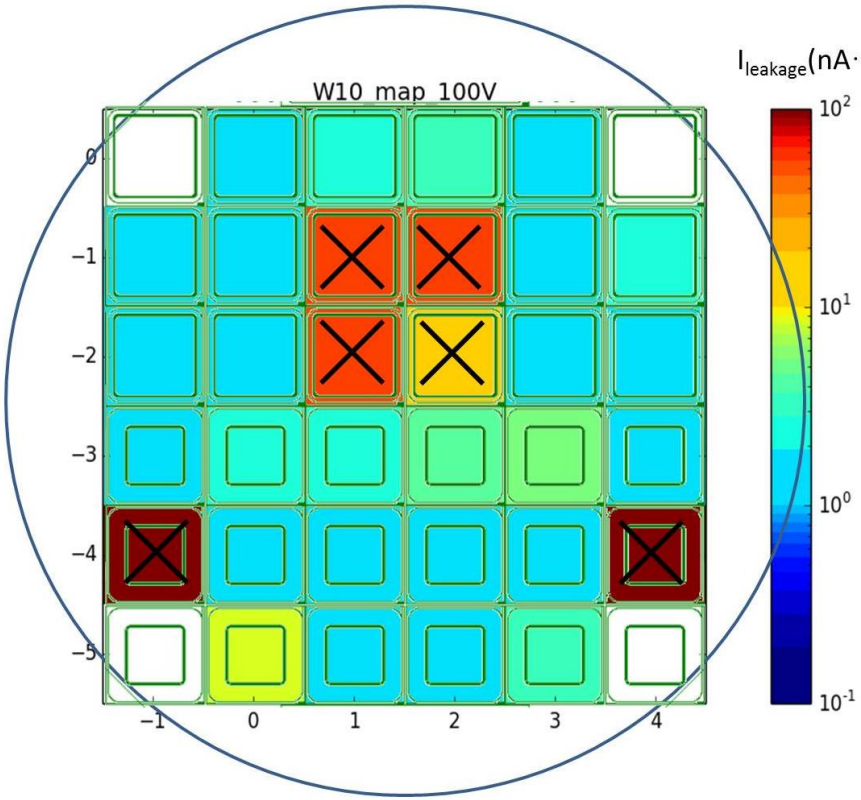




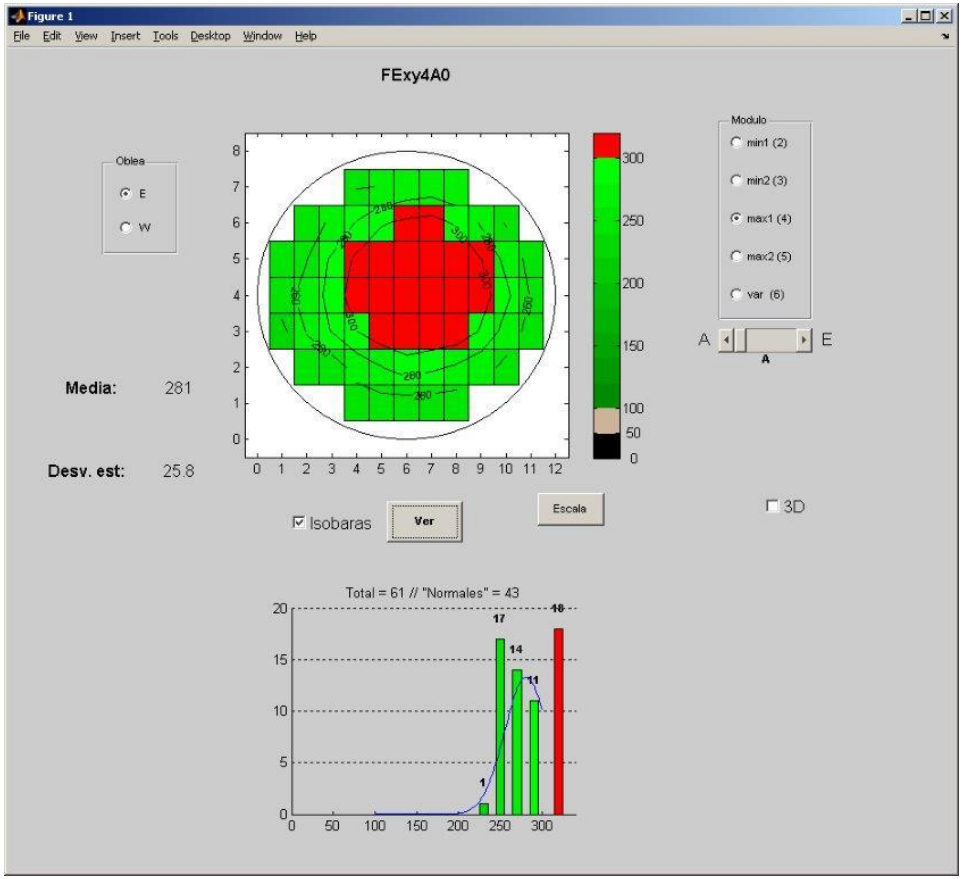
Automatic Electrical Characterization

- **Fast and efficient automatic electrical characterization set-up**
  - ✓ **Automatic 6” wafer probe station** with specific test needles adapted to the layout to be measured (**Custom probe cards**)
  - ✓ **Agilent E5270B Precision Measurement Mainframe**. ±100 V, ±100 mA (minimum resolution of 2 µV, 10 fA).
  - ✓ **HP4284 LCR Meter**. 20 Hz to 1 MHz ±0.01%
  - ✓ **Control Software** for table movement and test and data acquisition.
- **Automatic measures**
  - ✓ **Electrical Parameters:** I(V), C(V), parametric characterization, etc.
  - ✓ **Technological Characterization**: If specific test structures are implemented: sheet resistance, contact resistance, dielectric capacitances, etc.

Automatic Electrical Characterization



Wafer mapping and data analysis with custom developed tools
(Matlab & Python)



Thank you for your attention !!!!