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# New Technological Capabilities at CNM

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In this talk, we will present some technological capabilities that could be of interest for the RD50 community. In this sense, the first results from new PiN diodes integrated on 6-inch N-silicon wafers will be shown. To perform this 6-inch technological process we have upgraded the standard CNM 4-inch process to the new wafer size. Additionally, we will describe the works performed to increase the layout edition capabilities to achieve a full-sensor automatic layout generation using Python. Finally, we will present a description of the technological and electrical characterization resources for silicon detectors at our labs, in particular we will explain our Reverse Engineering procedures that allow a deeper insight on the physical and geometrical properties of the fabricated devices.

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