Design and Fabrication of an Optimal Peripheral Region for the LGAD

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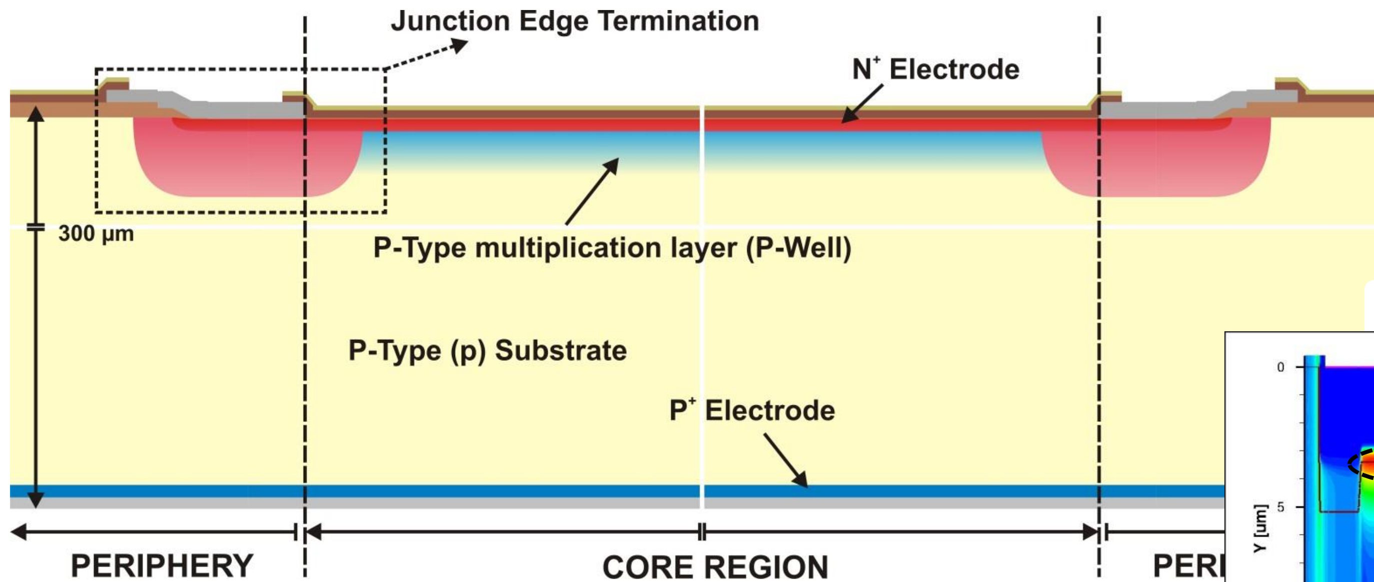
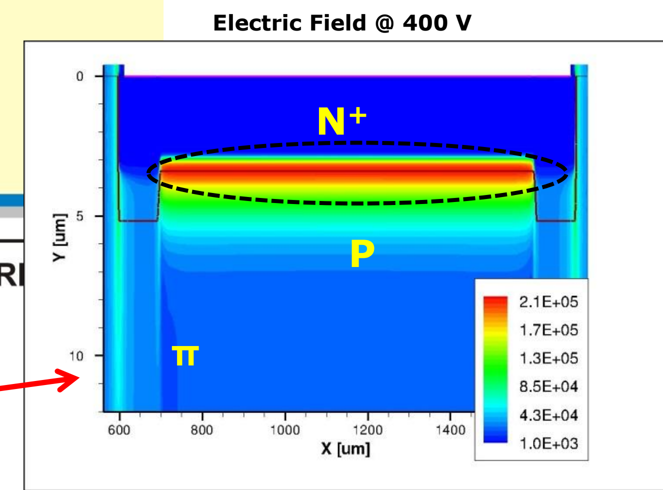
This work is supported by RD50 Collaboration

Talk Outline

- **Critical aspects of the LGAD design**
- **Optimization of the multiplication junction**
- **Optimization of the junction edge termination**
- **Optimization of the periphery**
- **New production run**
- **Conclusions**

Critical aspects of the LGAD design



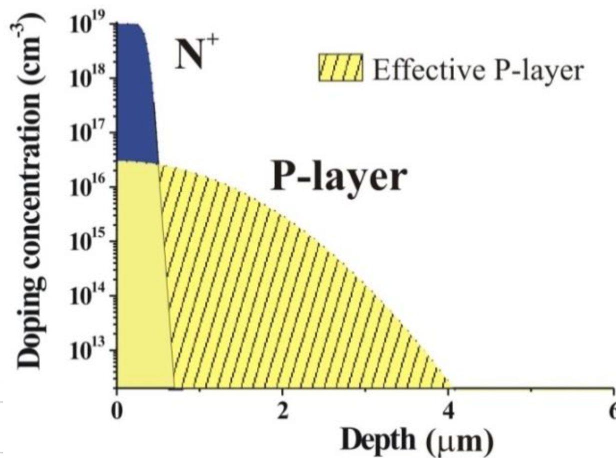


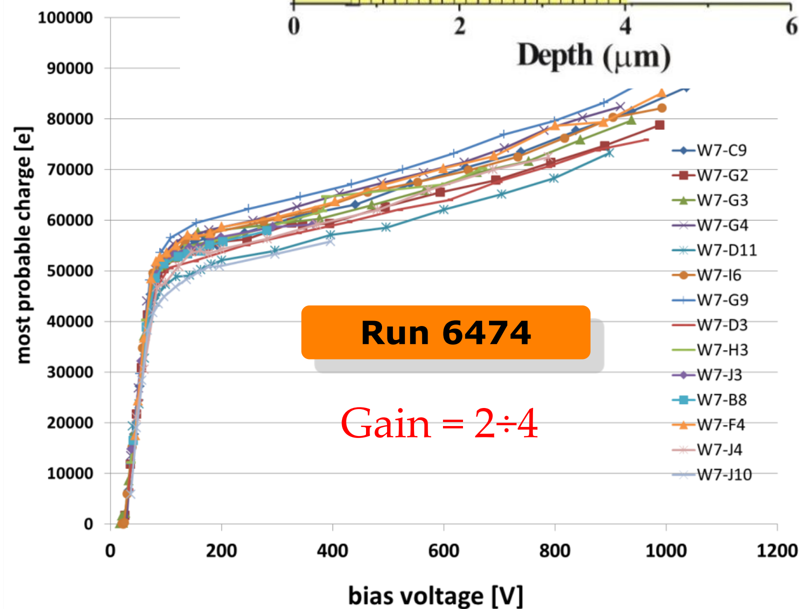
- **Core Region** → Uniform electric field, high enough to activate mechanism of impact ionization (multiplication)
- **Termination** → High electric field confined in the core region
- **Periphery** → (Dead region) Charges should not be collected. Reduction of the leakage currents

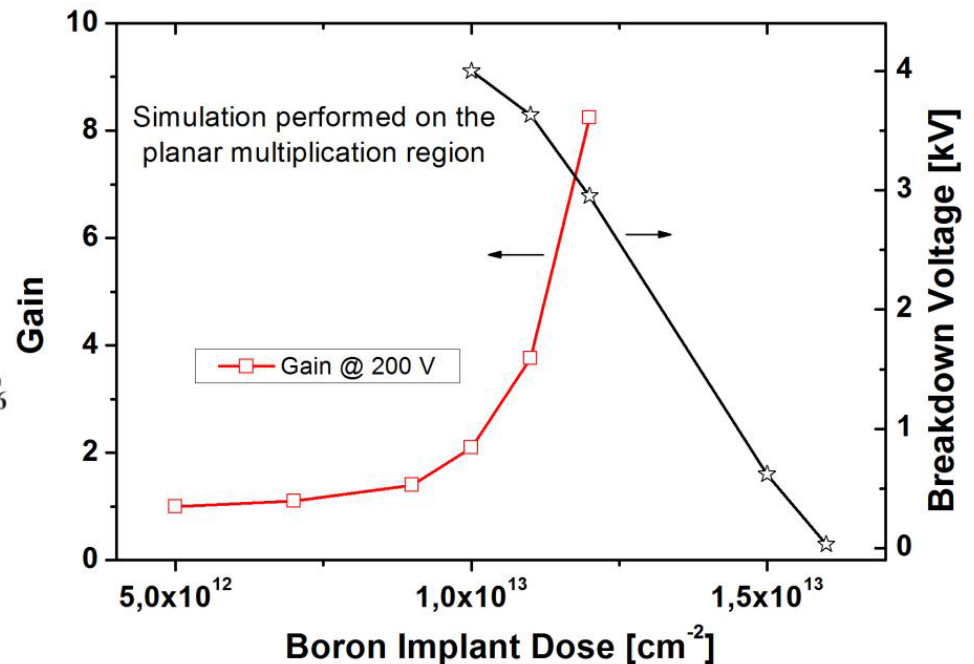
$$V_{BD}|_{\mathbf{Termination}} \gg V_{BD}|_{Central}$$

Core region: Optimization of the Multiplication layer

- **Doping profile** of the P and N^+ diffusions is crucial



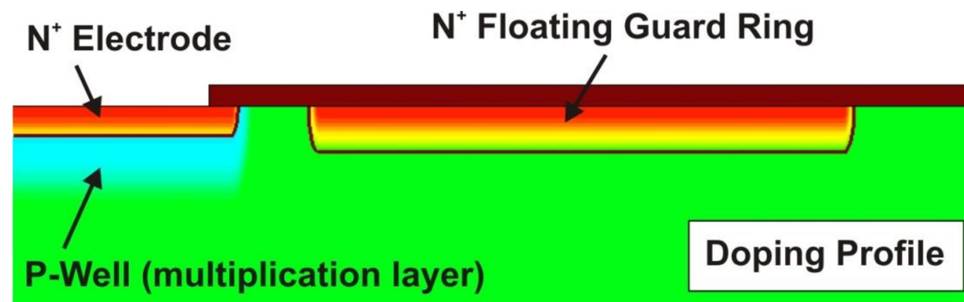


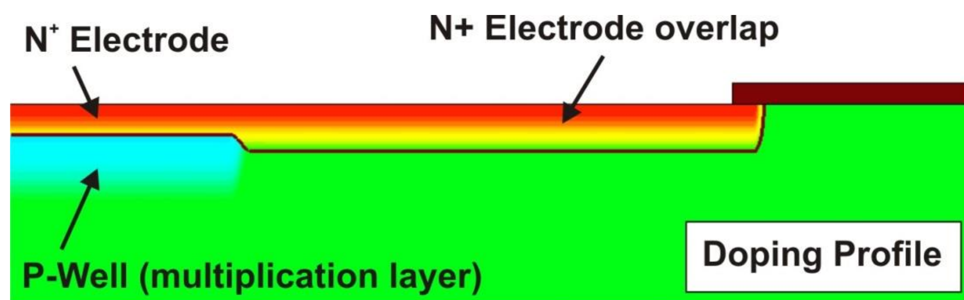


- Wafers have **different gains**:
  - Good uniformity of gain over the wafer.

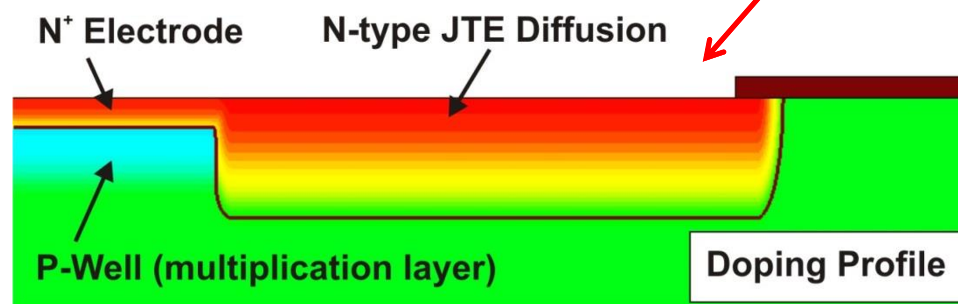
Optimization of the Junction Edge Termination

- **Three Requirements:**
  - $V_{BD_Core(1D)} < V_{BD_Termination}$
  - Electric Field Uniformity
  - Compatible with segmentation





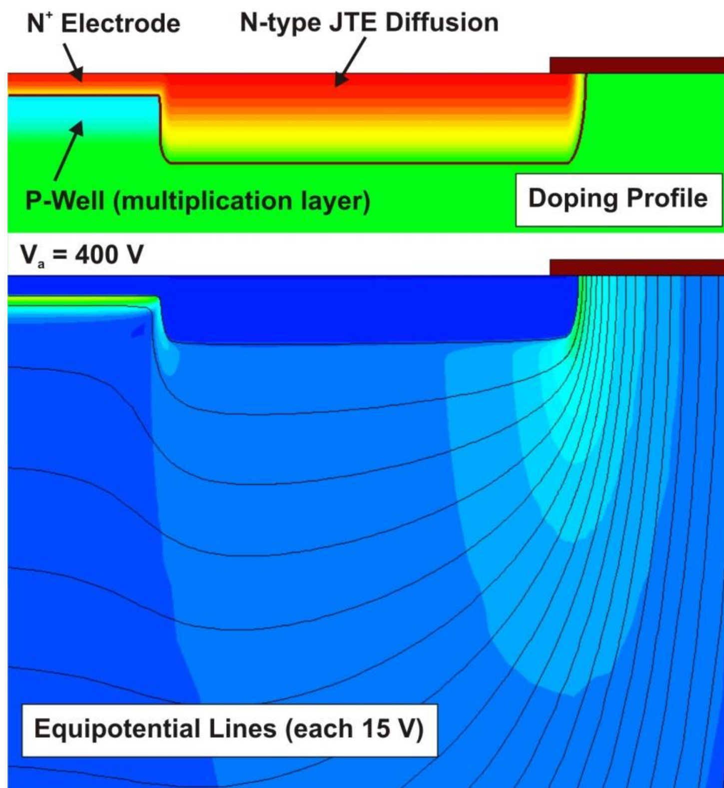
3 Designs have been analyzed

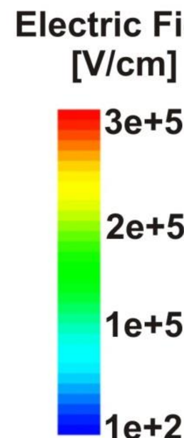


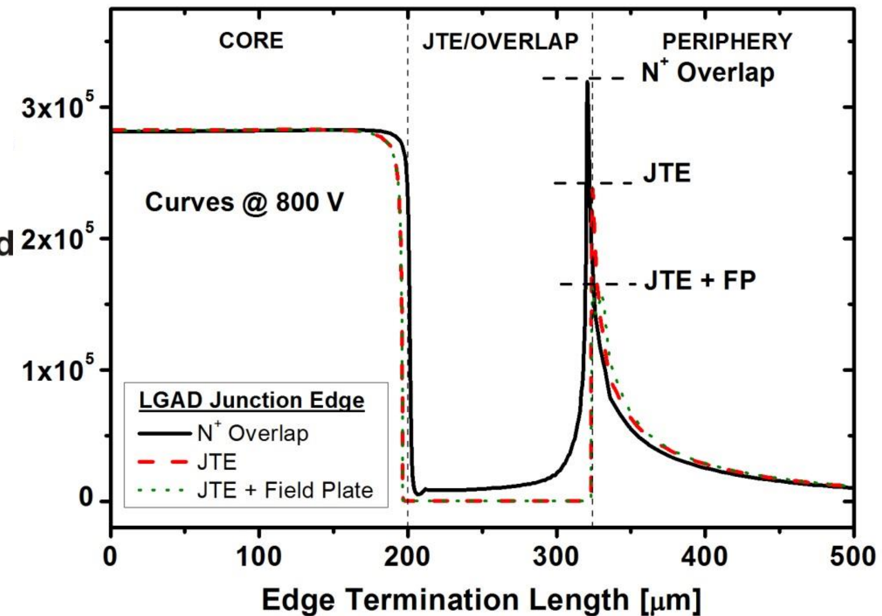
Junction Edge Termination: Deep N-type diffusion

- The electric field peak is reduced at the JTE curvature
- The highest electric field value is located at the main junction (1D)
  → multiplication control

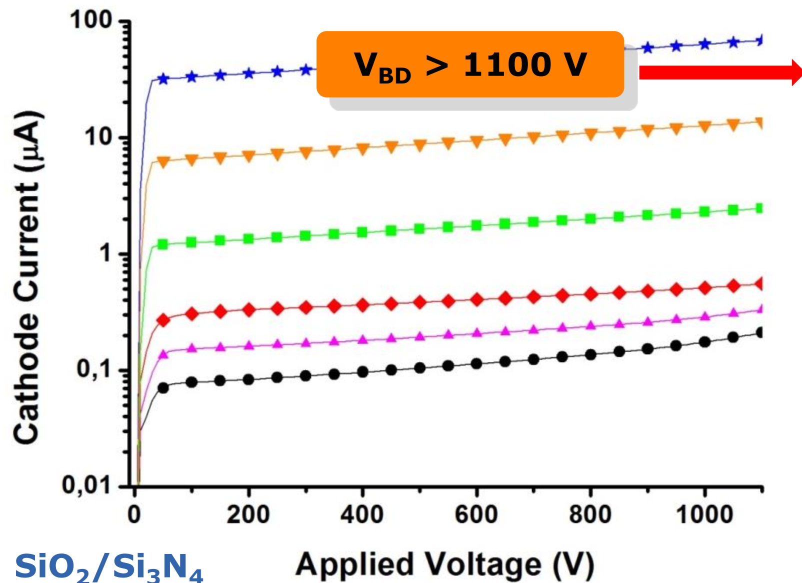
Ec value at the JTE junction is not as low, so the breakdown can be localized at the main junction



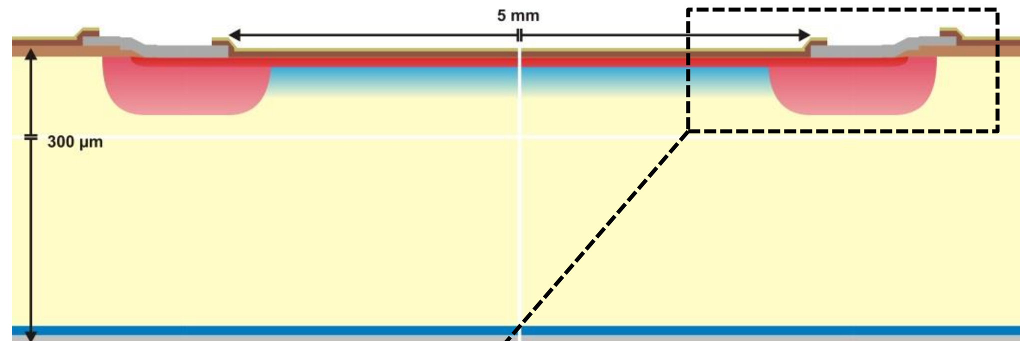




Junction Edge Termination: Deep N-type diffusion



Runs 6474 & 7062



SiO_2/Si_3N_4 Passivation

Metal

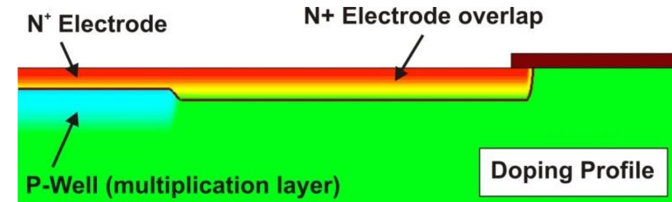
20um

P-type multiplication layer

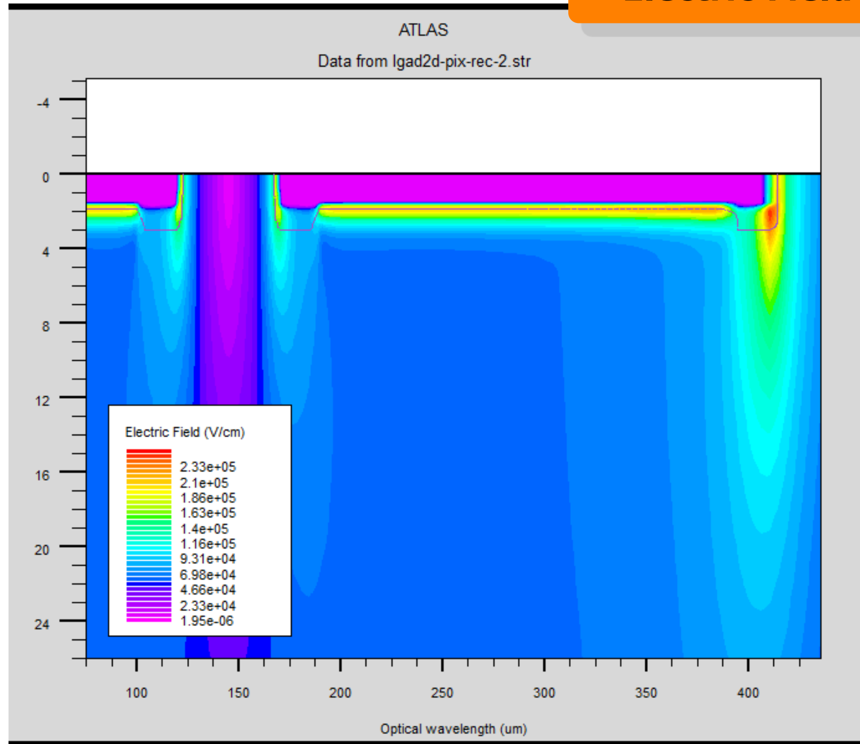
N-Type Diffusion (JTE)

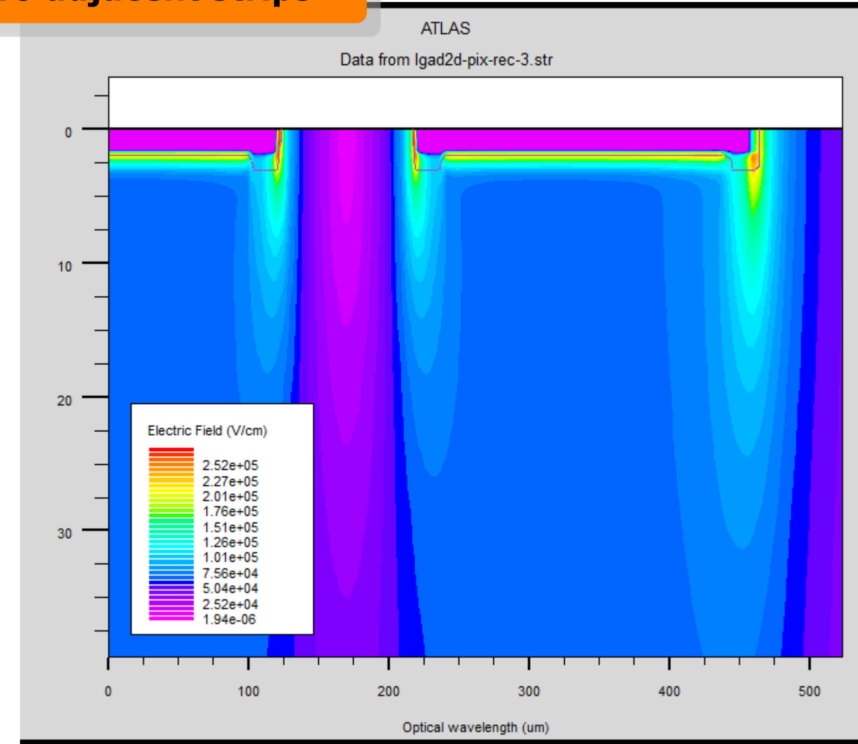
Junction Edge Termination: Segmented devices

- Deep N-type diffusion works properly for *pad* devices
- In segmented devices N+ electrode extension seems more convenient



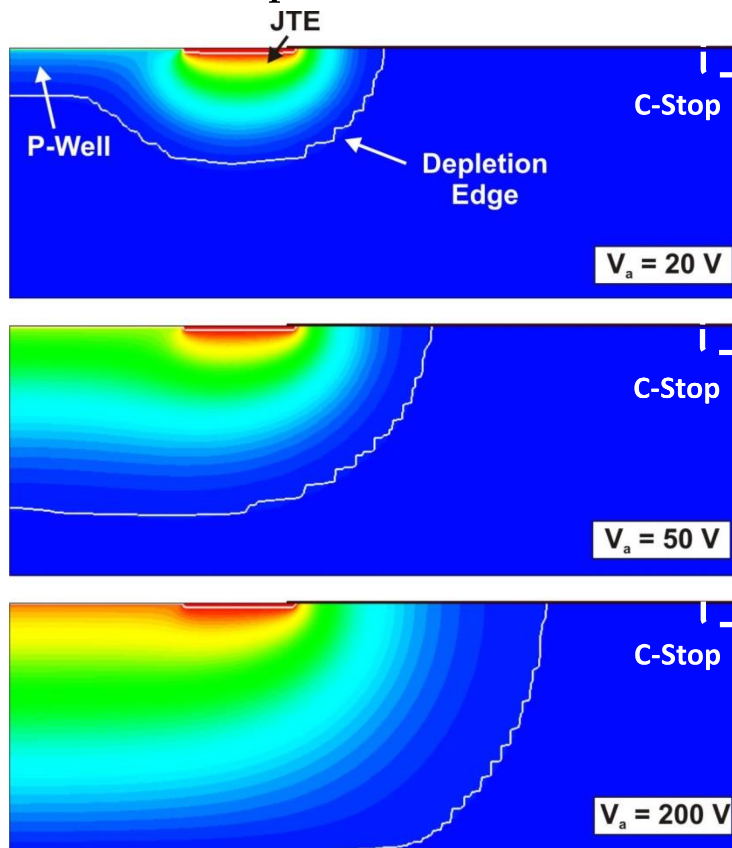
Electric Field in two adjacent strips



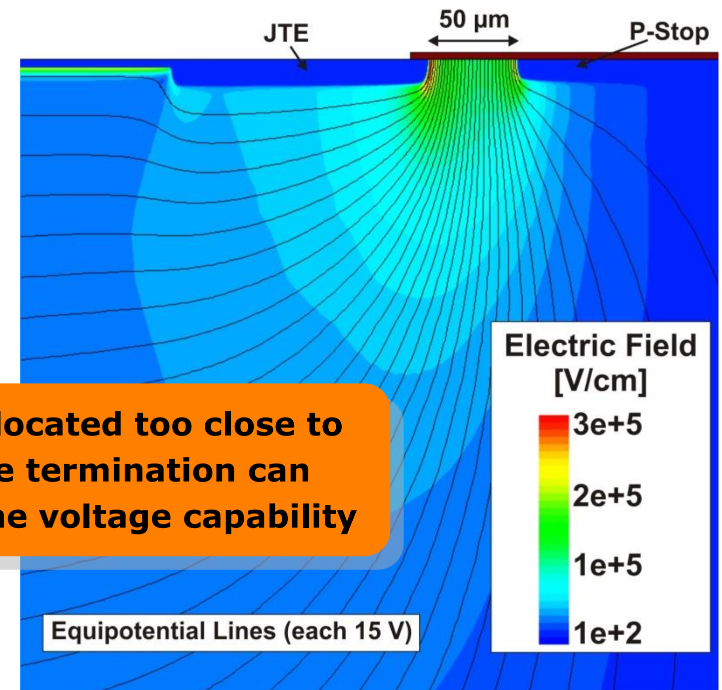


Design of the Device Periphery

- **Peripheral region should ensure the voltage capability as well as limiting the leakage current.**
  - After the full (vertical) depletion is reached, a fast lateral depletion of the lowly doped substrate takes place.



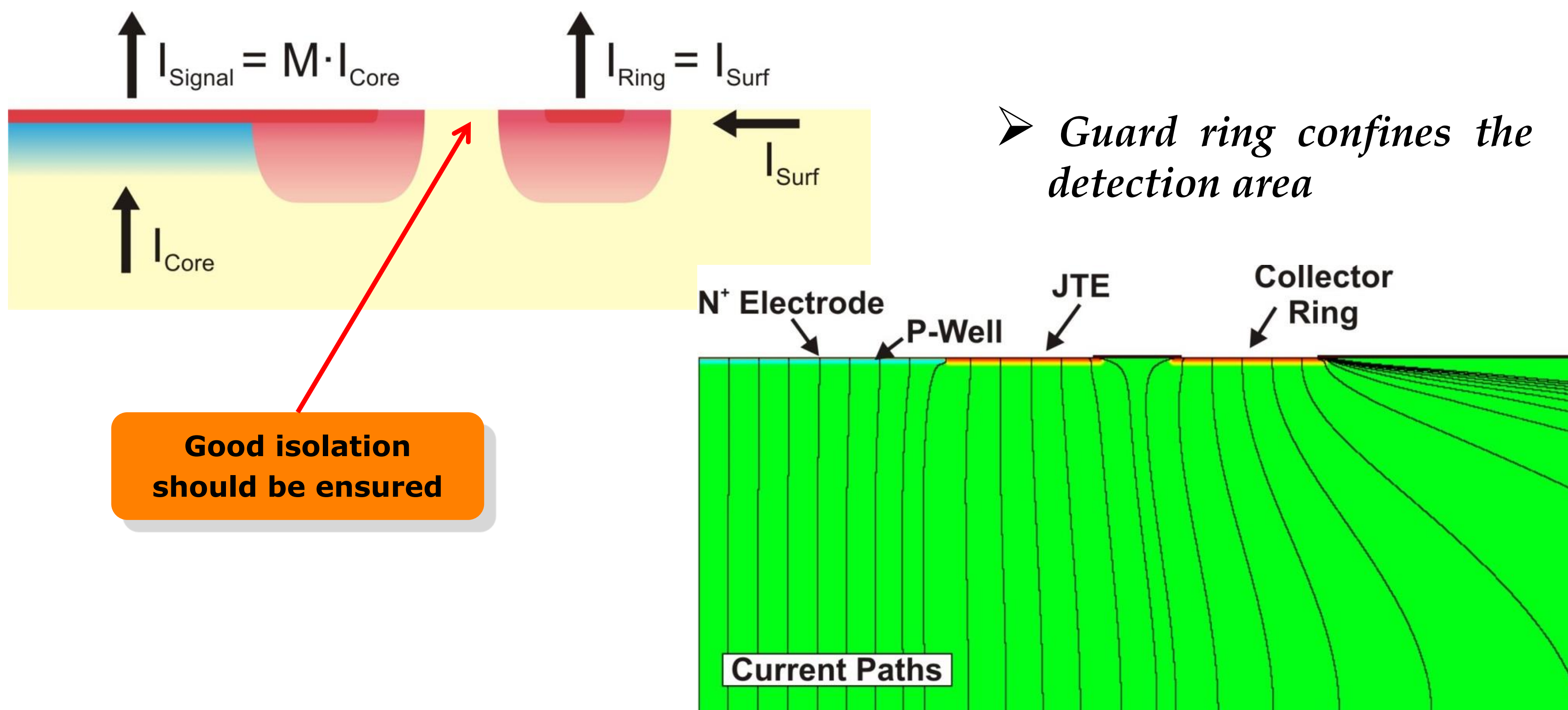
- *A deep P+ diffusion (C-Stop) is needed in the die periphery to avoid the depletion region reaching the unprotected edge*



A C-Stop located too close to the edge termination can degrade the voltage capability

Optimization of the periphery: Guard Ring

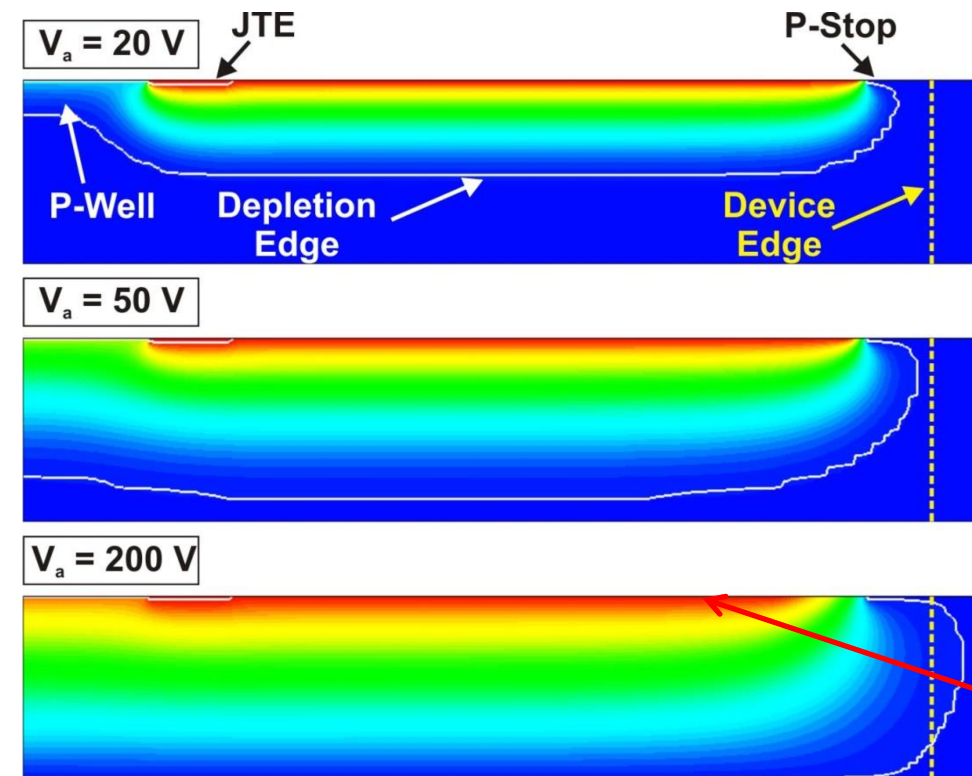
- **Biased guard Ring around the detection region.**
  - The ring is independently biased to extract the surface component of the current
  - Voltage capability is preserved (same curvature as JTE)

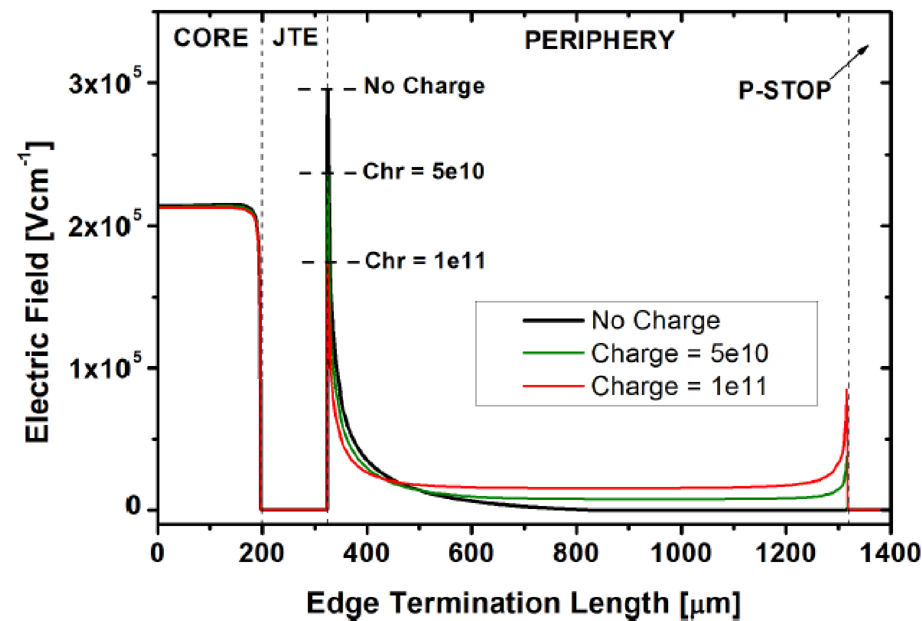


- *Guard ring confines the detection area*

Optimization of the periphery: Positive oxide charges

- **Field oxides grown in wet conditions (H_2 + O_2) typically have a positive charge density in the range of 5e10 cm^{-2}**
  - Surface inversion of the substrate and modification of the depletion dynamics.

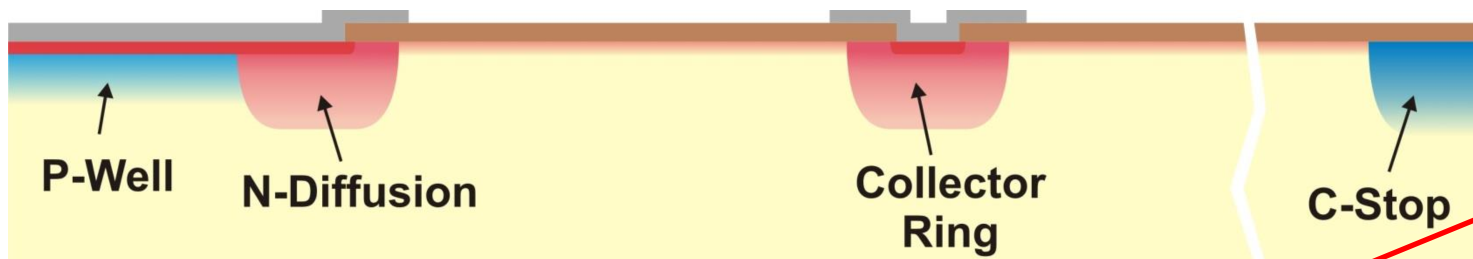




Surface leakage currents

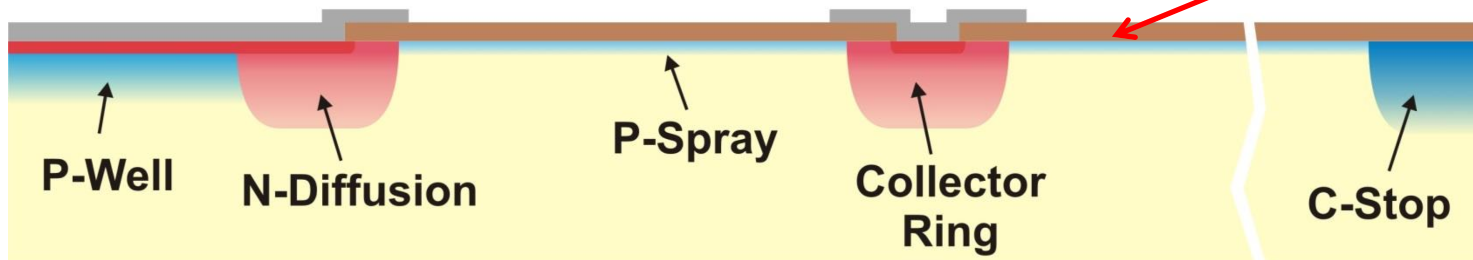
Optimization of the periphery: Strategies

- **Positive oxide charges (radiation induced or technologically originated) induce surface inversion of the substrate → Current path towards the collector electrode.**



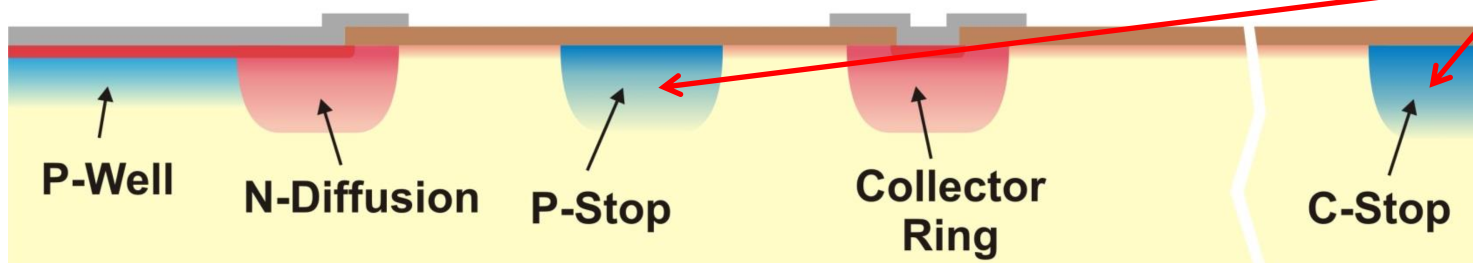
Boron blanket implant

- *P-Spray: Counteracts the inversion*



- *P-Stop: cuts the current path off*

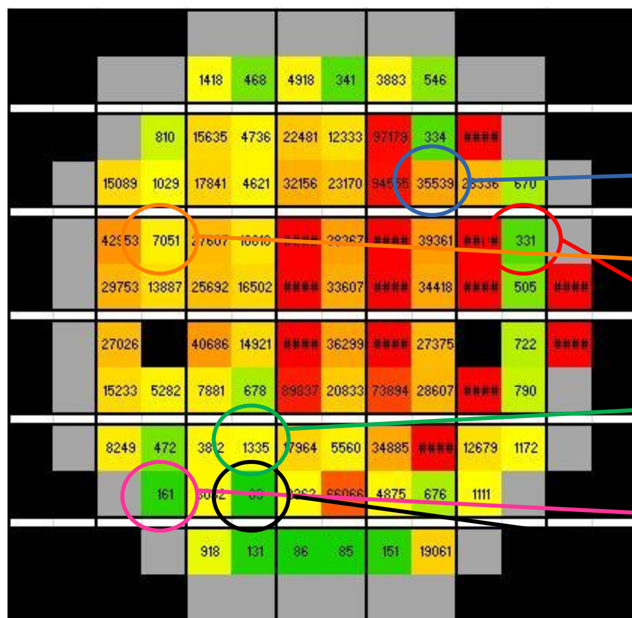
Same implant



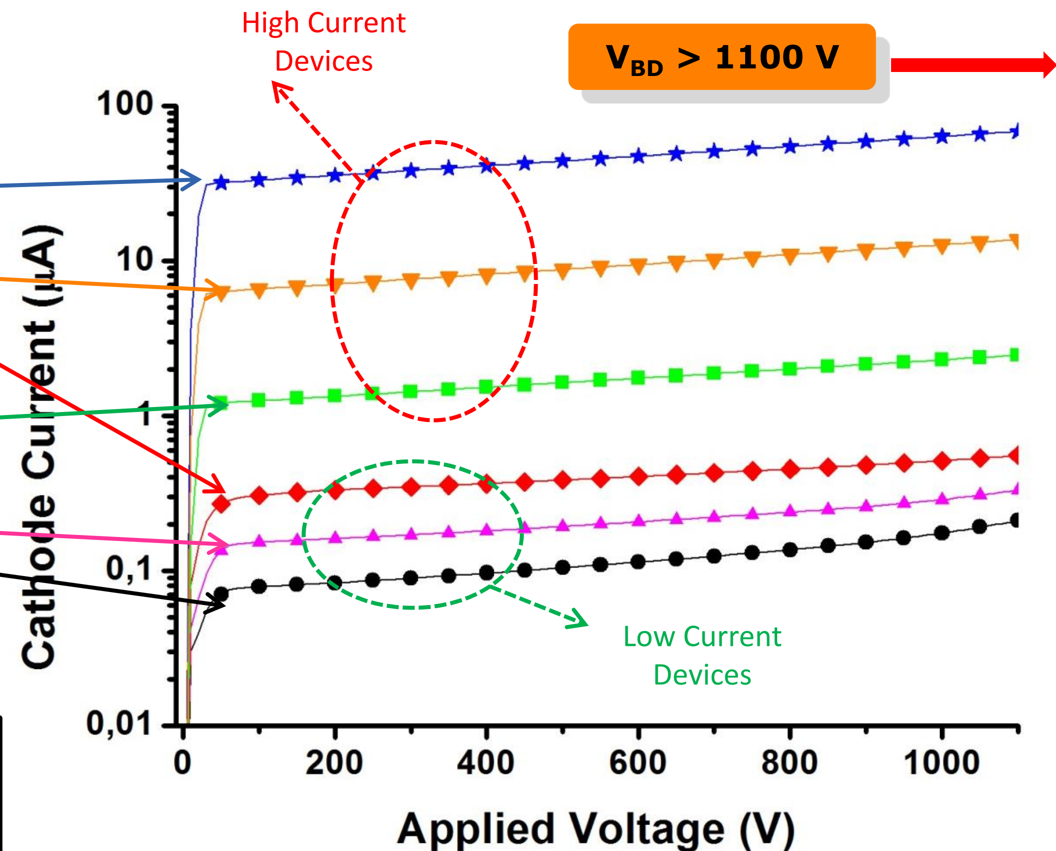
Electrical Characterization: Yield

Run 6474

- ✓ High Voltage Capability (Breakdown > 1100 V) in all wafers
- ✗ Leakage current varies from some 10 nA to more 100 μA in devices within the same wafer

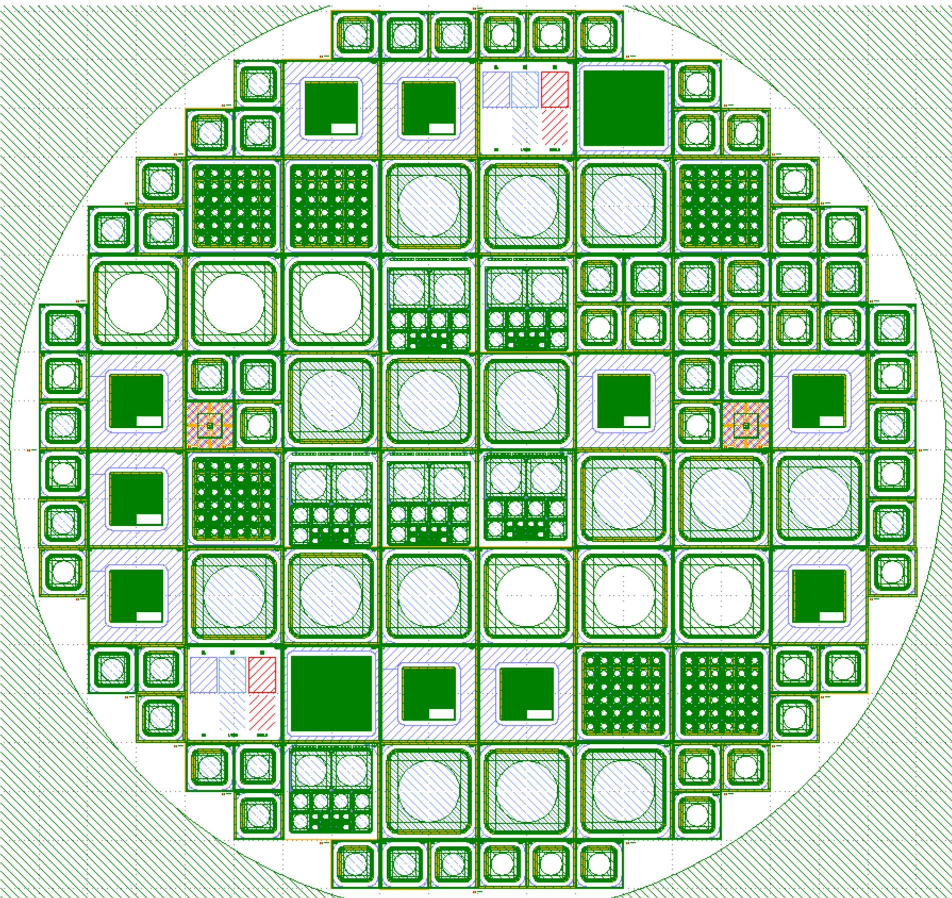


LGAD Wafer (W8 – High Boron Implant)

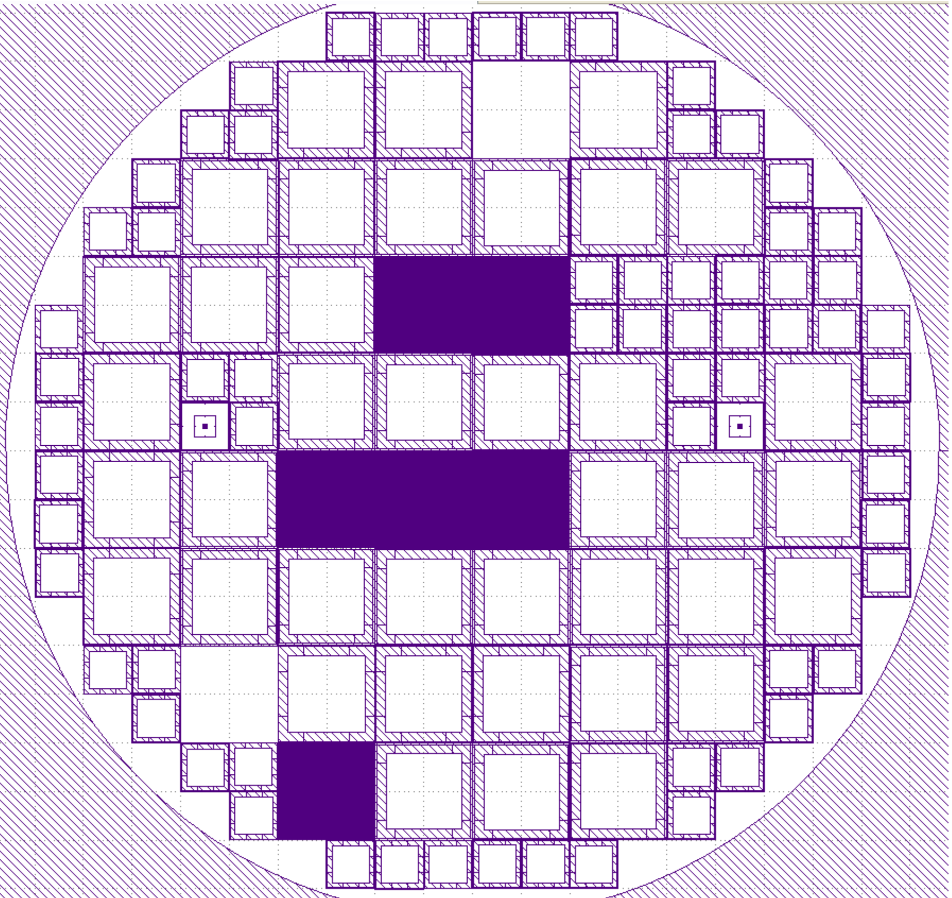


Guard Ring is short-circuited with N^+ electrode (inefficient P-Spray)

New Fabrication Run



Top Distribution



Back Metallization

New Fabrication Run

- 9 LGAD Pad Detectors
  - ✓ 3 (8 x 8 mm multiplication area)
  - ✓ 6 (3 x 3 mm multiplication area)
- 9 PiN Detectors
  - ✓ 3 (8 x 8 mm active area)
  - ✓ 6 (3 x 3 mm active area)
- 4 LGAD pStrips Detectors
  - ✓ 32-160-50-06-24
  - ✓ 32-160-62-06-12
  - ✓ 64-80-10-06-24
  - ✓ 64-80-22-06-12
- 2 PiN pStrips Detectors
  - ✓ 32-160-50-06-24
  - ✓ 64-80-10-06-24
- 1 FEI4 compatible pStrip Detector

IJS Ljubljana

- 1 Pixelated LGAD Detector (6 x 6 pixels)
- 1 Pixelated PiN Detector (6 x 6 pixels)

INFN Torino

- 3 LGAD for Timing Applications
  - ✓ 200 um to chip edge
  - ✓ 250 um to chip edge
  - ✓ 800 um to chip edge

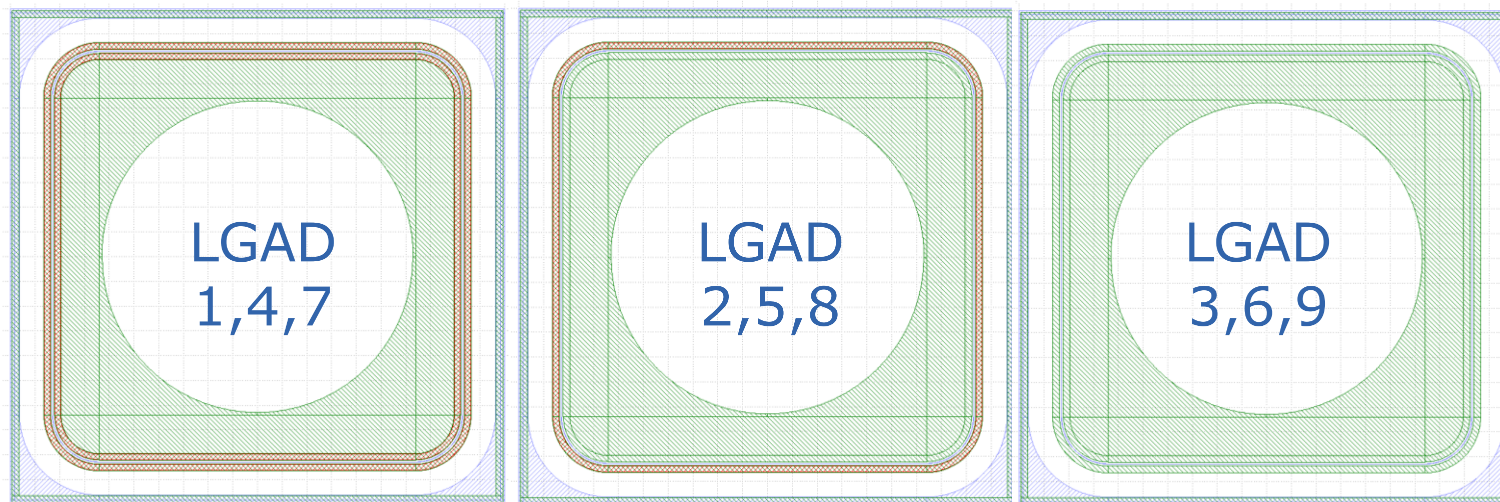
LAL Orsay

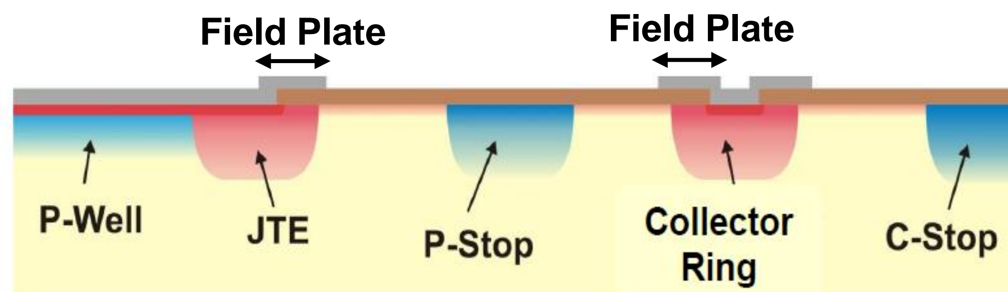
- 1 Specific Test Structure (SPR,SIMS,XPS)

❑ **113 Structures**

- **47 (10 x 10 mm, total area)**
- **66 (5 x 5 mm, total area)**

New Fabrication Run: LGAD & PiN *pad* Detectors





- LGAD & PiN Pad Detectors
  - ✓ Multiplication Area
    - 8 x 8 mm (Type 1, 2, 3)
    - 3 x 3 mm
  - Termination:
    - * P-Stop + N-Guard Ring (Type 3, 6, 9)
    - * P-Stop + N-Guard Ring with JTE (Type 2, 5, 8)
    - * JTE + P-Stop + N-Guard Ring with JTE (Type 1, 4, 7)
    - * Field Plate 10 µm, 0 µm (Type 7, 8, 9)

New Fabrication Run: LGAD & PiN *strip* Detectors

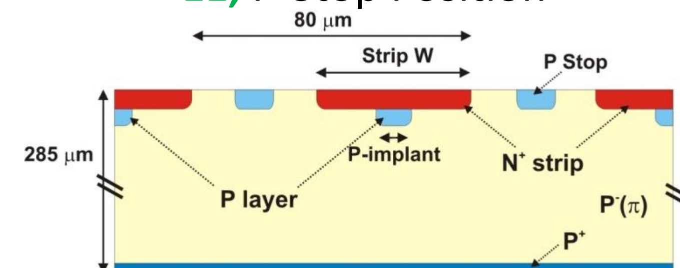
32.160.50.06.24

64.80.10.06.24

32.160.62.06.12

64.80.22.06.12

- 4 LGAD pStrips Detectors
  - ✓ 32-160-50-06-24
  - ✓ 32-160-62-06-12
  - ✓ 64-80-10-06-24
  - ✓ 64-80-22-06-12
- 2 PiN pStrips Detectors
  - ✓ 32-160-50-06-24
  - ✓ 64-80-10-06-24
- Key Legend
  - ✓ AA-BB-CC-DD-EE
  - ✓ AA, Channels Number
  - ✓ BB, Pixel Size
  - ✓ CC, Multiplication Width
  - ✓ DD, P-Stop Width
  - ✓ EE, P-Stop Position



LGAD and PiN Pixelated Detectors

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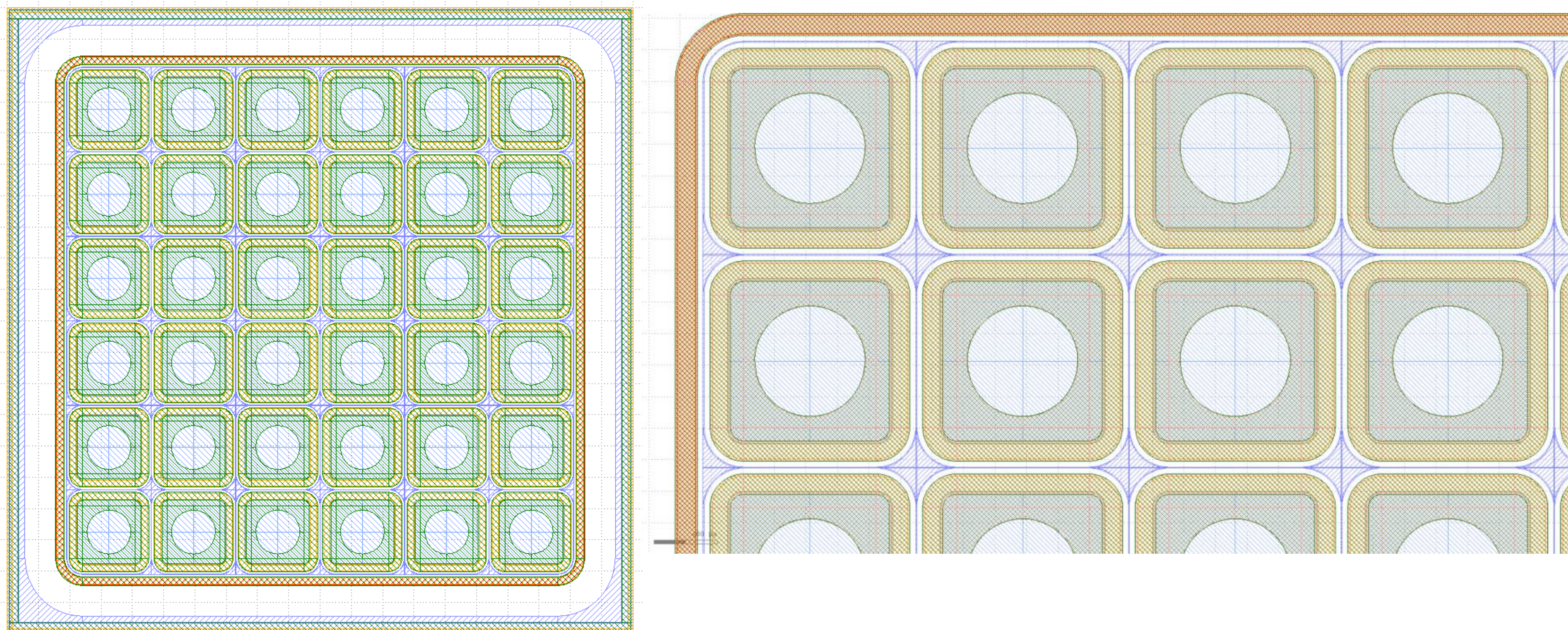
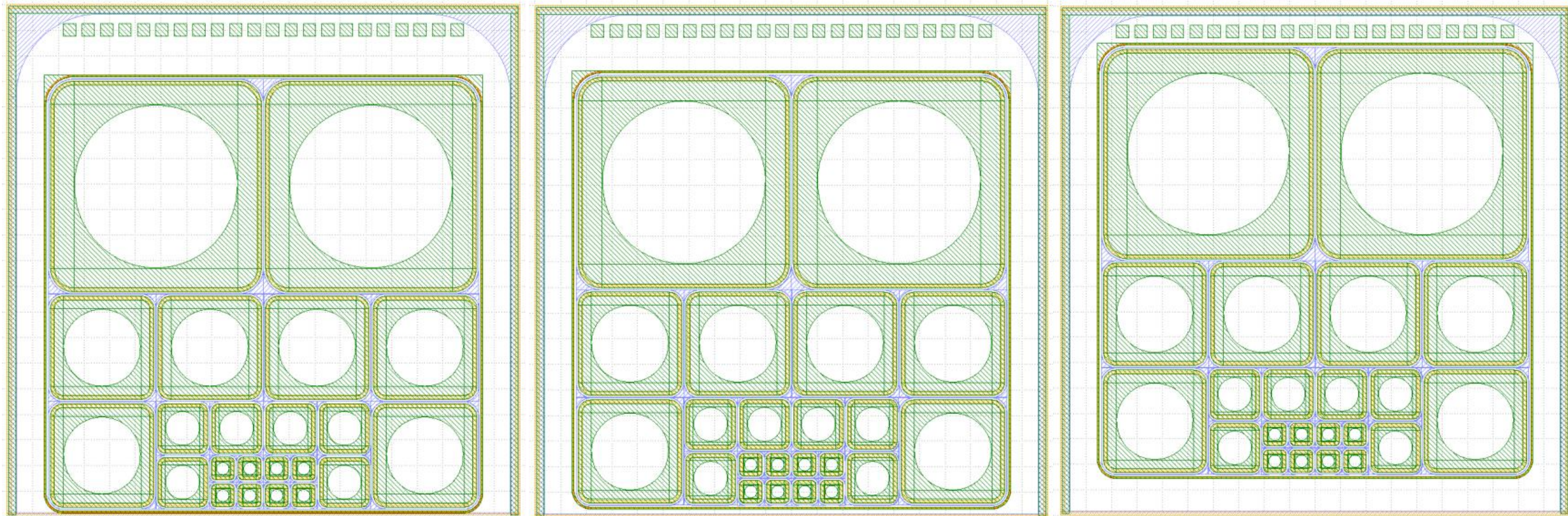


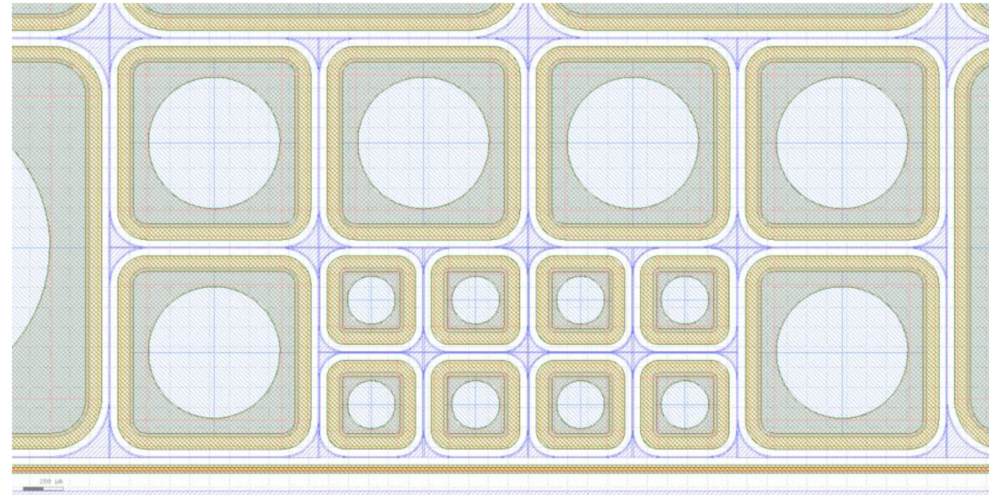
- 1 Pixelated LGAD Detector (6 x 6 pixels)
- 1 Pixelated PiN Detector (6 x 6 pixels)

LGAD for Timing Applications

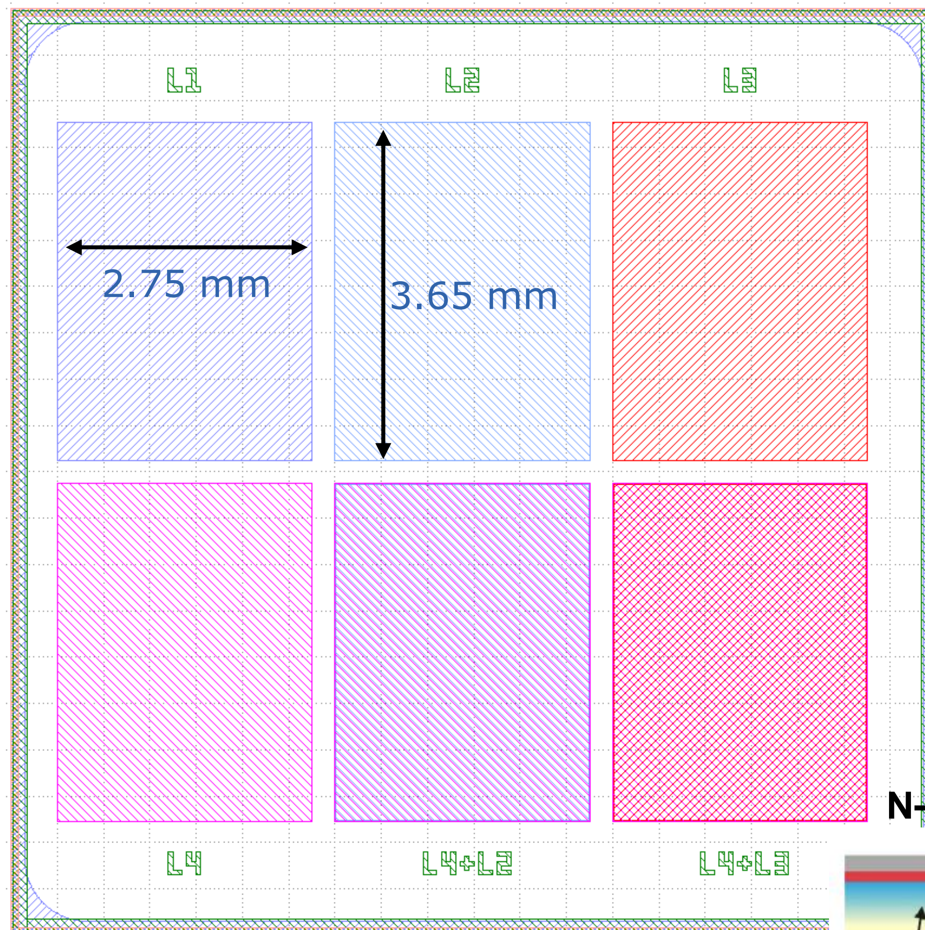


INFN Torino

- 3 LGAD for Timing Applications
  - ✓ **200 um** to chip edge
  - ✓ **250 um** to chip edge
  - ✓ **800 um** to chip edge

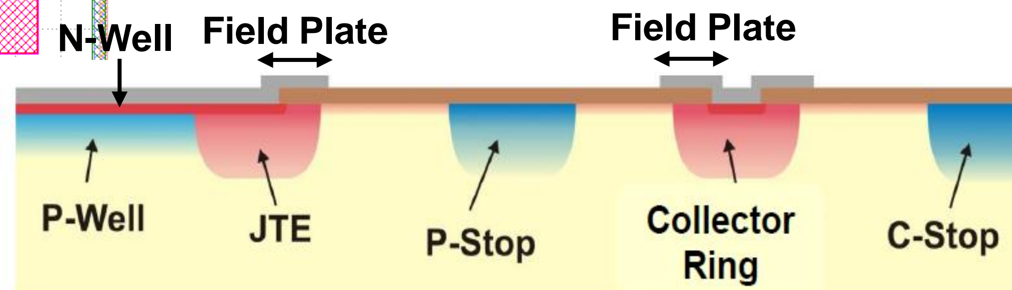


Specific Test Structure. SRP, SIMS, XPS



LAL Orsay

- L1 P-Stop, C-Stop Well
- L2 P-Well (P Multiplication)
- L3 JTE
- L4 N-Well
- L4 + L2 N-Well over P-Well
- L4 + L3 N-Well over JTE



Conclusions

- Optimization of the LGAD peripheral region is crucial for the detector performance
  - Edge termination techniques confine the high electric field into the multiplication area and give voltage capability to the detector
  - Structures within the peripheral region avoid high leakage currents and degradation
- Deep N-diffusion termination technique has proved good performance
- P-Spray technique has shown poor effectiveness
- New production run at the IMB-CNM include *pad* and segmented (*strip* and *pixel*) designs with an optimized peripheral region based on the P-Stop technique.
- 300 μm-thick prototypes with the new mask set is now in production. A 200 μm-thick run is on going.

Thank you

Questions?

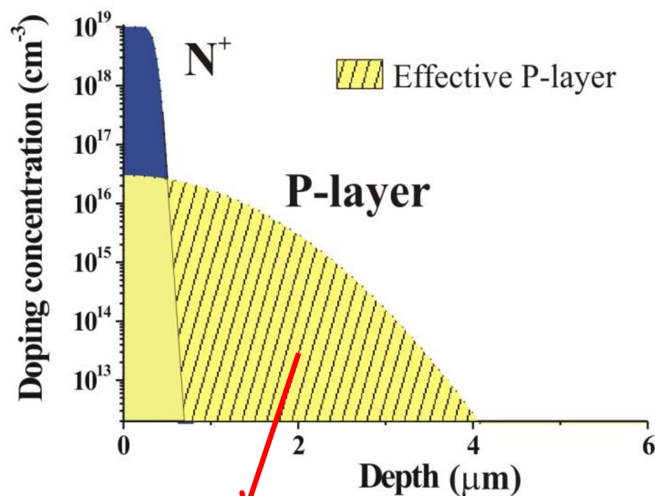
Back up Slides

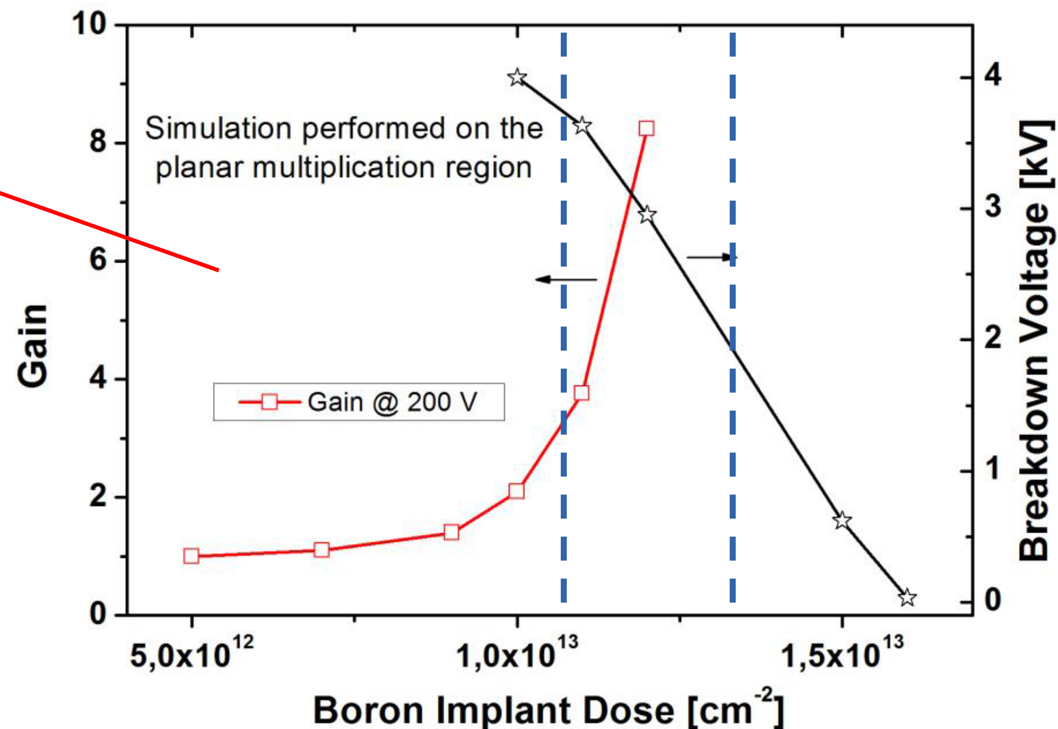
Just in case

Optimization of the Multiplication layer

- P-type multiplication layer determines both Gain and Breakdown

✓ Higher Boron implant Dose:
- Higher Gain
- Lower Breakdown

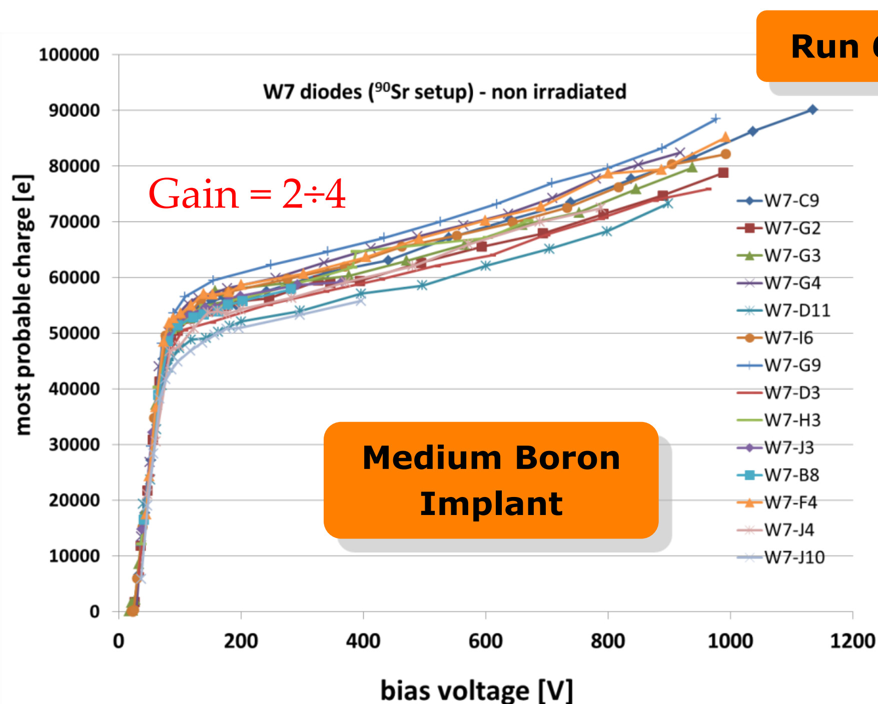


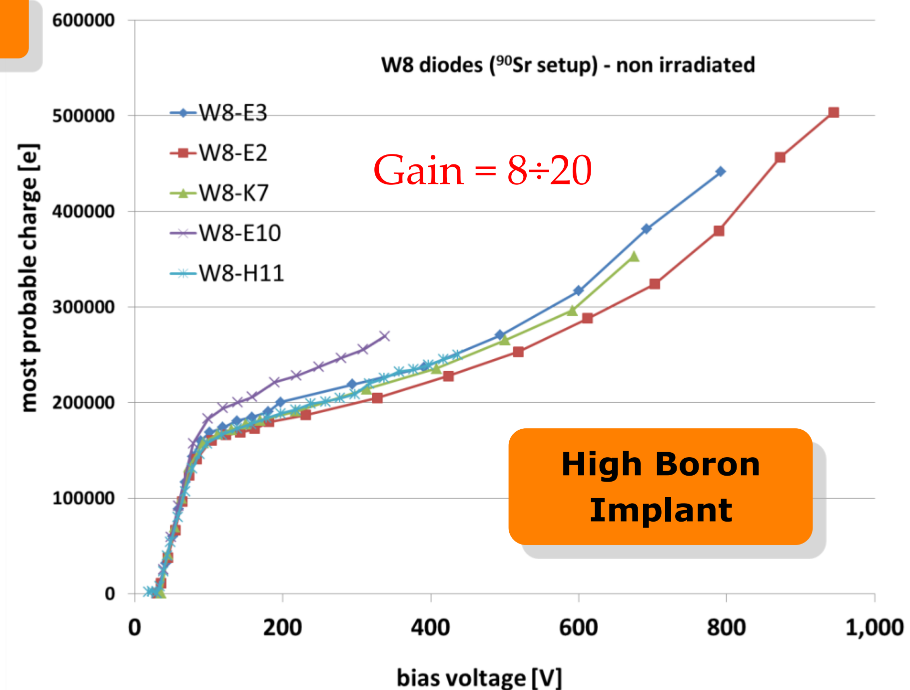


- *Effective charge and doping value at the junction determine the Gain*

Small variations in the Boron implant dose ($\sim 2 \times 10^{12}$ at/cm²) lead to large changes in Gain and Breakdown values

Charge Collection Measurements: Electrons (*mips*)



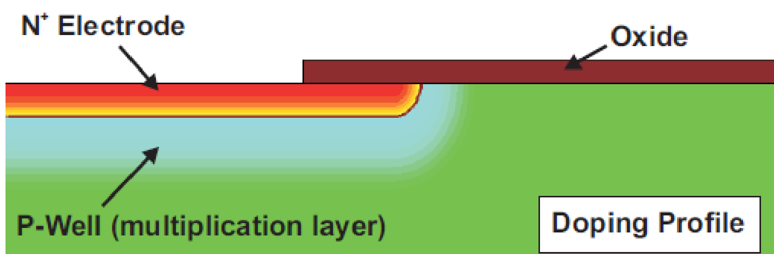


G. Kramberger, 24th RD50 Workshop, Bucharest

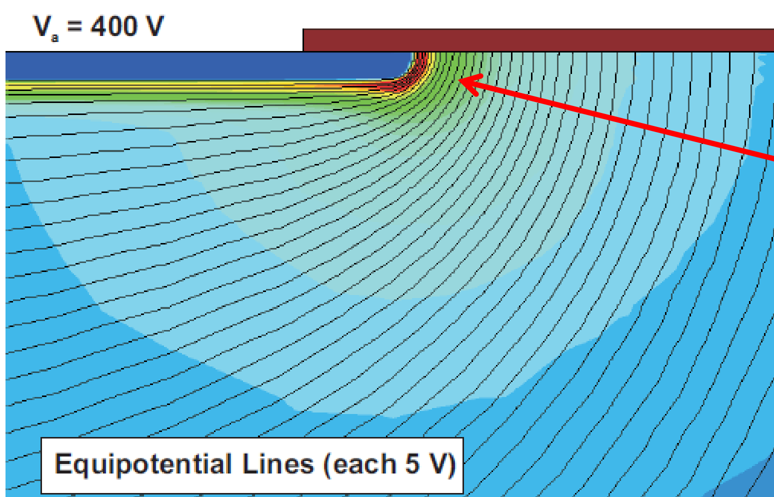
- LGAD diodes with different values of the doping dose of the p-type multiplication layer.
  - W7 → 1.6×10^{13} cm^{-2}
  - W8 → 2.0×10^{13} cm^{-2}
- Wafers have **different gains**:
  - Good uniformity of gain over the wafer.
  - Very good stability of some diodes up to >1000 V.

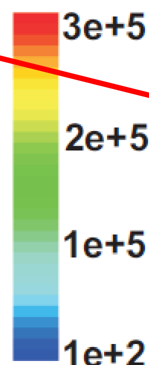
Edge Termination: Why is needed?

- **The N^+ shallow contact and the P-multiplication layers have to be locally created with a lithography mask**
  - ✓ **The electric field at the curvature of the N^+/P junction is much higher than that of the plane junction (where Gain is needed)**
  - ✓ **Avalanche at the N^+/P curvature at a very low reverse voltage (premature breakdown)**



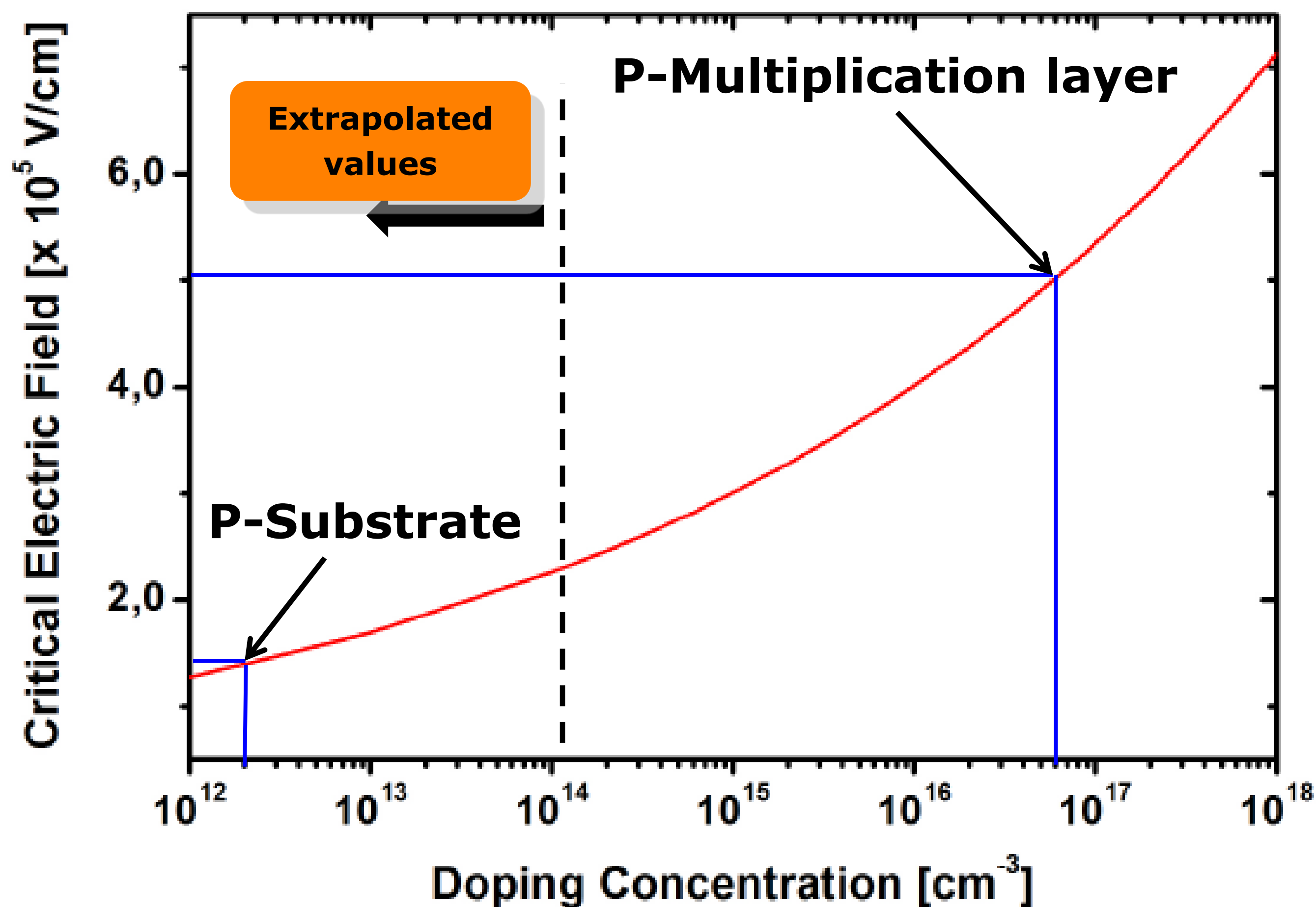
Shallow N^+ and P-multiplication layers self aligned





High electric field peak at the curvature

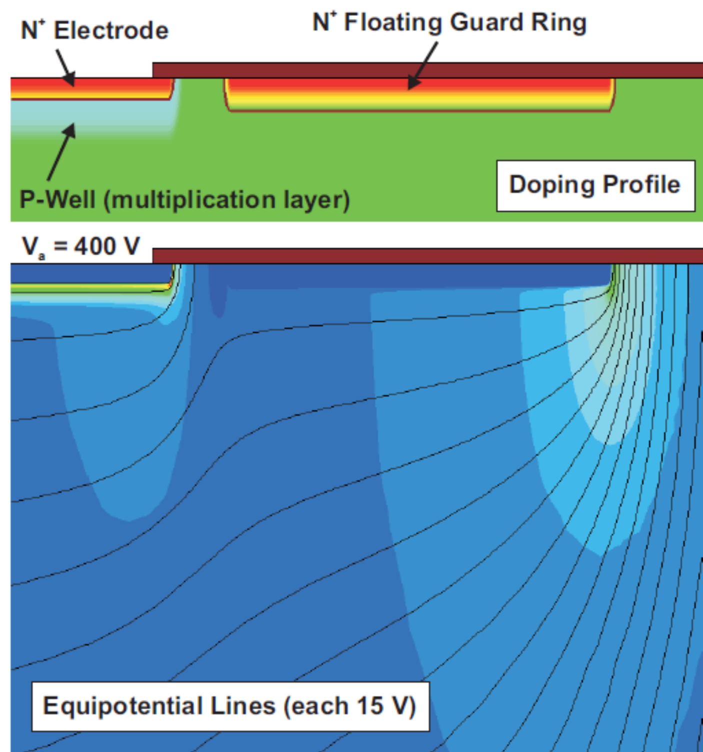
Design of the Edge Termination: Critical Electric Field



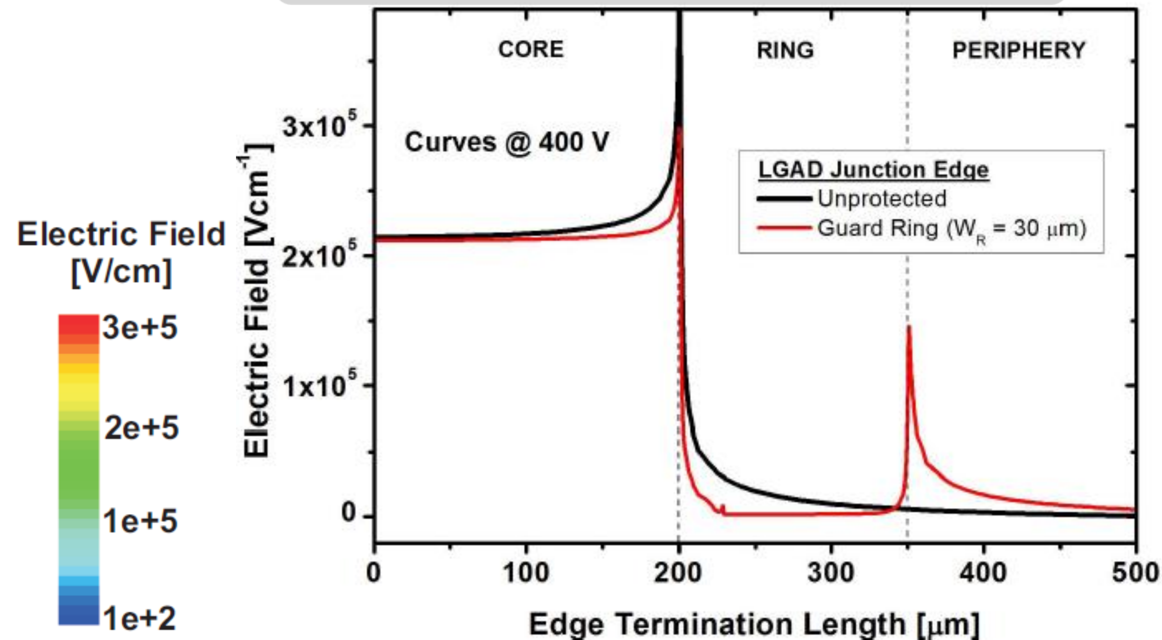
B. Jayant Baliga (2008): ***Fundamentals of Power Semiconductor Devices***

Junction Edge Termination: Floating Guard Ring

- **The N+ shallow diffusion is used to implement a floating guard ring.**
  - The lateral electric field distribution is smoothed leading to two peaks (main junction and floating guard ring)
  - The electric field peak and the risk of avalanche breakdown at the curvature of the main junction is reduced. Optimization of the guard ring location is needed.

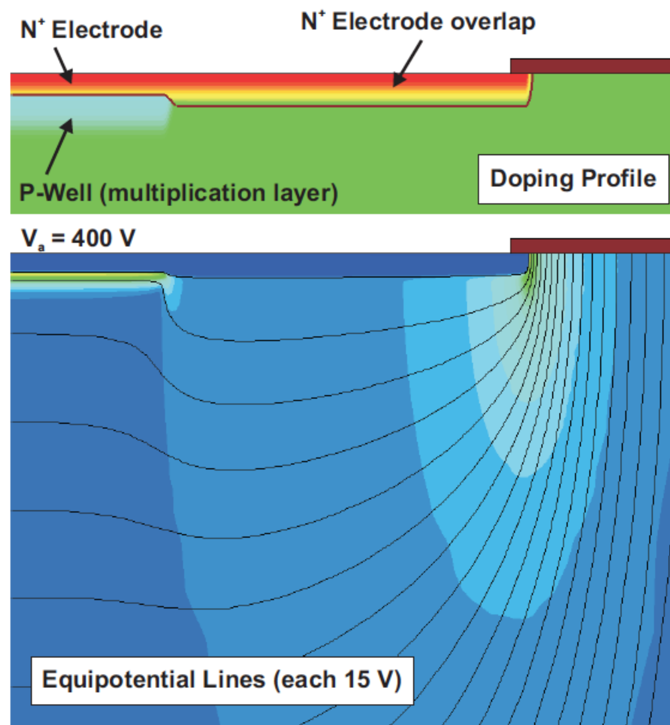


The lower Ec value at the ring junction can lead the termination to breakdown

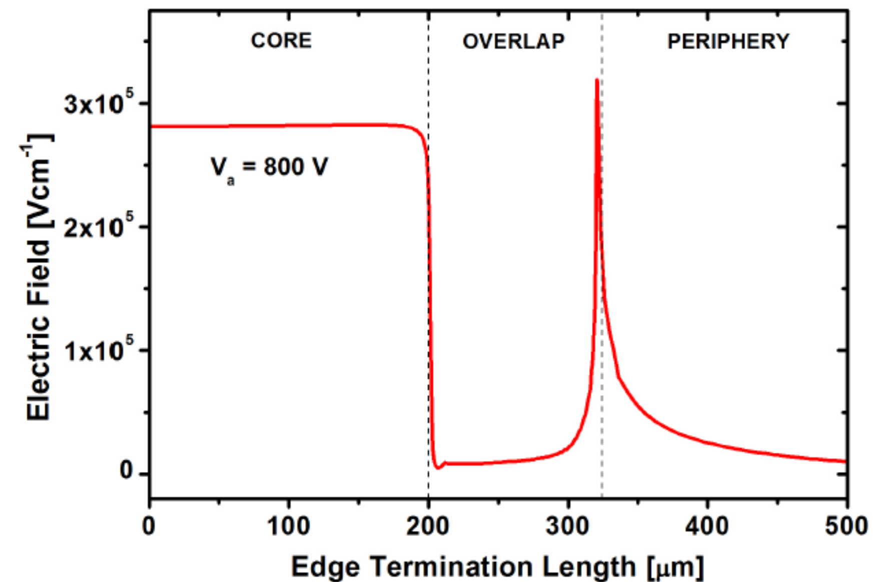


Junction Edge Termination: N^+ Extension

- **The N^+ is used to extend the N+ beyond the edge of the multiplication layer**
  - Phosphorous diffuses more in the very lowly doped substrate (higher curvature radius and voltage capability).
  - The electric field rapidly increases at the plain junction (multiplication).

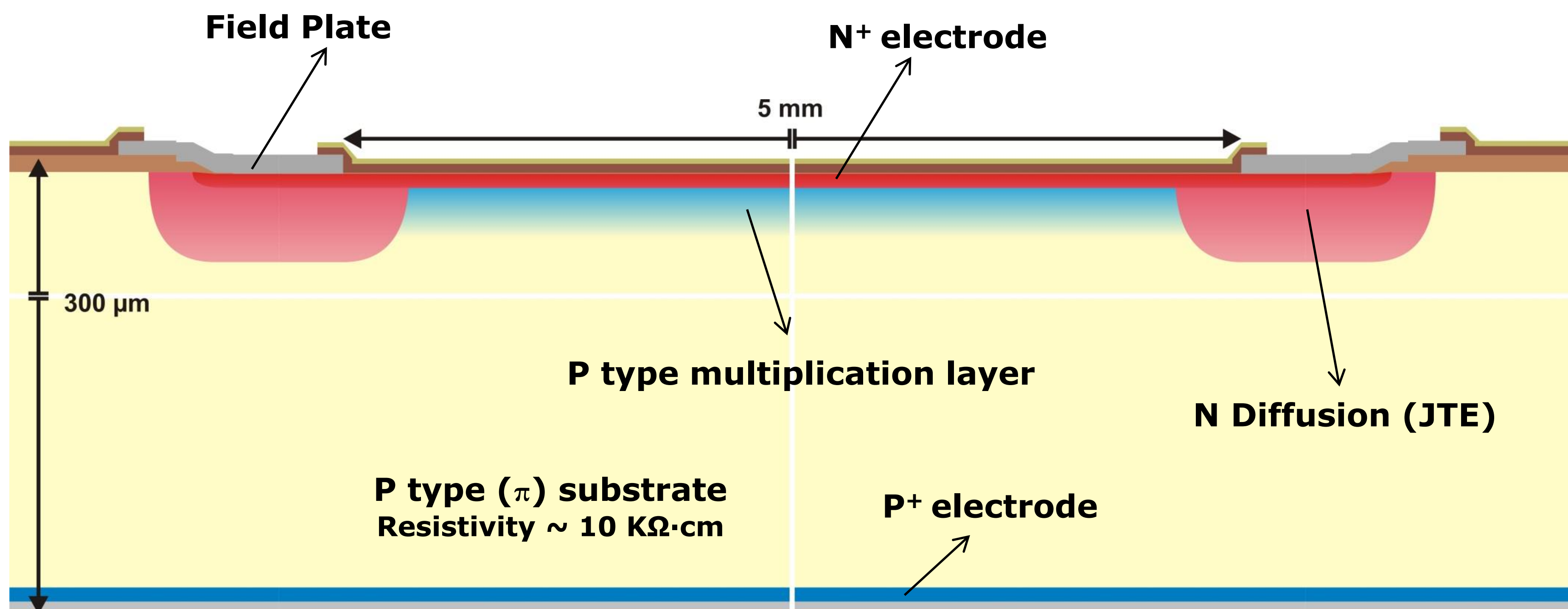


The lower Ec value at the overlap junction can lead the termination to breakdown



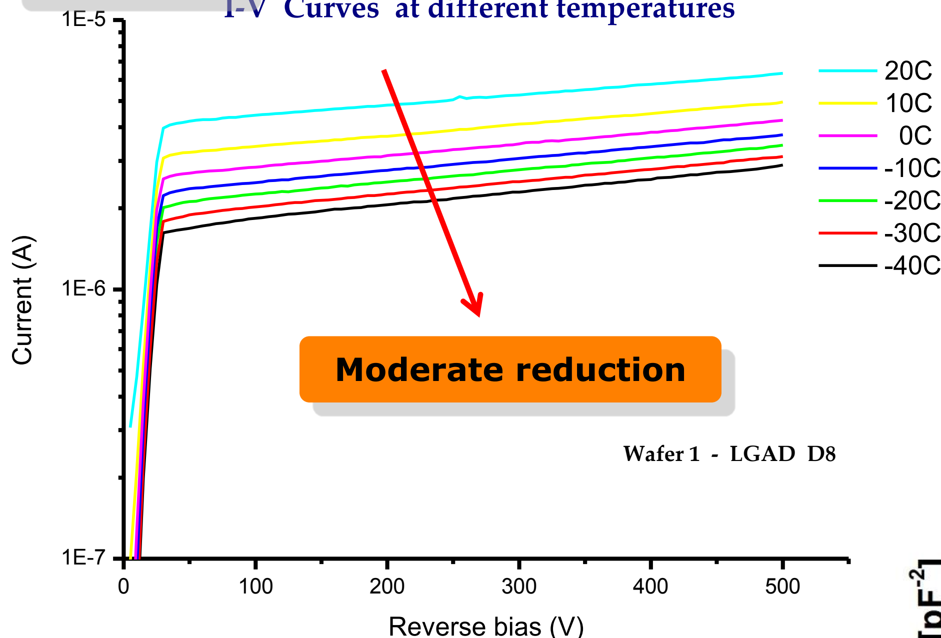
Junction Edge Termination: Junction Termination Extension

- **Lowly doped N-type Deep diffusion (JTE) around the curvature of the main junction**
  - Additional (specific) photolithographic step
  - The addition of a Field Plate moderates the electric field at the JTE curvature



Implementation: Problems at the peripheral region

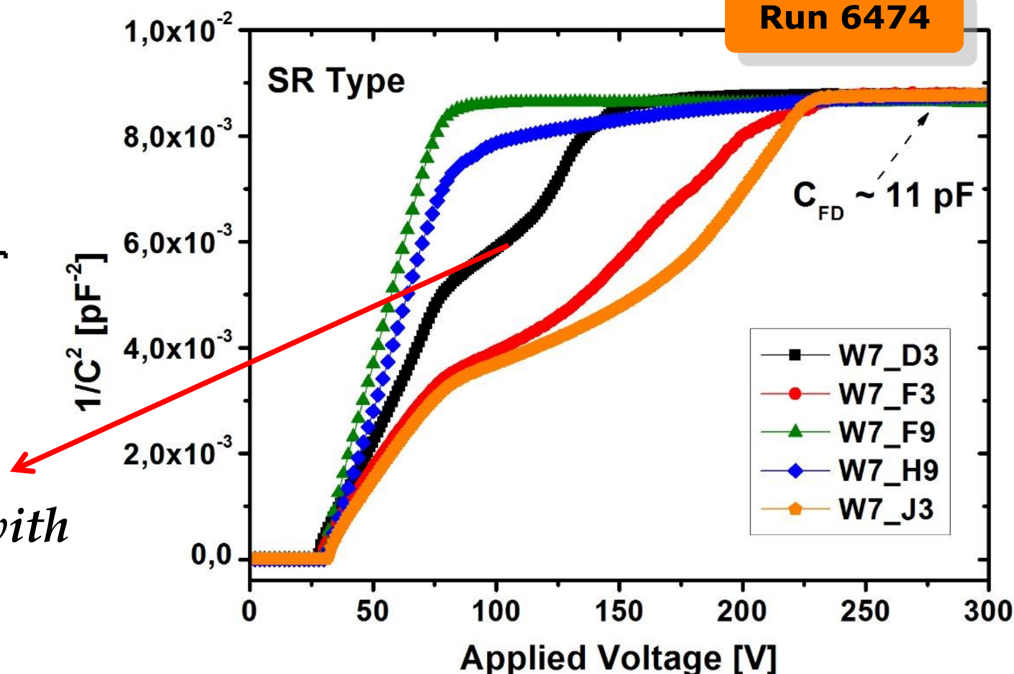
Run 7062



Moderate reduction

- *Leakage current is **mostly** generated at the periphery*

Run 6474



- *Capacitance humps are related with the **depletion of the periphery***