Ongoing R&D Activities at CiS

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Tobias Wittig, RD50 Meeting, 19.11.2014
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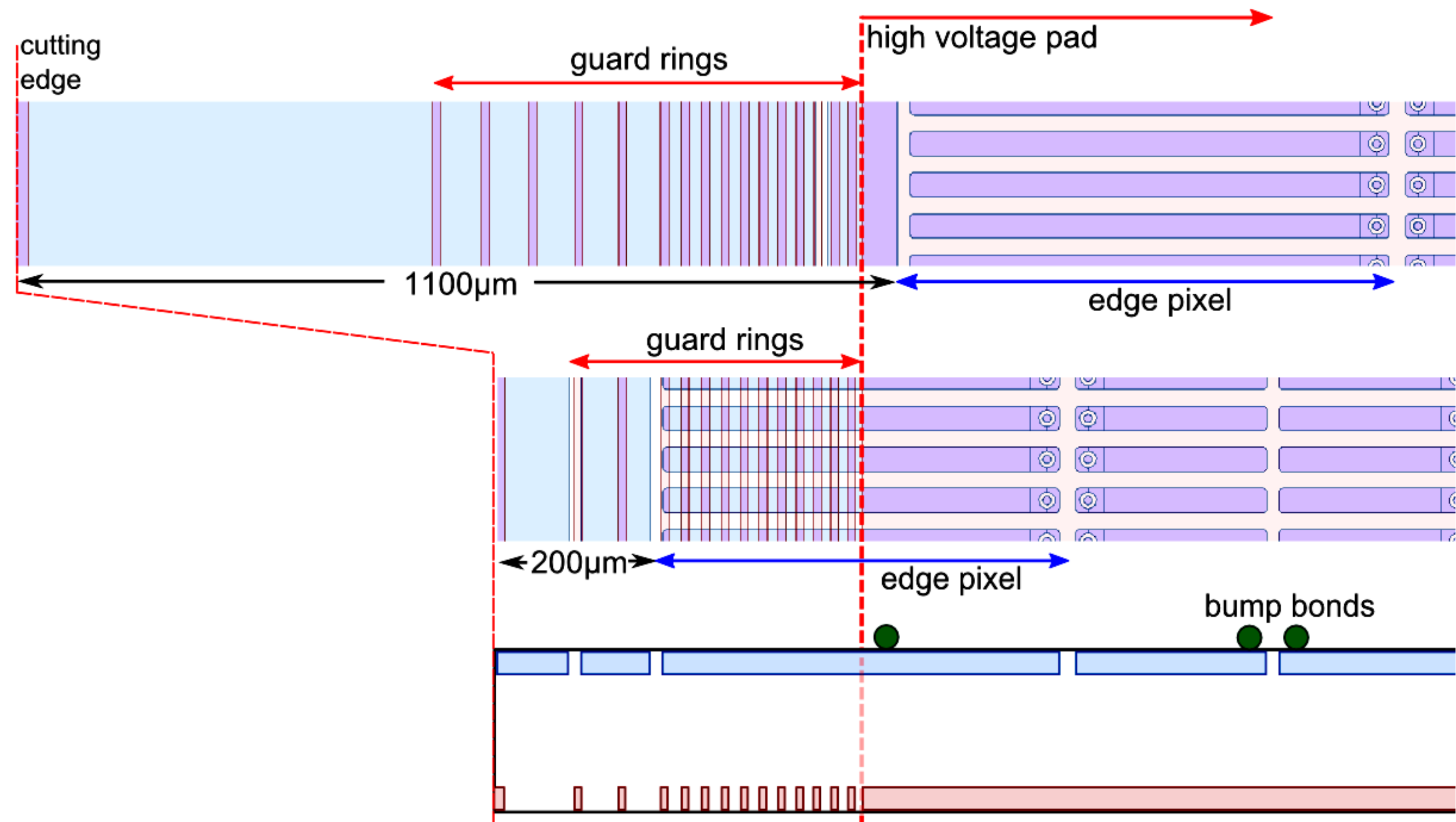
in cooperation with
technische universität dortmund

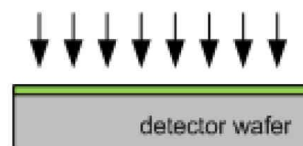
reduction of inactive edges

- so far at CiS: slim edge ATLAS IBL design, guard rings opposite to the pixels
  - conventional technology
  - only applicable for double sided n-in-n technology
  - reduction has (or will soon) reach its limits (O(200µm))
  - only in one dimension
- for further reduction (+second dimension), an improved technology is needed

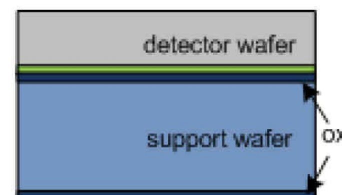


active edges

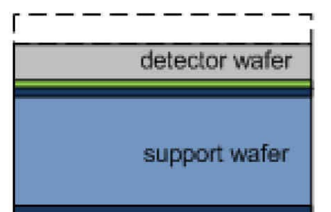
- new project has started, dealing with R&D of active edge sensors
- no new idea
  - activation of sensor side walls by doping
  - prevention of leakage current generation at side wall defects
- planned process is inspired by VTT (and others)
  - not many alternatives of how to implement the side wall activation in general
  - anyhow, several variances are possible for details



a) Phosphorus implantation



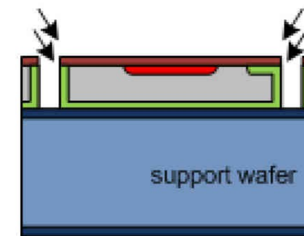
b) Wafer bonding to the oxidized support wafer



c) Grinding and CMP polishing of the detector wafer to the final thickness

d) Oxide growth, lithography, etching and ion implantation to form doped regions

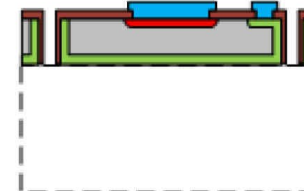
e) ICP etching to reveal the edge



f) Four-quadrant ion implantation to activate edges

g) Anealling and edge oxidation

h) Contact holes, Al deposition and patterning

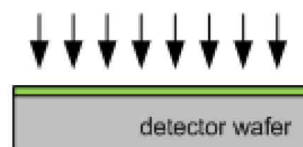


i) Removal of the support wafer

Wu et al., 2012 JINST 7 C02001

active edges – free parameters

- substrate doping
- thickness of sensor wafer
- trench widths
- implementation of doping of side wall
- trench refilling after side wall doping?
  - how?
  - if not:
    - how to conduct photo lithography with non-planar surface?
- sensor edge design



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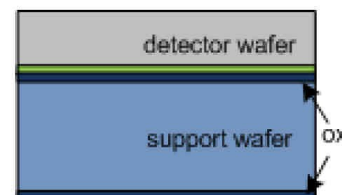

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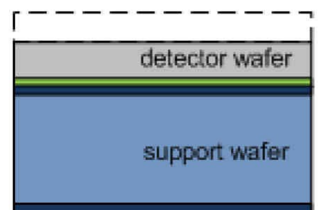

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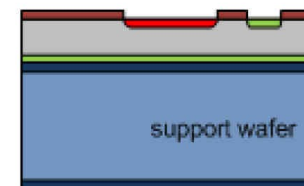

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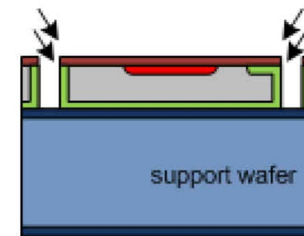

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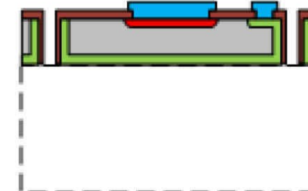

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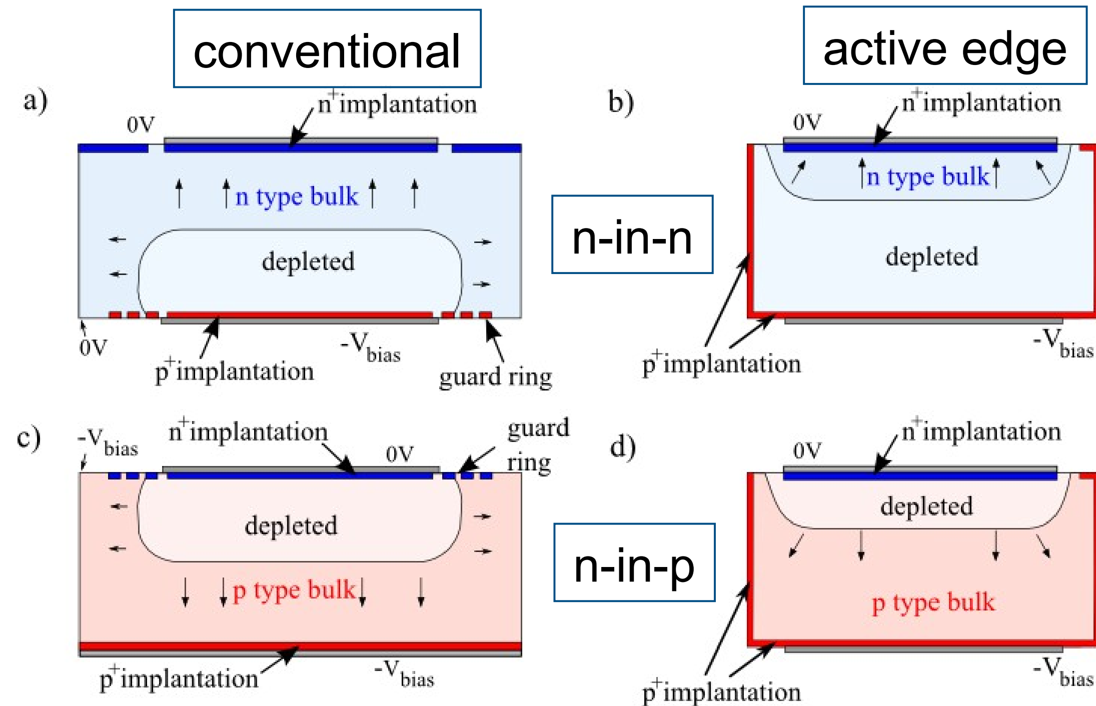
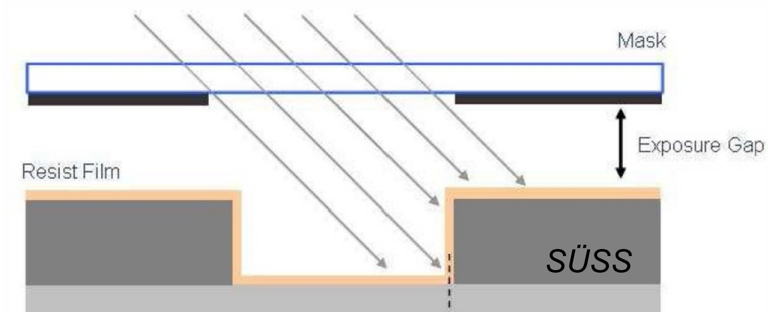
Wu et al., 2012 JINST 7 C02001

active edges – plans

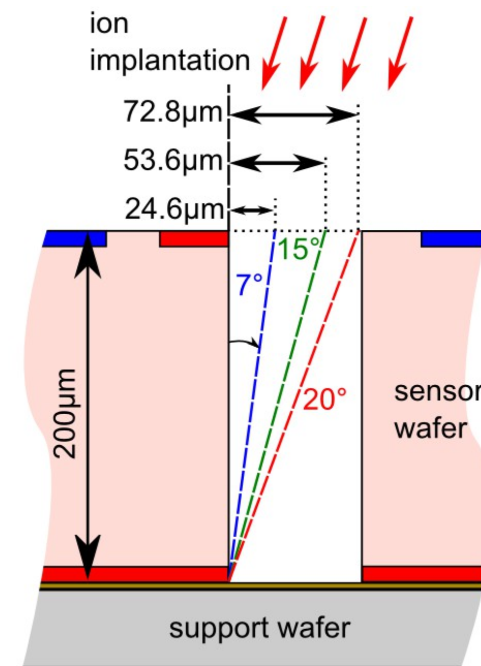
- substrate doping
  - only one wafer side is patterned
  - can process n-in-p as well as n-in-n sensors with the same mask set
- sensor thickness
  - one conservative, ~200...300µm
  - one thin, 100µm
- trench widths
  - various different sizes on same wafer: ~ 10...500µm
- non-planar lithography
  - very ambitious
  - not much experience up to now but in principal should be possible
    - optimization of photo resists
    - angular exposure

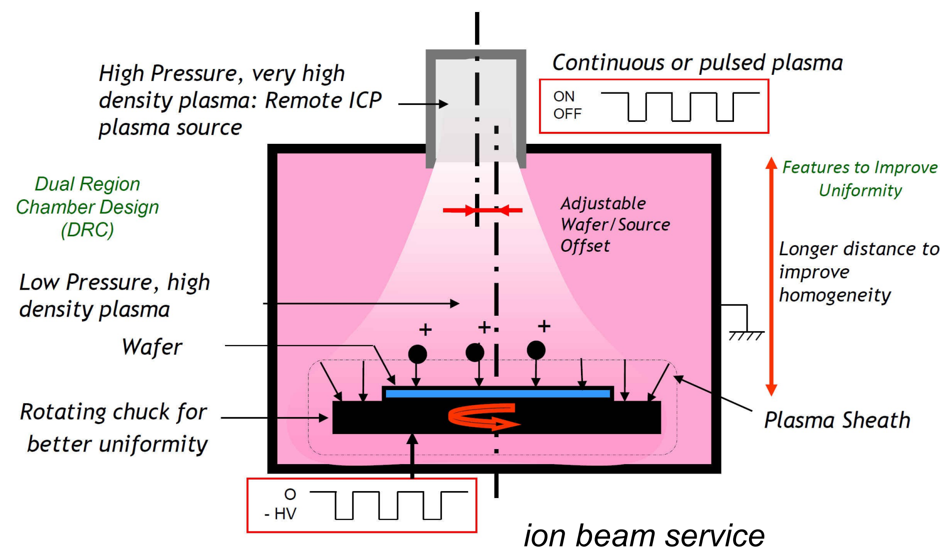




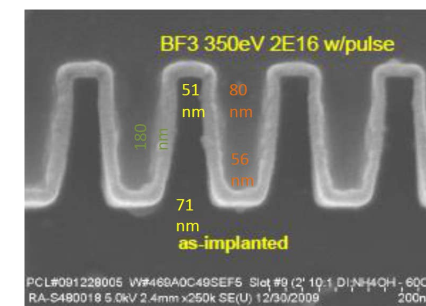
active edges – side wall doping

- 4 quadrant ion implantation
  - most consequent method
  - appears to be reliable
  - inefficient doping: implantation time has to be much longer than for surface implantation
    - shallow angle
    - implantation of all 4 quadrants
  - possible savings with higher angles
- plasma immersion ion implantation (PIII)
  - special method for homogeneous doping of 3D structured surface
  - technically speciallised for low energies
    - deeper profile has to be adapted by annealing time
  - cost savings are supposable
- deposition of Boron from gaseous phase
  - conventional process
  - used regularly in the past



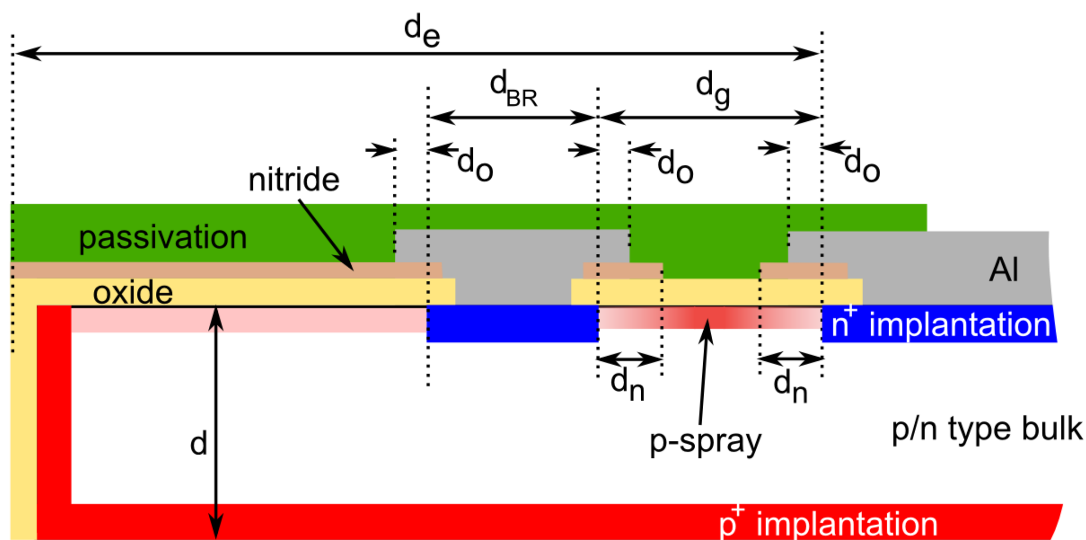


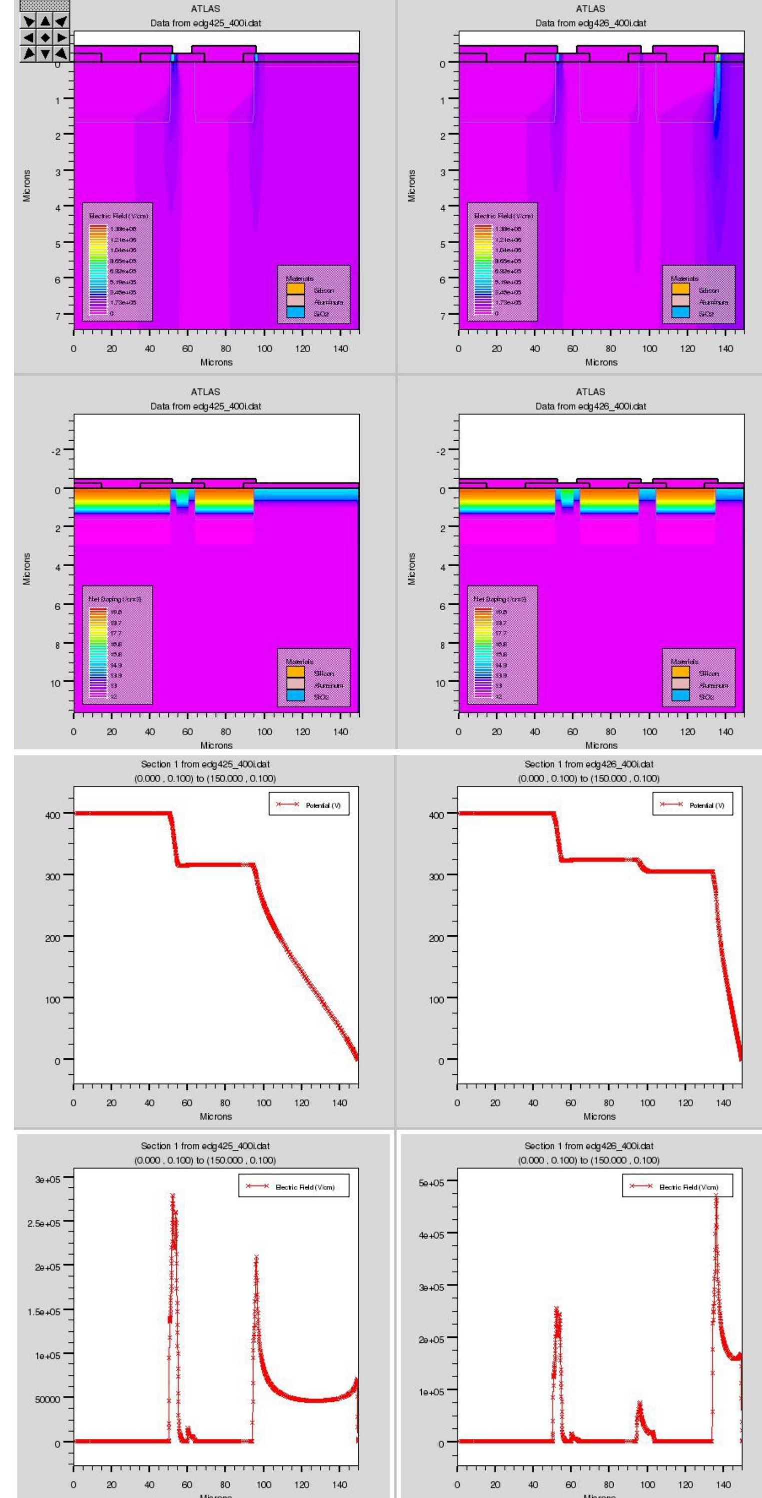
ion beam service



active edges - simulations

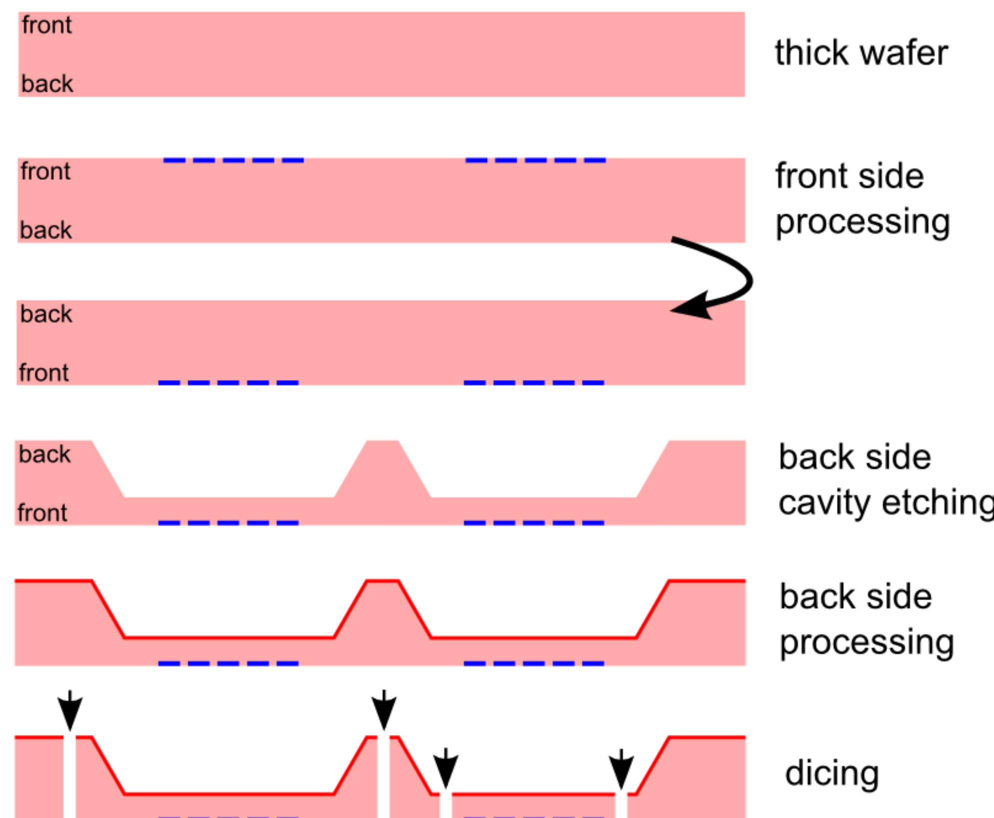
- many free parameters for the sensor layout
  - edge distance, number of guard rings, width of guard rings, metal overlap, p-spray dose ...
- vast number of combinations possible
- not possible to implement all of them
- currently conducting TCAD simulations to see which combinations are promising
- get an qualitative impression of how the design can be optimized
  - electric field maximum is an important reference point





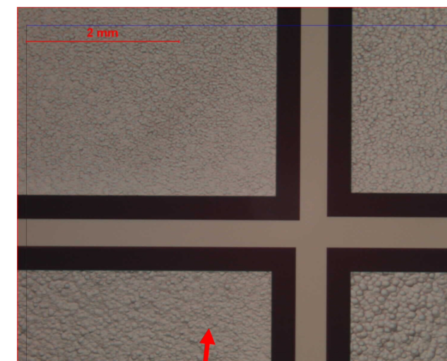
reduction of sensor thickness

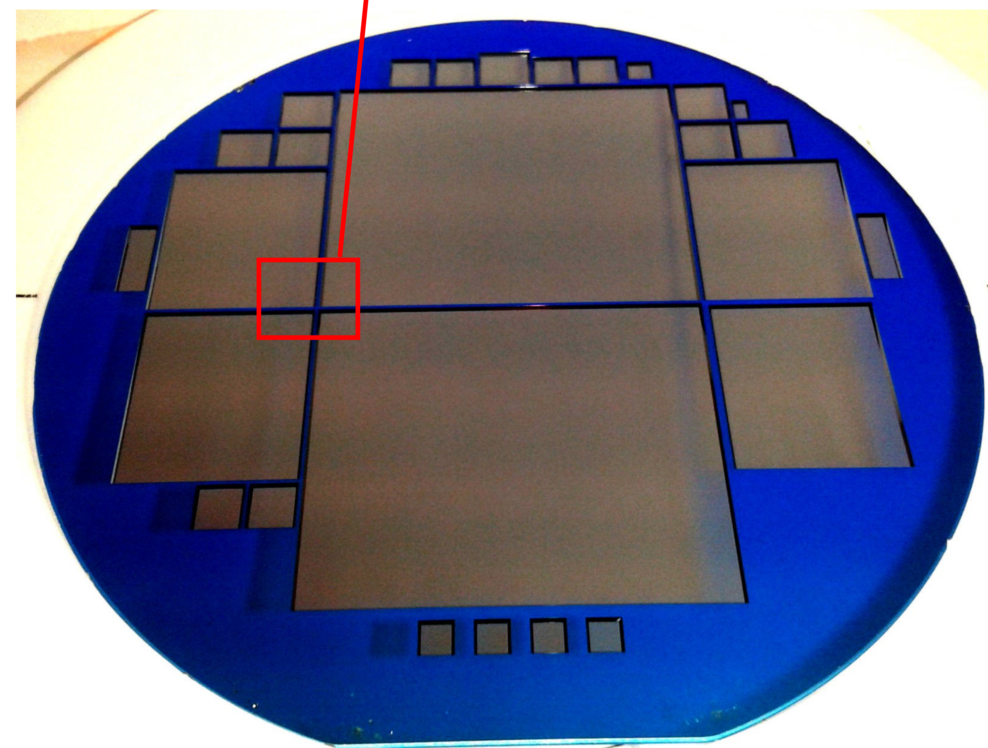
- smaller thickness is advantageous for planar sensors after high irradiation
- wafers getting extremely fragile with thicknesses <150um, esp if 6�namespace sizes are desired
- alternative to handling wafer can be etching of cavities to backside (<100> bulk)
- guarantees stability on wafer level by thick frames at the sensors edges
- sensitive area is located at the ‚membrane': thickness down to 50um should be feasible
- dicing can be done at the thick frames or within the cavity
- technology well known from pressure sensors
- process should work out for single sided sensors
- long term research project is applied

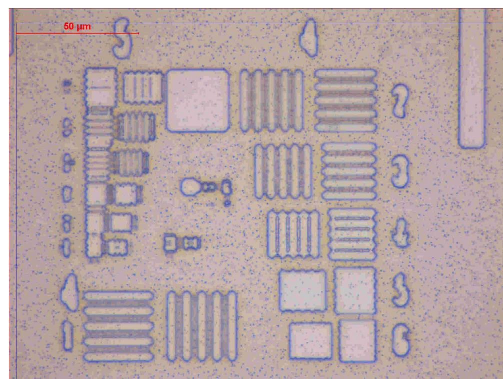


first test of large area thinning (1)

- common prototype run with MPP
- n-in-p ATLAS pixel sensors
  - different cavity sizes up to FE-I4 quad sensor size (~4x4cm²)
- starting thickness 525µm, target thicknesses 150/100µm
- started with dummy wafers to test feasibility
- KOH etching works in principle for such large areas
- resolution during photo lithography on front side is not influenced, state-of-the-art detector layouts can be realized

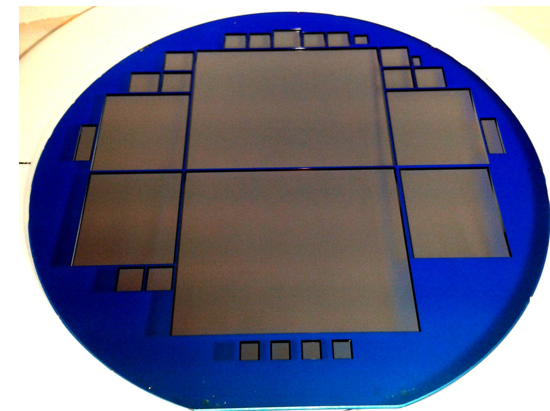


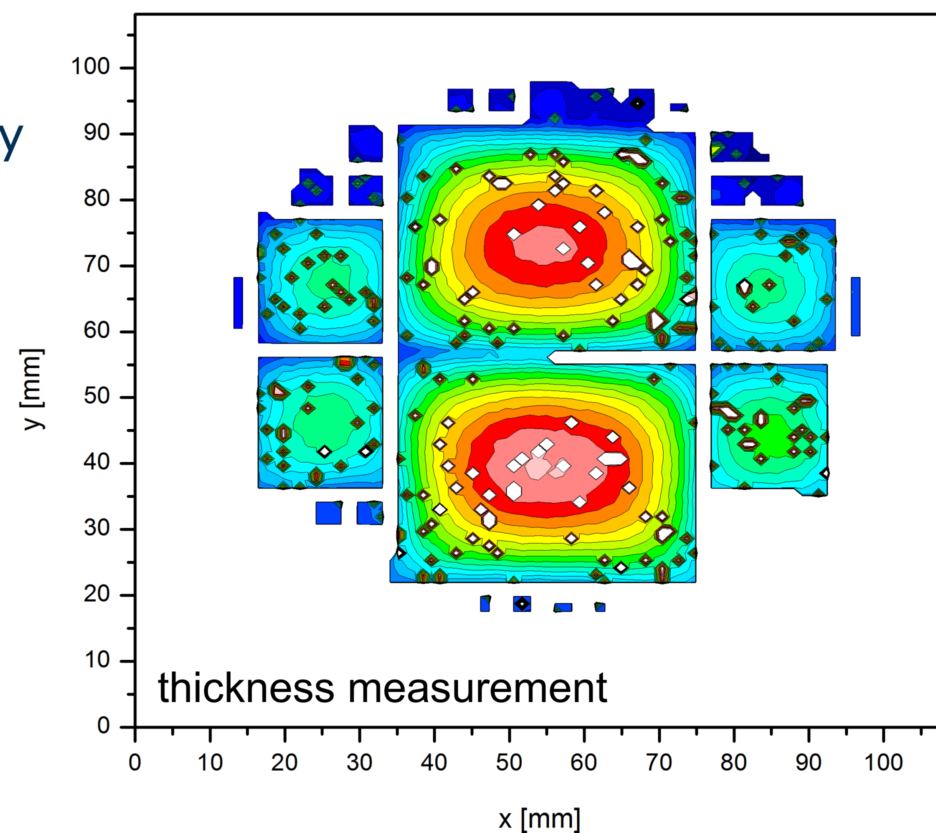


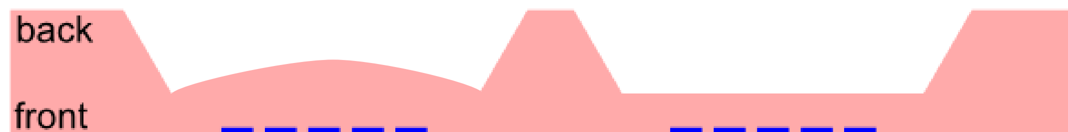


first test of large area thinning (2)

- first wafers show very high thickness variations
  - membrane is thin at the edge, thick in the center
  - especially pronounced for the quad sensors
  - up to some tens of µm -> not acceptable
- investigations are running
- it is assumed that etching rate is influenced by mechanical tensions
- it is conceivable that behaviour can be influenced by nitride and oxide layers on the front side
  - such optimizations have been done for pressure sensors
  - for this case much more challenging
    - significantly larger areas
    - distinct different sizes of membranes

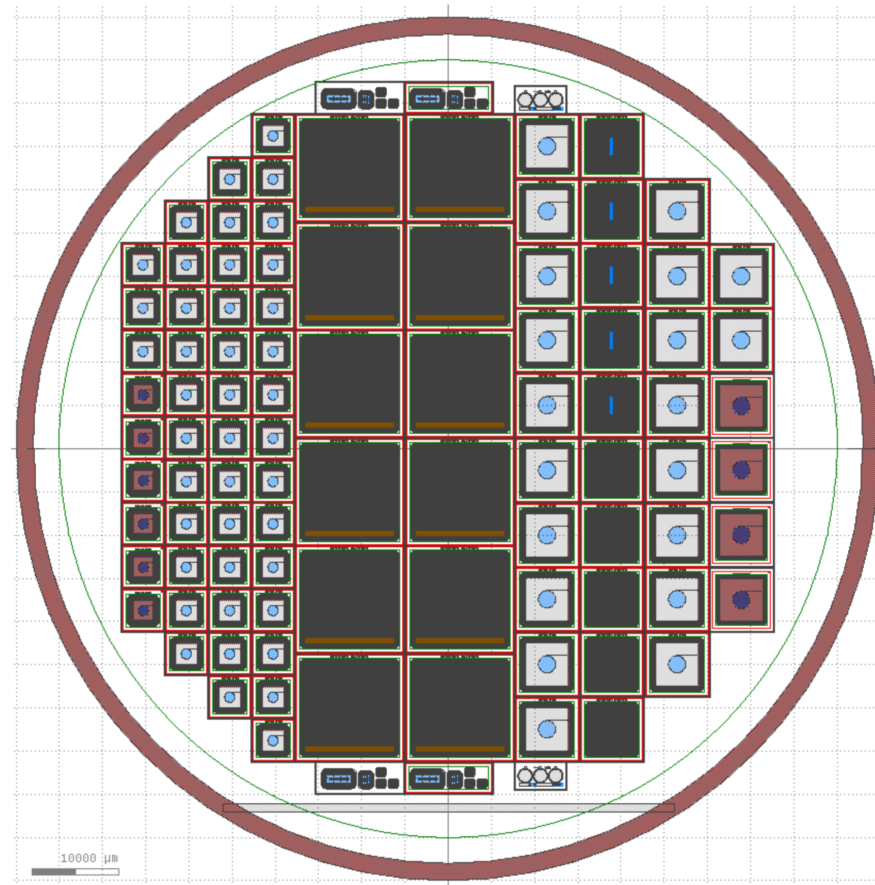




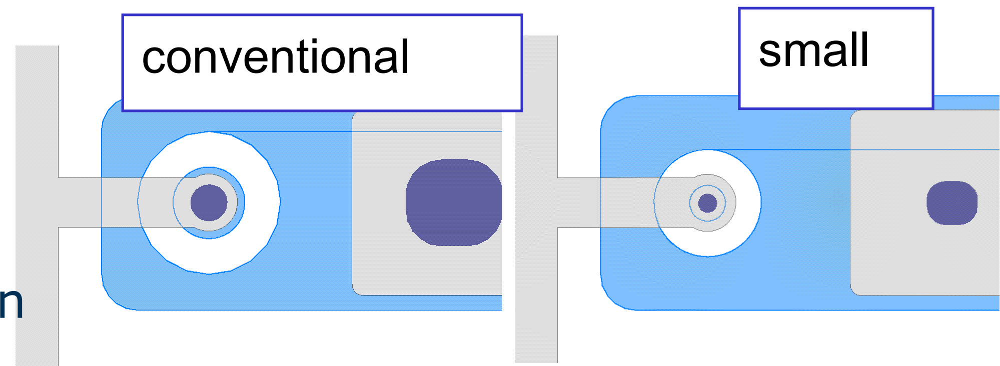


upcoming RD50 prototype wafer run

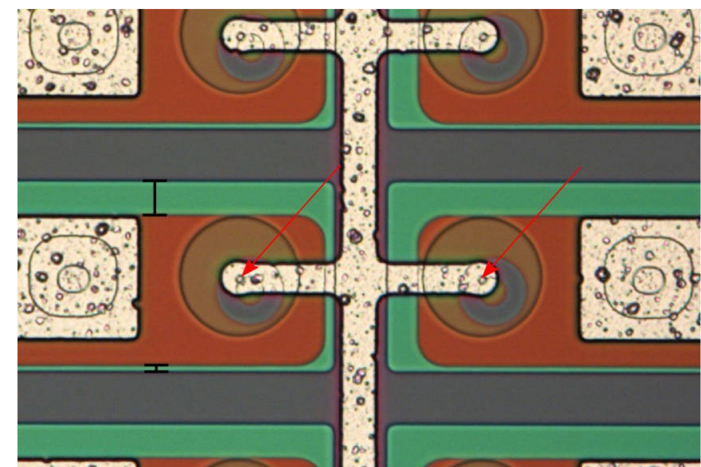
- analog technology as MPP run
- n-in-p, backside cavity etching
- less ambitious as cavitiy areas are much smaller
- several different structures on wafer
  - micro strips (80µm pitch, Poly-Si-Res)
  - diodes (two sizes)
  - spaghetti diodes (two kinds)
- two kinds of wafer material
  - Epi (525µm substrate + 50µm Epi)
    - etching the complete substrate
  - FZ (285µm)
    - etching to 50, 100, 150, 200µm (+unetched)
- layout almost finished
- production starts in the coming weeks

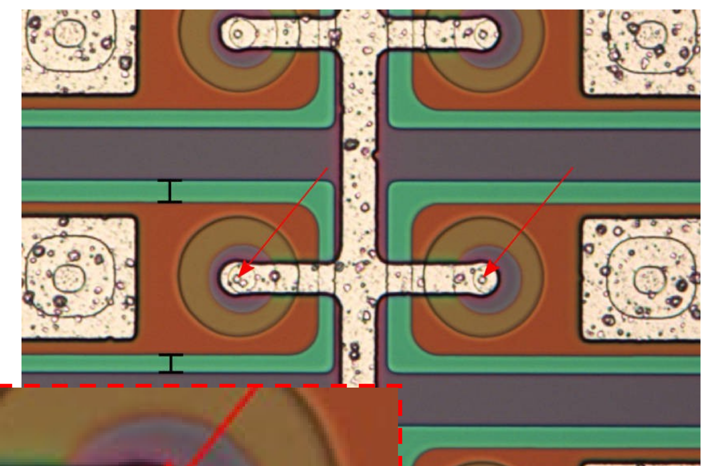


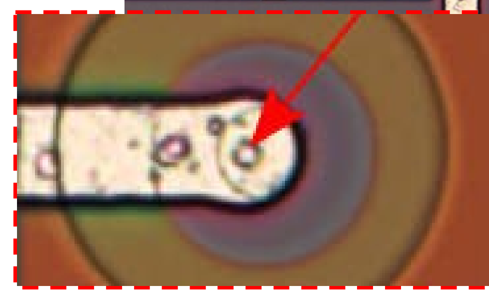
minimization of structure sizes



- laser direct imaging (LDI) was tested in combination with the conventional projection exposure (first try)
- no masks necessary anymore for LDI
- target dimensions O(2...3um)
  - implantations
  - oxide openings
- recognized larger discrepancies in alignment of laser and projection exposure
  - laser alignment fluctuated across wafer
  - reason was found and method could be improved for the next time
- tiny oxide openings seem to be open, at least visible in microscope
  - unfortunately it is hard to test if contact between metal and implant is given
  - dedicated test structures are foreseen/implemented on future productions



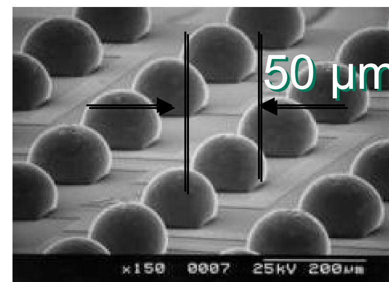


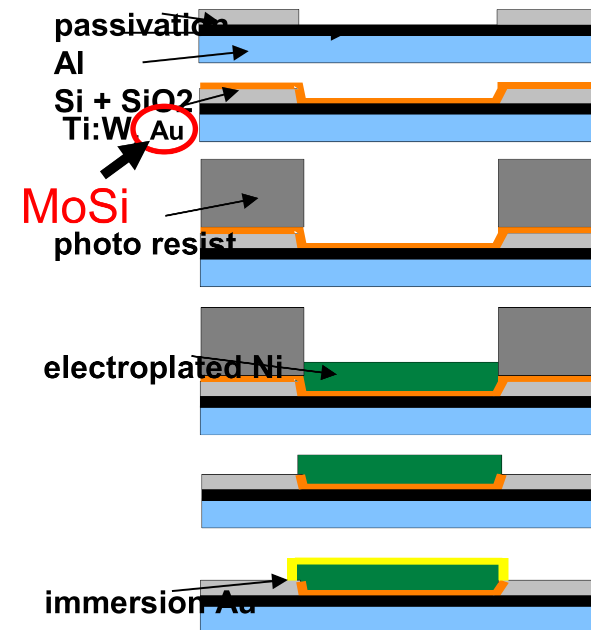


flip chipping technologies

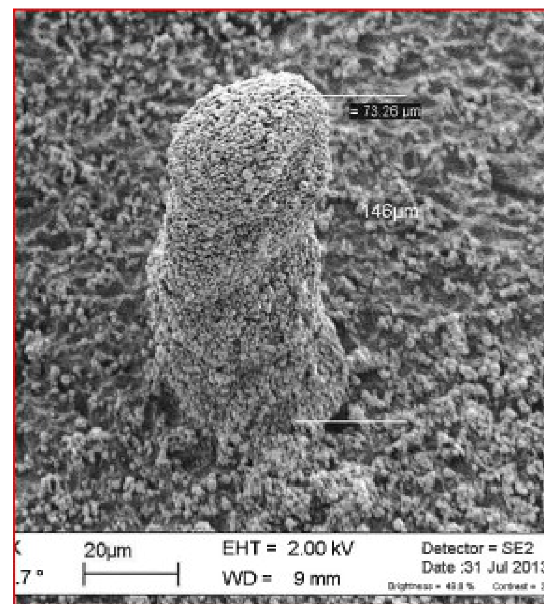
- sputtering and electroplating
  - → suitable for ultra fine contacts
- expensive and high technological effort
- looking for alternative for Au/Cu plating base
  - MoSi
  - conductive lacquer is more promising at the moment and is followed up

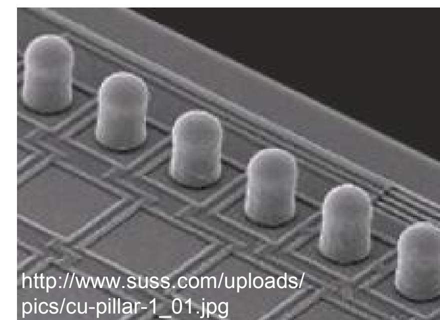
- adhesive bonding of pixel sensors
- requirement: contacts like pillars which stick out of the adhesive
- using nanoscale silver paste transfer to grow pillars step by step
- O(20µm) diametre reached up to now
- several challenges e.g.
  - proper contacts of the pillars
  - behaviour of adhesive at low temperatures

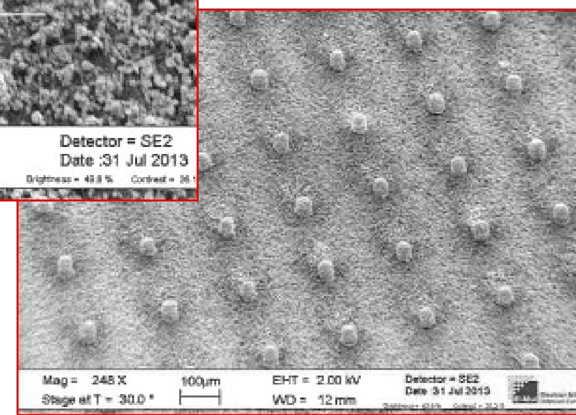




collaboration with Allresist



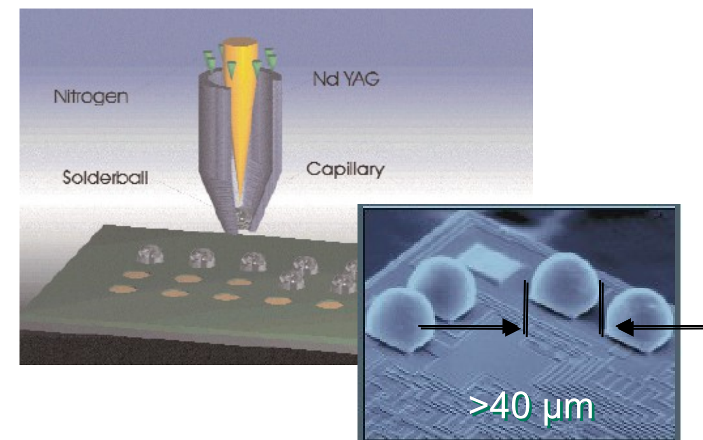




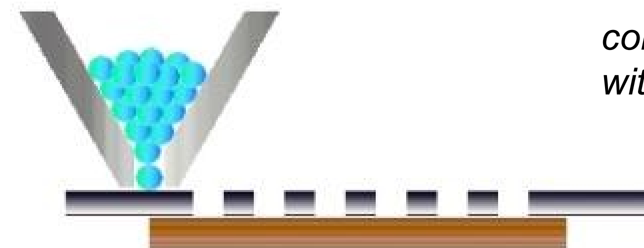
collaboration with ISC Konstanz & Utilight

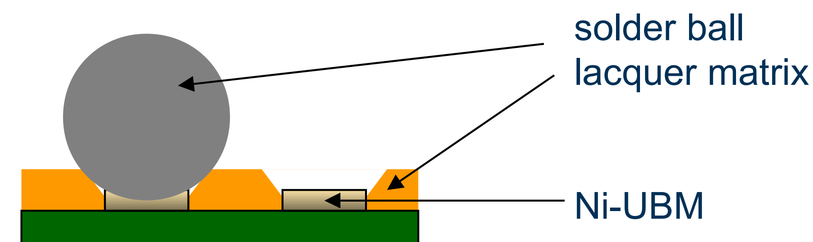
flip chipping technologies

- chemical processing of Ni/Au UBM and solder ball placement
  - low cost process due to maskless processing
  - suitable down to 40µm solder balls
  - facilitate the match of solder ball and pad with small cavities
  - for a start, begin with (single) solder ball placement -> not applicable for larger pixel sensors
  - think of method where balls are spread over the area and are captured by the cavities



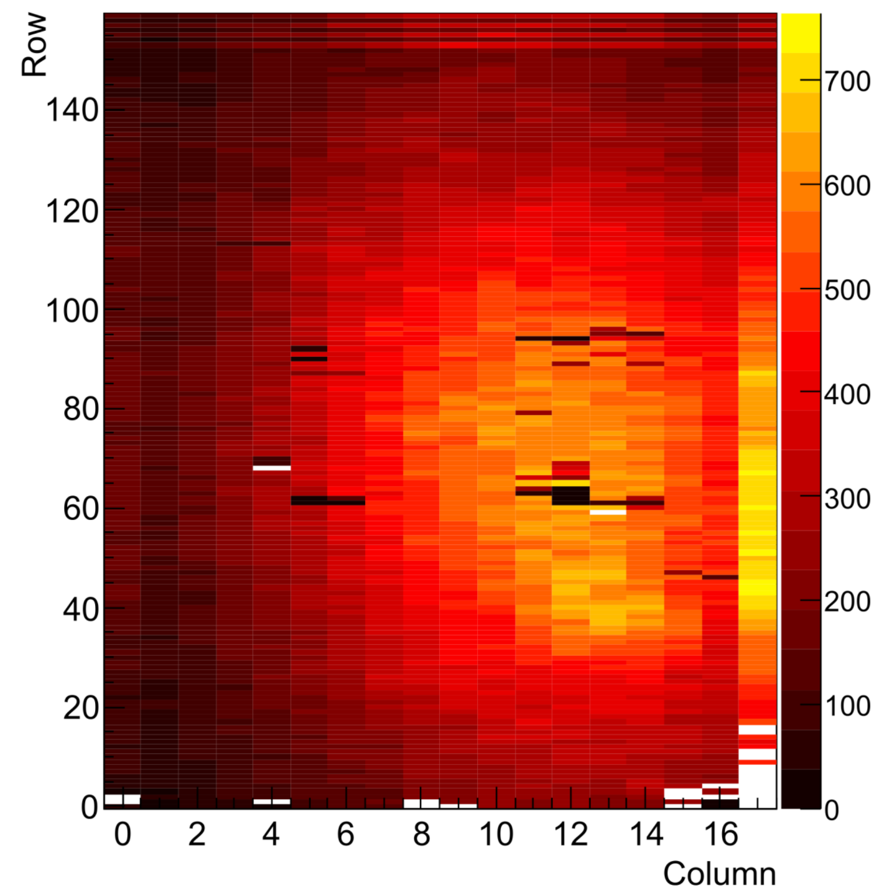
collaboration with Pactech

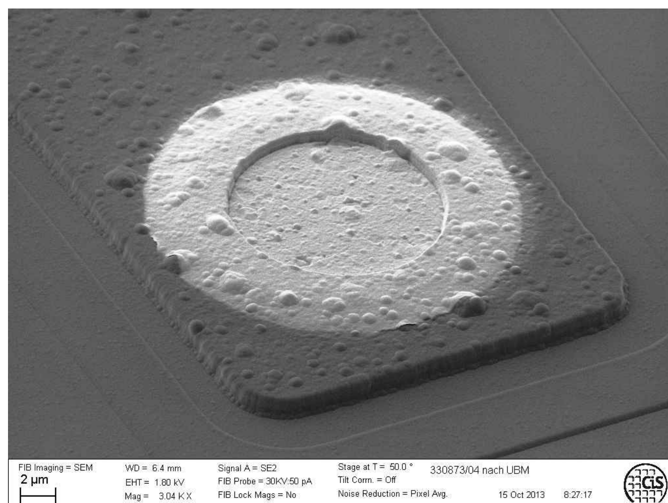




electroless Nickel UBM

- already tryed out with ATLAS pixel sensors
- combination with IZM solder bumps
- FE-I3 modules have been tested and seem to work
  - no significant bump failures are noticed
  - irradiation will be carried out in the coming weeks
- FE-I4 module assembly is expected soon





conclusion

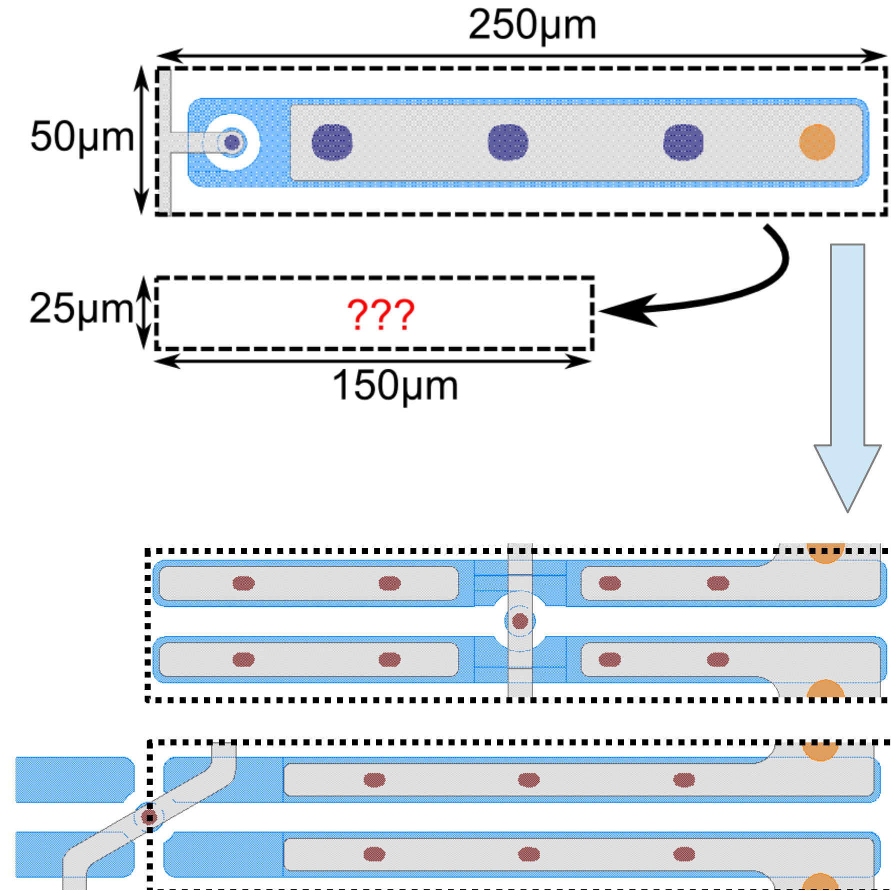
- CiS is engaged in various developments of future detector challenges in HEP
  - active edge sensors
  - large area thinned planar sensors
  - sensor design minimization
  - various sensor chip packaging technologies

  not mentioned up to now (but also running/prepared project):
  - defect engineering to improve radiation hardness
  - micro channel cooling
  - 3D sensors
  - 6'' wafer processing

Backup

sensor design challenges

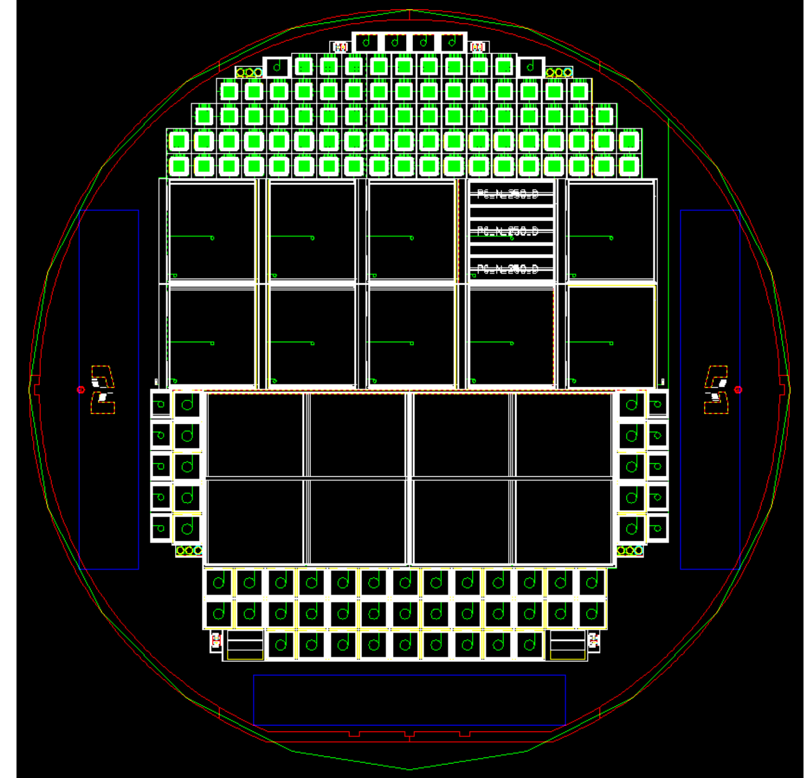
- smaller pitch aswell represents challenge to future sensor designs
- esp. conventional bias grid is not usable anymore
- testing different bias grid versions on current wafer productions
- variations of
  - bias dot position
  - bias dot diameters
  - pixel implant width

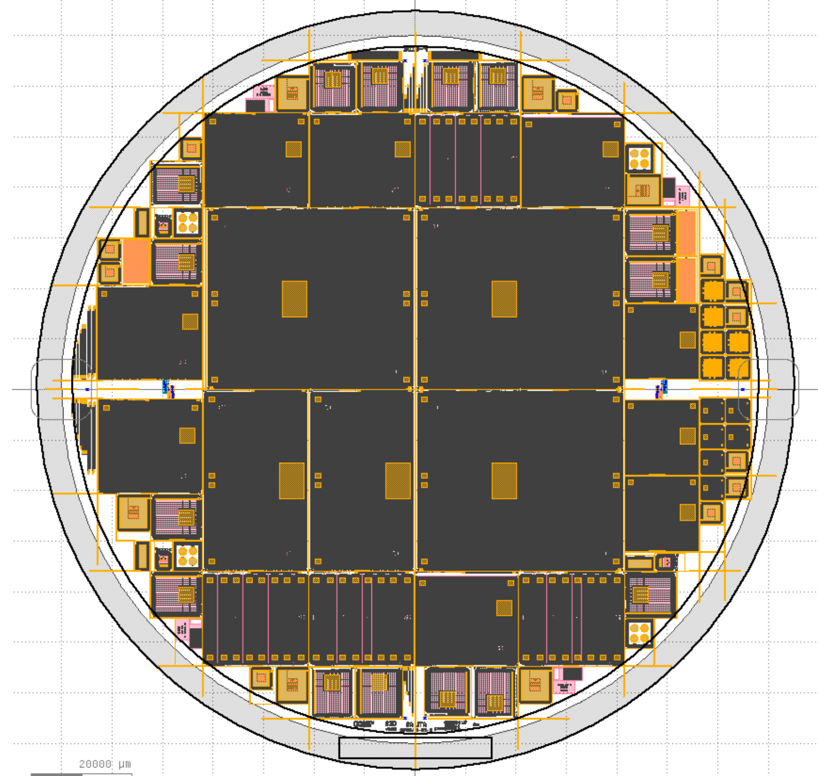


6‟ productions

- changeover to a 6‟ processing line is inevitable for a cost efficient large scale sensor production
- first steps are already done at CiS
  - first 6‟ n-in-p production for MPP Munich processed and delivered
    - 270um thickness
  - first 6‟ n-in-n production started right now (see next slide)

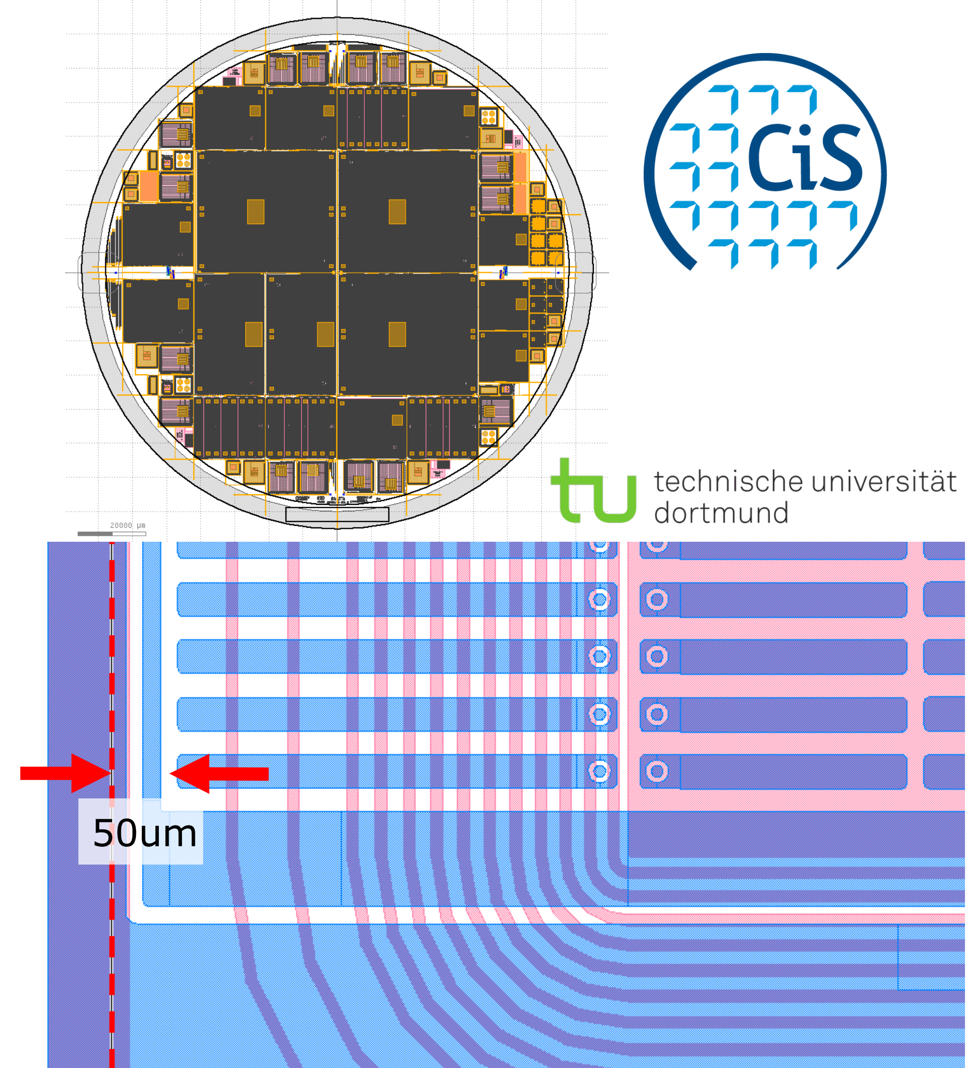
- at the time being, several processing steps are outsourced (MPI Halle)
- planned to conduct as many steps as possible in-house in the future

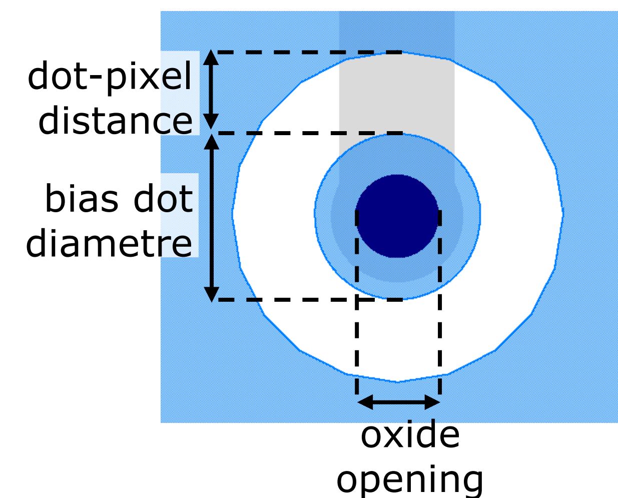




6‟ n-in-n production

- 500um thickness
- predominantly ATLAS pixel sensors
  - FE-I4 Quads, Alpines, pseudo-Hex possible
  - FE-I4 SCS, several versions
    - bias grid variations
    - extreme slim edge design
      - investigate if inactive edge of 50um is possible
- MediPix/TimePix & DosePix sensors
- test structures
  - systematic variations of bias grid dimensions
  - find out the minimal structure size which can be reached
    - with conventional projection exposure
    - with laser direct imaging





3D sensors

- geometrical advantages of 3D sensors compared to planar sensors are obvious
  - large volume of charge generation
  - small drift distances
- should technically result in a better radiation hardness
- CiS is planning to do initial steps towards the processing of 3D sensors
- new project in preparation, plans:
  - simulation/optimization of the layouts
  - determine challenges
    - etching of pillars (ICP etcher)
    - homogeneous doping of the pillars
    - properties of the interface within the pillars
  - maybe alternatives to Poly-Si deposition?
    - Spin-On
    - vapor deposition
  - concept of testability on wafer level

- cooperations with other institutes/universities very welcome

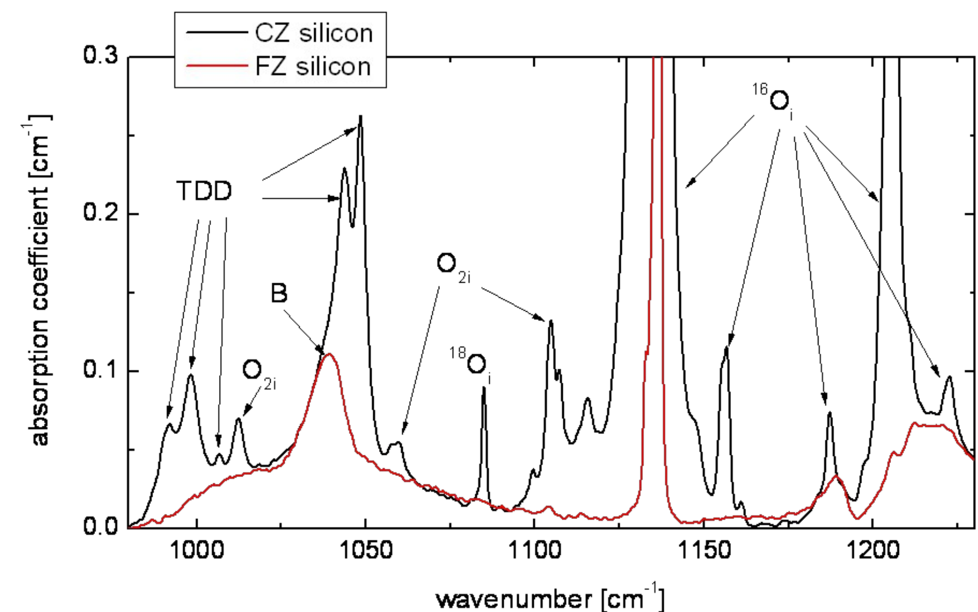
defect engineering

new project in preparation:

- improvement of the radiation hardness of silicon sensors by defect engineering

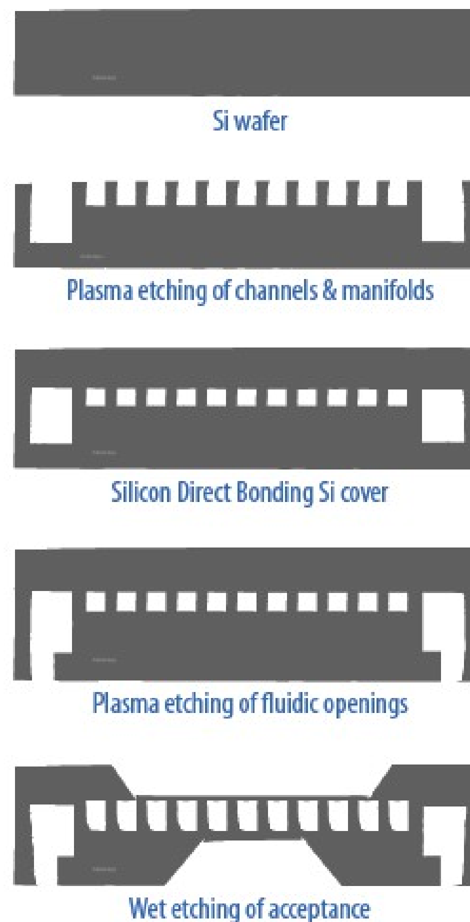
plans:

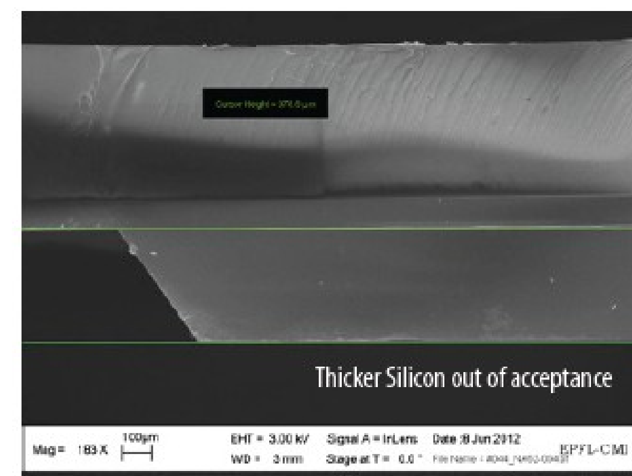
- analysis of defects in silicon during and after the processing, possibly also after irradiation
- investigation of the reason for increase of radiation hardness by oxygen
- optimize the defect configuration
  - investigate effect of other elements for bulk enrichment
  - adaption of essential process steps
    - influence of thermal budget to the oxygen defect configuration
    - influence of thermal donors
    - tempering
    - dielectrical layers
- tools:
  - simulation
  - charge carrier life time
  - low-temperature FTIR
  - DLTS



micro channel cooling

- etching of pipes into wafer should be possible at the end of this year (ICP etcher)
- technologies for remaining steps are already existing
- long-term research project running





PH-DT
Detector Technologies

VERTEX 2013

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