

# Alternative technologies for Low Resistance Strip Sensors (LowR) at CNM

CNM (Barcelona), SCIPP (Santa Cruz), IFIC (Valencia)

M. Ullán, V. Benítez, J. Montserrat, O. Beldarrain, M. Zabala,  
D. Quirion, M. Lozano, V. Fadeyev, A.A Grillo, H.F.-W. Sadrozinski

Contact person: Miguel Ullán



- Motivation
- Baseline solution
- Alternatives
- Titanium Silicide ( $\text{TiSi}_2$ )
- Highly Doped Polysilicon (HDPoly)
- Conclusions & future work

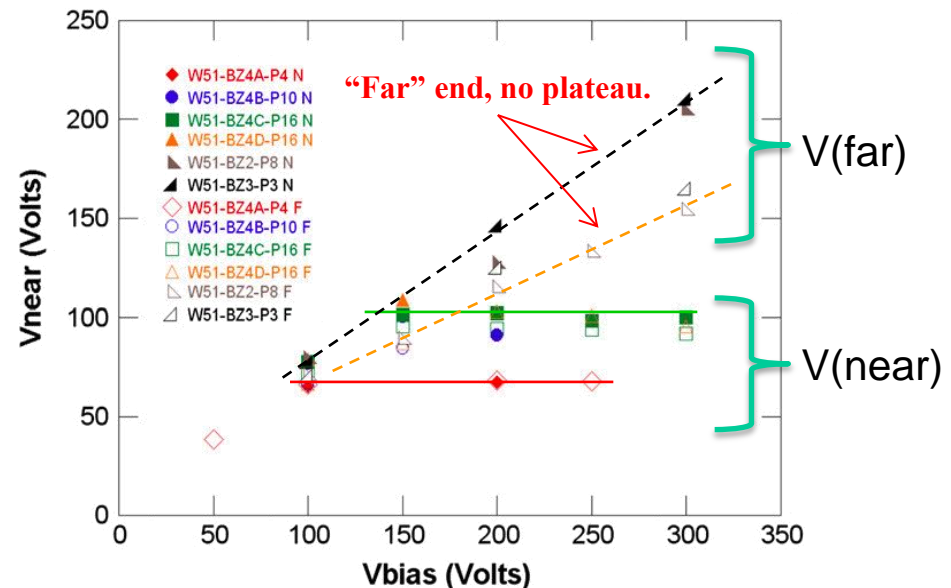
- In the scenario of a **beam loss** there is a **large charge deposition** in the sensor bulk and **coupling capacitors can get damaged**
- Punch-Through Protection (PTP) structures used at strip end to develop low impedance to the bias line and evacuate the charge

But...

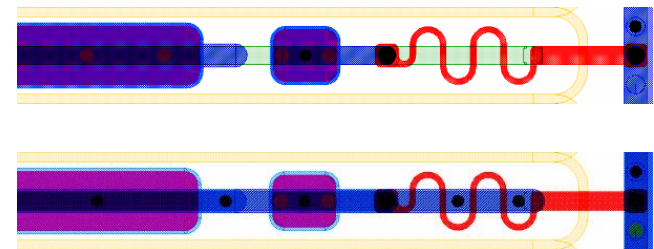
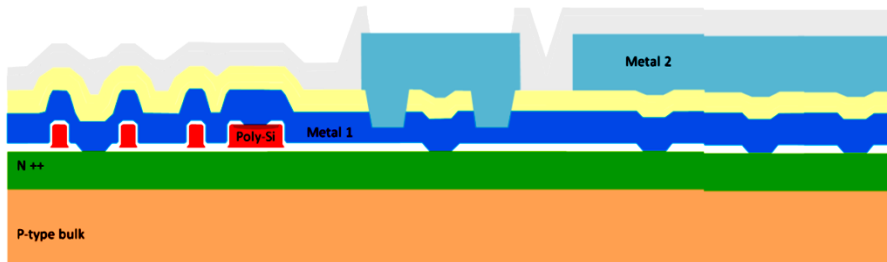
- Measurements with a large charge injected by a laser pulse showed that the strips can still be damaged
  - The **implant resistance** effectively **isolates** the “far” end of the strip from the PTP structure leading to the large voltages

Proposed Solution:

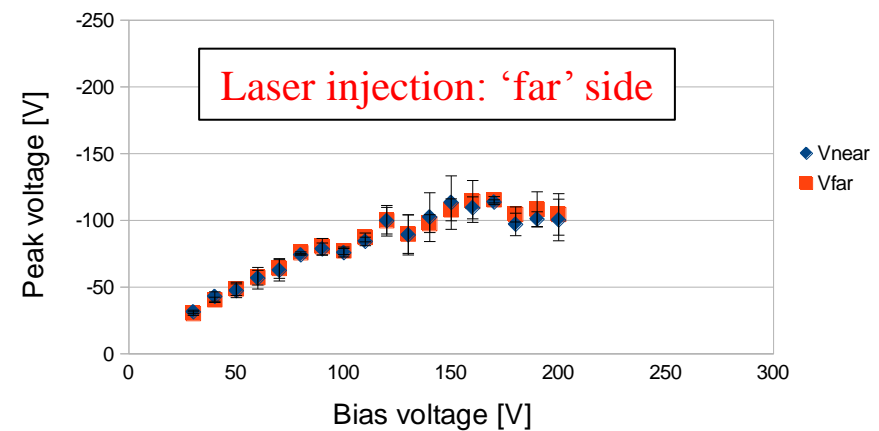
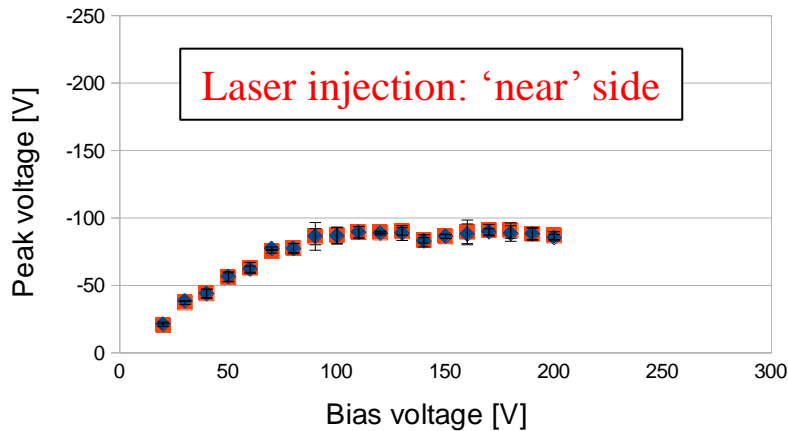
- To **reduce the resistance** of the strips:  
“Low-R strip sensors”



- Deposition of Aluminum on top of the implant:
  - $R_{\square}(\text{Al}) \sim 0.04 \Omega/\square \Rightarrow 20 \Omega/\text{cm}$  (**Drastic reduction of strip resistance!**)
- Metal layer deposition on top of the implant (first metal) before the coupling capacitance is defined (second metal).
  - Double-metal processing to form the coupling capacitor
  - A layer of high-quality dielectric is needed between metals for the coupling cap.
    - ☞ **Deposited** on top of the first Aluminum (not grown)
    - ☞ **Low temperature processing** needed not to degrade Al:  $T < 400 \text{ }^{\circ}\text{C}$ 
      - **Plasma Enhanced CVD (PECVD)** process at 300-400  $^{\circ}\text{C}$
    - ☞ **Triple-layer:** TEOS oxide (1000 Å) +  $\text{Si}_3\text{N}_4$  (1000 Å) + TEOS oxide (1000 Å)



## LowR 20 um PTP



- ✓  $V_{far} = V_{near}$
- ✓ A plateau is observed for both near and far laser injections on  $V_{far}$  and on  $V_{near}$ .
- ✓ When laser is fired on the near side, plateau is seen after 100 V bias. For the far side case, plateau is observed after 120 V.

### 👉 Technological difficulties:

- Double metal technology
- Low temperature deposited oxide quality

Other methods to obtain LowR sensors being studied:

- Titanium Silicide ( $\text{TiSi}_2$ ): allows the use of high temperature steps
  - ✓ oxide deposition  $\rightarrow$  oxide densification (high T)  $\rightarrow$  higher quality
- Highly Doped Polysilicon (HDPoly): allows the growth of thermal oxide after it
  - ✓ Oxide is grown on the polysilicon  $\rightarrow$  high quality oxide
  - ✓ Back to “standard” process

	sheet R (Ohm/#)	kOhm/cm	strip R (kOhm)
Implant	22	11	25.3
Metal	0.04	0.02	0.05
TiSi2	1.2	0.6	1.38
Poly	2	1	2.3

- Low-resistance strip sensors using these two alternative technological options have been fabricated at CNM

## ➤ $\text{TiSi}_2$

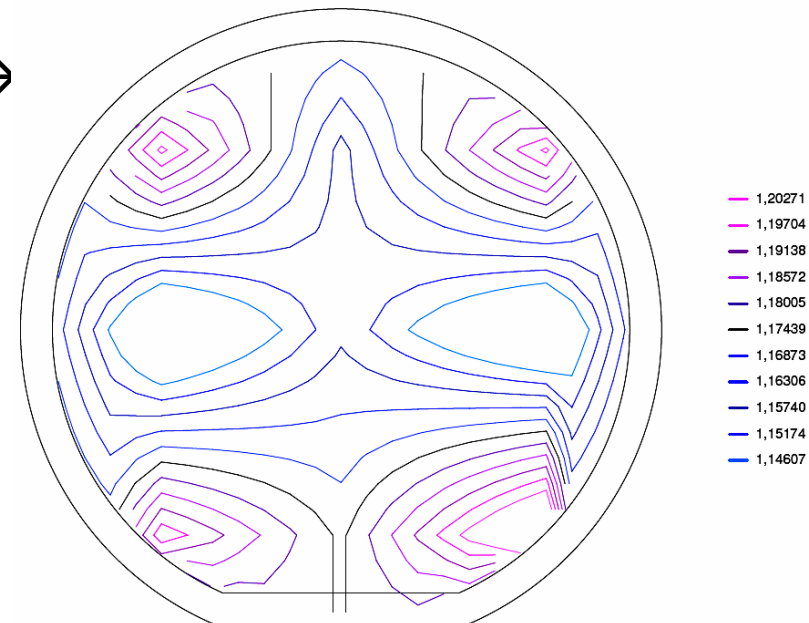
- Titanium Disilicide is a compound of Ti and Si
- It is formed using a high temperature process (RTA) on a layer of Ti deposited on Si
- A non-conductive layer of  $\text{TiO}_2$  can also be formed which is non-conductive and has to be removed/avoided
- The extra remaining Ti is selectively etched → → the process is self-aligned
- Higher leakage current in diodes (for thin implants)

## ➤ $\text{TiSi}_2$ formation technology at CNM

- 100 nm Ti deposited
- RTA
- Low sheet resistance:  $\sim 1.2 \pm 0.03 \Omega/\square$
- ✓ Good formation of  $\text{TiSi}_2$  layer

Contour Map

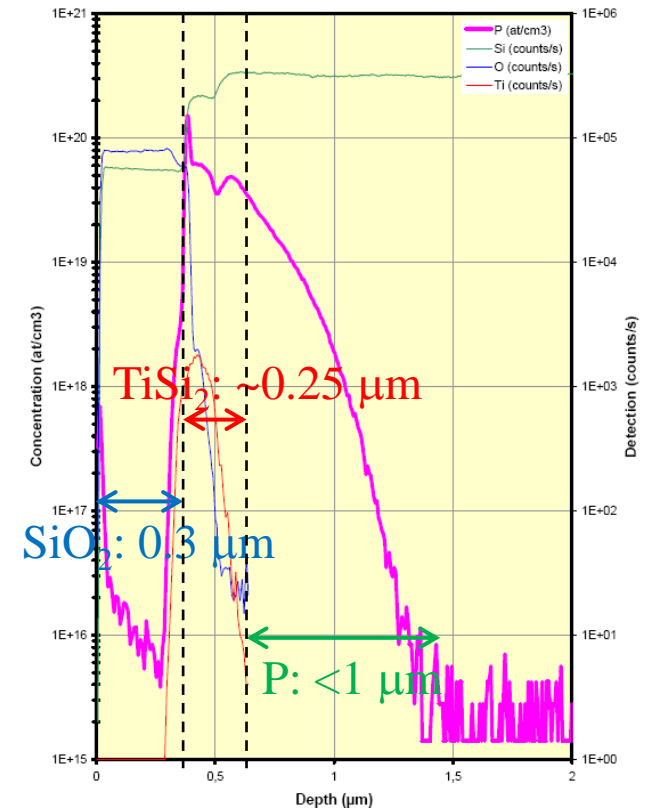
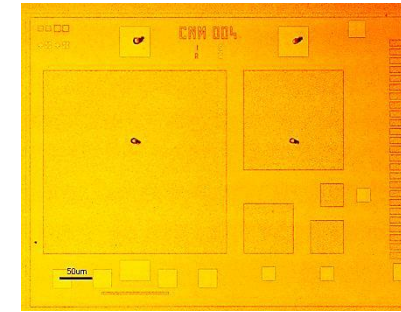
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3. Sample Size (mm) - Sample: 100 Flat: 4 Exclusion: 5		
4. Thickness (um) : 500	5. Correction F : 4,532	
6. Probe Space (mm) : 1	7. TCoefficient : 0	
8. TMeasure ("C) : 23	9. TReference ("C) : 23	
10. MMode : Cartesian		
11. Date : 10/07/2013 Time : 15:13:32		
12. Op ID : None		
13. Analysis [ ohm/sq ]		
1) Max : 1,22423	2) Min : 1,12571	3) Ave : 1,17439
4) StDev : 0,03398	5) Uni (%) : 4,19452	6) Max-Min(Range) : 0,09852
/ Ave (%) : 2,89381		
14. Description : 6971-MIM-1		



- TiSi<sub>2</sub> MiM capacitors fabricated
  - Substrate is implanted as in strips
  - A layer of TiSi<sub>2</sub> is created as bottom plate of the capacitors in contact with Si
  - 300 nm of oxide deposited at low T (PECVD)
  - Densification at 900 °C , 30 min
  - Aluminum layer deposited and defined as top plate of the capacitors

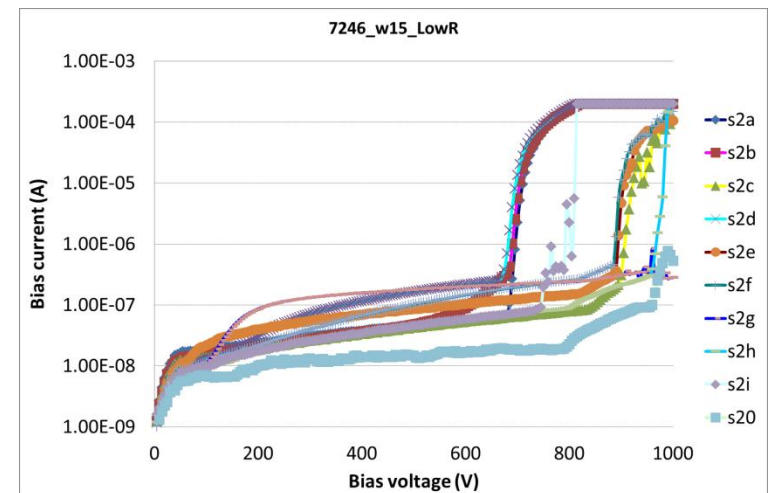
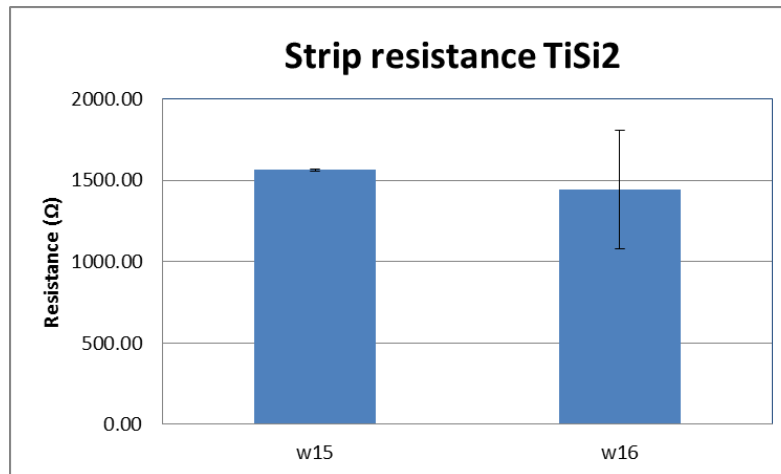
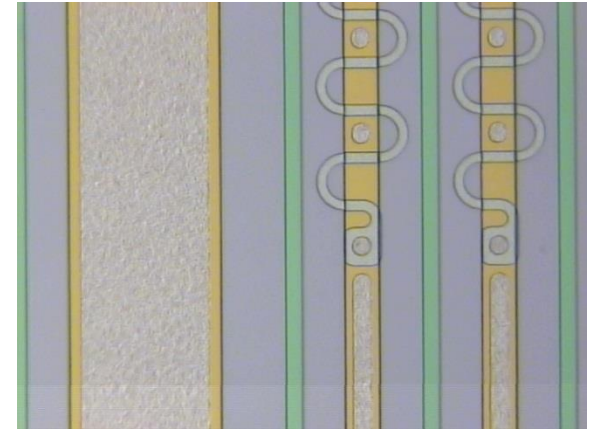
## ➤ Results

- SIMS (Secondary Ion Mass Spectrometry)
  - Detection limit  $>10^{15} \text{ cm}^{-3}$
  - No perfect calibration for TiSi<sub>2</sub>
  - Negligible effect on implant depth
  - TiSi<sub>2</sub> layer  $\sim 2.5 \times$  Ti layer
- 98-100% yield up to 100 V
- Breakdown voltage  $>150 \text{ V}$





- To form the low resistance strips a layer of TiSi<sub>2</sub> is formed on top of the implant
  - Self aligned process → no additional mask required
  - Good general performance of sensors
  - More than order of magnitude reduction in strip resistance (~0.7 kΩ/cm)
  - No additional leakage current observed



- Polysilicon layer doped with liquid source ( $\text{POCl}_3$ , “Phosphoryl chloride”) in contact with the silicon implant (substitutes the metal layer)

- High doping levels reached at high temperatures ( $1050^\circ\text{C}$ ) and long times

- Possibility to grow a thermal oxide on top of the polysilicon layer to form the coupling capacitor

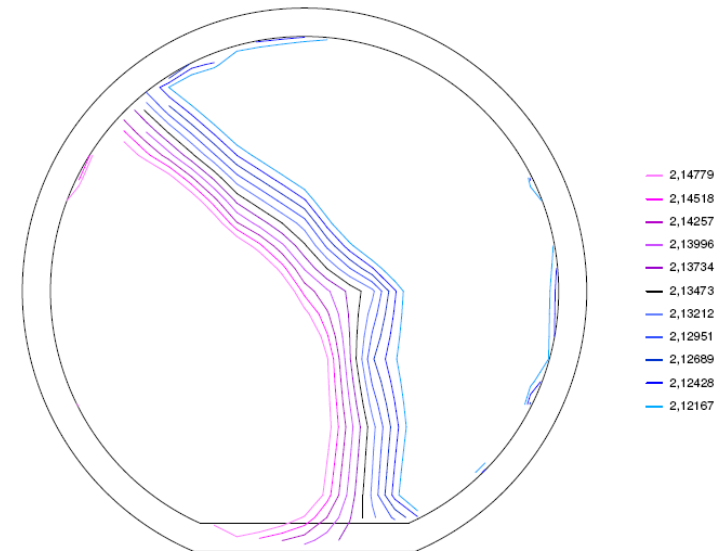
- Much higher quality oxide
- Although risk of lower breakdown voltages
- Higher thermal load of the process
- Risk of dopant precipitates later in the process

- HDPoly formation at CNM

- DOE (thickness  $\uparrow$ , doping time  $\downarrow$ )
- Good conductance:  $\sim 2.0 \pm 0.04 \Omega/\square$

Contour Map

1. Lot ID : None  
 2. Data File : None  
 3. Sample Size (mm) - Sample: 100 Flat: 4 Exclusion: 5  
 4. Thickness (um) : 500  
 5. Correction F : 4,532  
 6. Probe Space (mm) : 1  
 7. TCoefficient : 0  
 8. TMeasure (°C) : 23  
 9. TReference (°C) : 23  
 10. MMode : Cartesian  
 11. Date : 19/12/2013 Time : 18:23:23  
 12. Op ID : None  
 13. Analysis [ ohm/sq ]  
 1) Max : 2,19803  
 2) Min : 2,07913  
 3) Ave : 2,13473  
 4) StDev : 0,03505  
 5) Uni (%) : 2,78490  
 6) Max-Min(Range) : 0,11890  
 / Ave (%) : 1,64176  
 14. Description : 7146-MIM-1



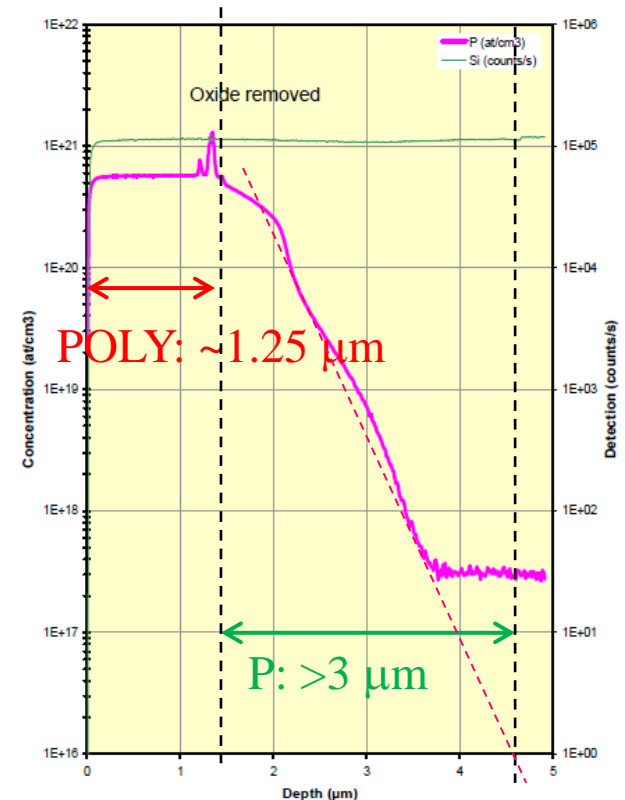
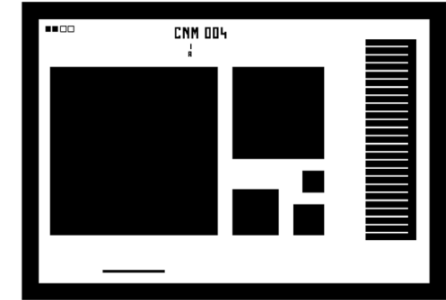
	W1	w2	w3	w4	w5
Poly thicken	-	-	+	+	+
doping (t)	-	+	-	+	-
Resist (Ohm/sq)	2.13	1.70	2.02	1.65	2.00

- Capacitors:

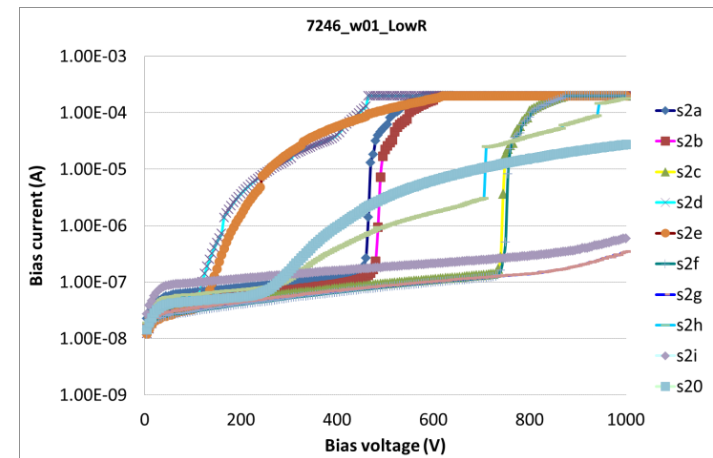
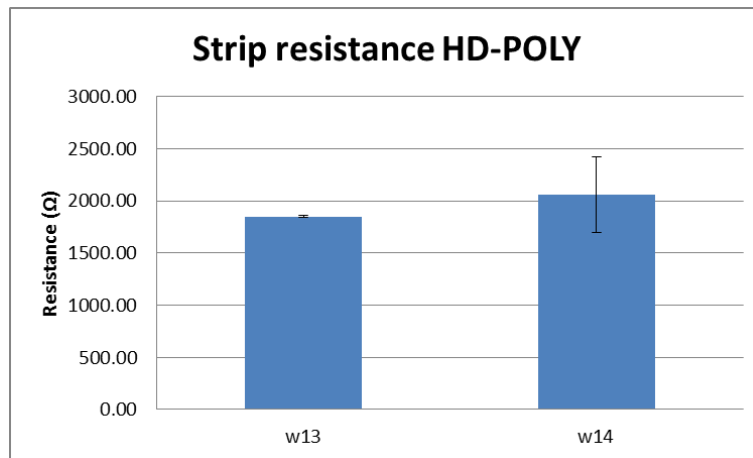
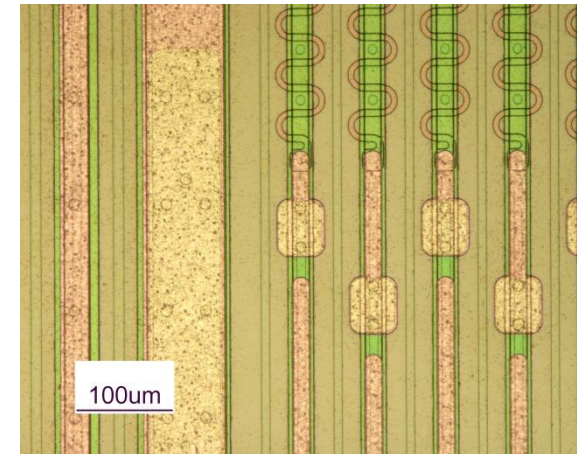
- Substrate is implanted as in sensors
- Polysilicon is deposited and doped without mask (to form the bottom plate of the capacitors)
- Thermal oxide is grown afterwards (200 nm)
- Photolithography: to open contact to Poly
- Aluminum sputtering
- Photolithography: Capacitors' top plate definition and contact to poly (bottom plate)

- MIM capacitors

- SIMS (Secondary Ion Mass Spectrometry)
  - Detection limit  $>10^{17} \text{ cm}^{-3}$
  - Poly doping up to  $\sim 6 \times 10^{20} \text{ cm}^{-3}$  (implant  $\sim 2 \times 10^{20}$ )
  - Not negligible effect on implant depth ( $>3 \text{ }\mu\text{m}$ )
  - Not important effect on sensor performance
- 98-100 % yield up to 20 V
- Breakdown @ 40-50 V
  - 200 nm oxide thickness



- A layer of Polysilicon is deposited on top of the implant and then highly doped
  - Good general performance of sensors
  - One order of magnitude reduction in strip resistance ( $\sim 1 \text{ k}\Omega/\text{cm}$ )



- ✓ Low-resistance strip sensors (LowR) proposed to extend the protection afforded by PTP structure to the entire active area of the sensor
- ✓ Implementation with Aluminum layer already demonstrated (see presentation at last RD50 meeting: <https://indico.cern.ch/event/307015/session/9/contribution/17/material/slides/1.pdf>)
- ✓ New technological implementations have been fabricated
  - Titanium Silicide ( $\text{TiSi}_2$ ) → Improved oxide quality
  - Highly Doped Polysilicon (HDPoly) → High quality oxide + standard process
- ✓ Sensors fabricated and tested with good general performance
  
- Future work
  - Complete tests on new devices with  $\text{TiSi}_2$  and HDPoly
  - Laser tests on alternative technological solutions
  - Tests after irradiation

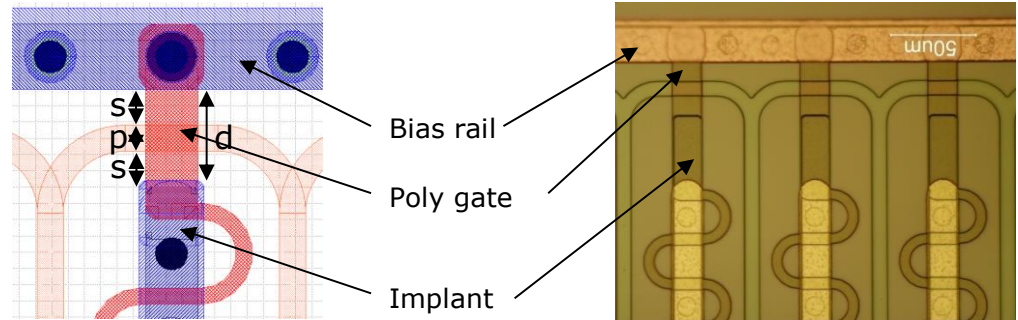
# Extra slides



## ➤ PTP design:

- Design of experiments (DOE): varying  $p$ ,  $s \Rightarrow d$

DOE		N-P separation 's' [ $\mu\text{m}$ ]		
		12	8	6
P-stop width 'p' [ $\mu\text{m}$ ]	8	32	24	20
	6	30	22	18
	4	28	20	16
Total PTP distance 'd'				



## ➤ Wafer design:

- 10 ATLAS-barrel-like sensors: **“LowR sensors”**
  - 64 channels,  $\sim 2.3$  mm long strips
  - First metal connected to the strip implant to reduce  $R_{\text{strip}}$
  - Each sensor with a different PTP geometry (with polysilicon bridge)
- 10 extra **standard sensors** for reference (no metal in implant). Identical design to the LowR but without metal strip on top of the implant

