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# Edge TCT measurements on irradiated HVCMOSv3 sensors

CERN Summer student
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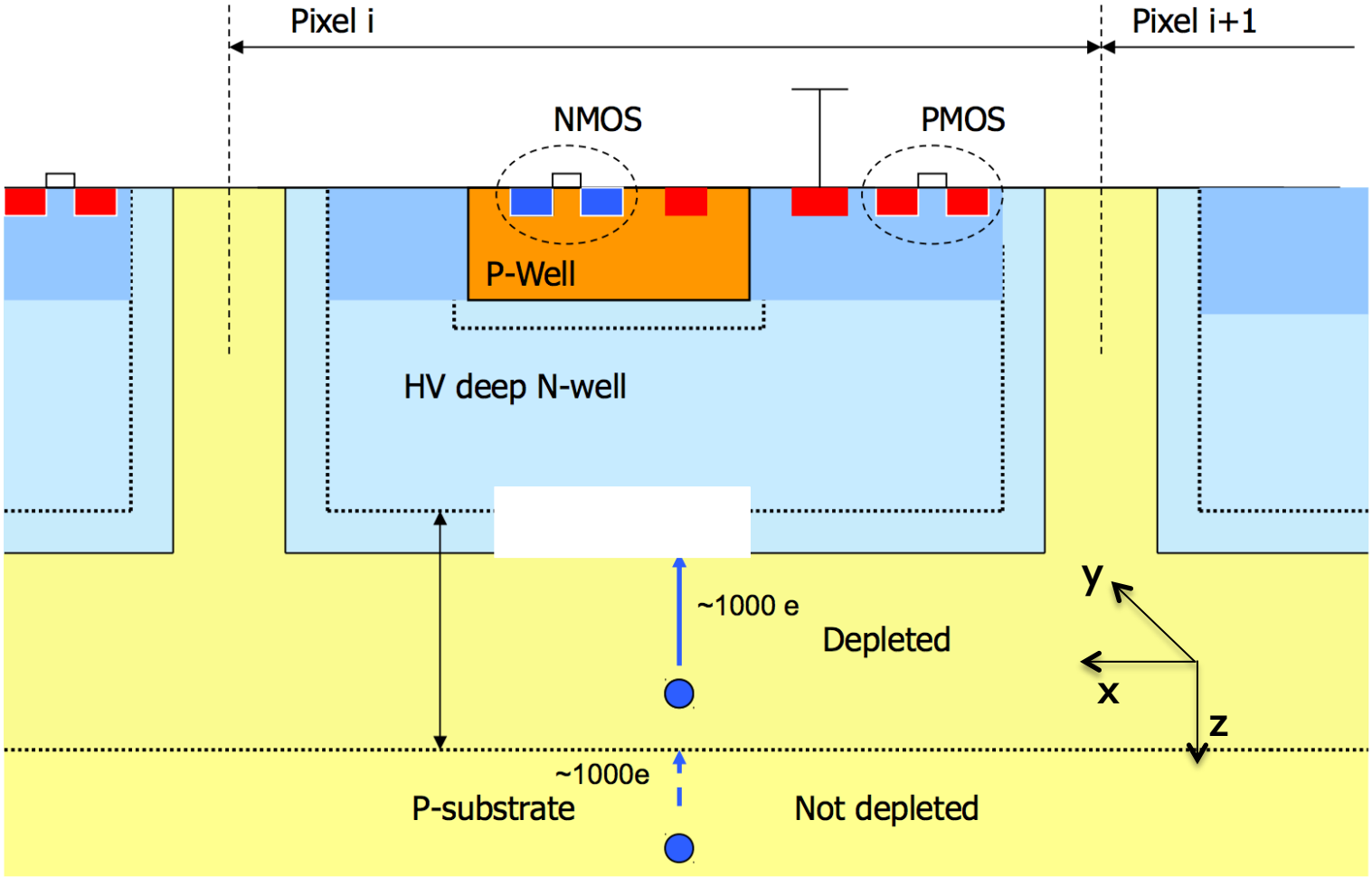
# Background

- ATLAS is investigating HV-CMOS for HL-LHC upgrades for pixel and strip applications
- A few prototypes have been analysed.
- One of them is HV2FEI4v3 (HV CMOS coupled to FEI4 readout chip) designed by Ivan Peric.

# HV – CMOS structure

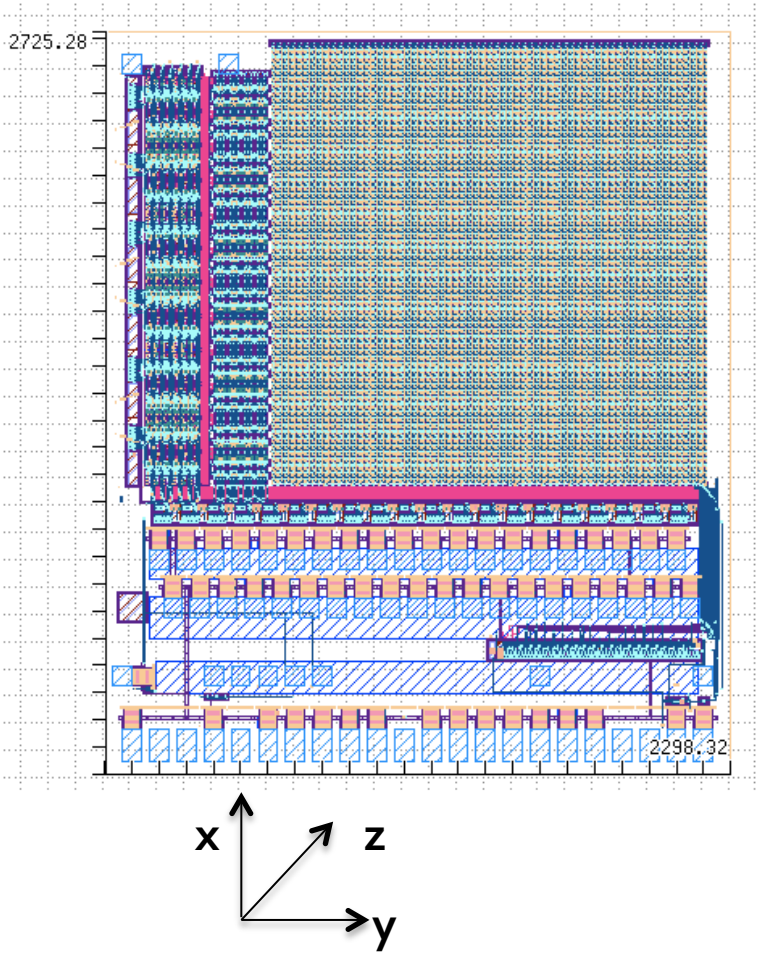


# HV-CMOS structure

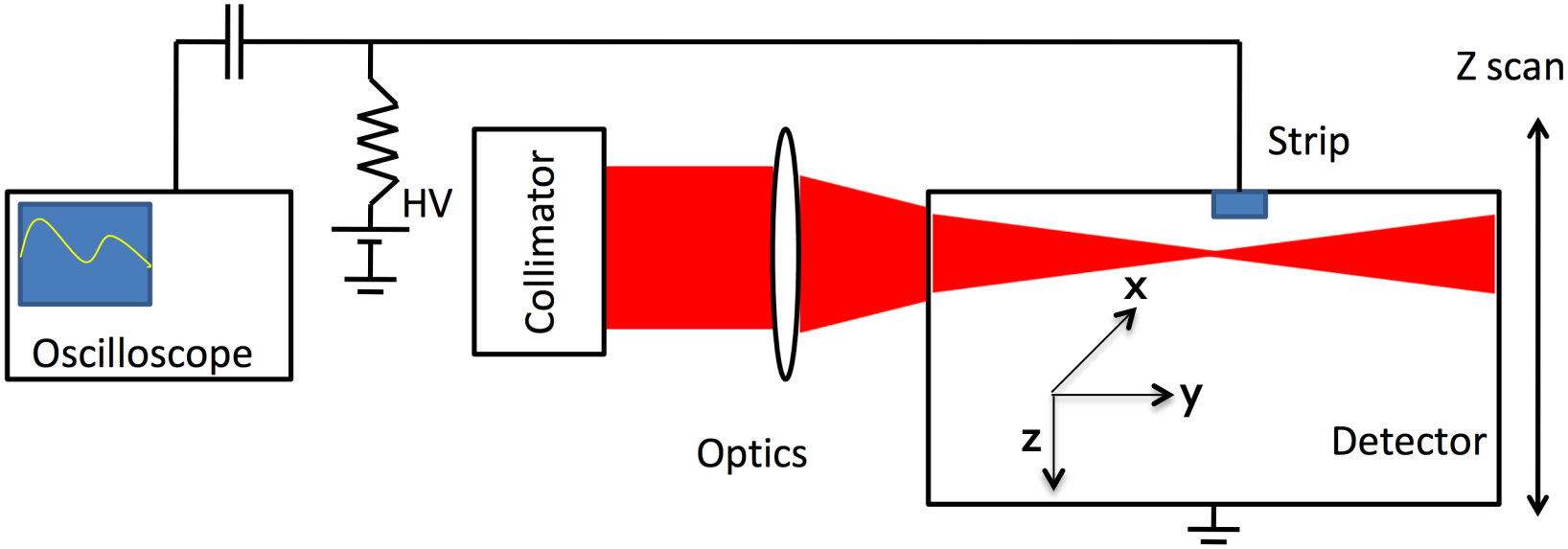
- Monolithic
- The n-well depth is increased significantly wrt standard MAPs and is built on a medium resistivity p-type substrate
- Small depletion region (~10 μm)
- The depleted region allows quick charge collection
- Diffusion occurs around the depleted region
- Can be used as pixel or strip detector

# Introduction to HV2FEI4v3

- Chip 2.73 x 2.30 x 0.23 mm with Pixel matrix
- Square passive test diode of length 100 μm was investigated.
- Four samples (thermal neutron irradiation at Ljubljana, thanks !):
- 0, 1, 7, 20 x $10^{15}$ $n_{eq}$ $cm^{-2}$
- Essential to understand the sensors' charge collection properties ➔ Edge TCT

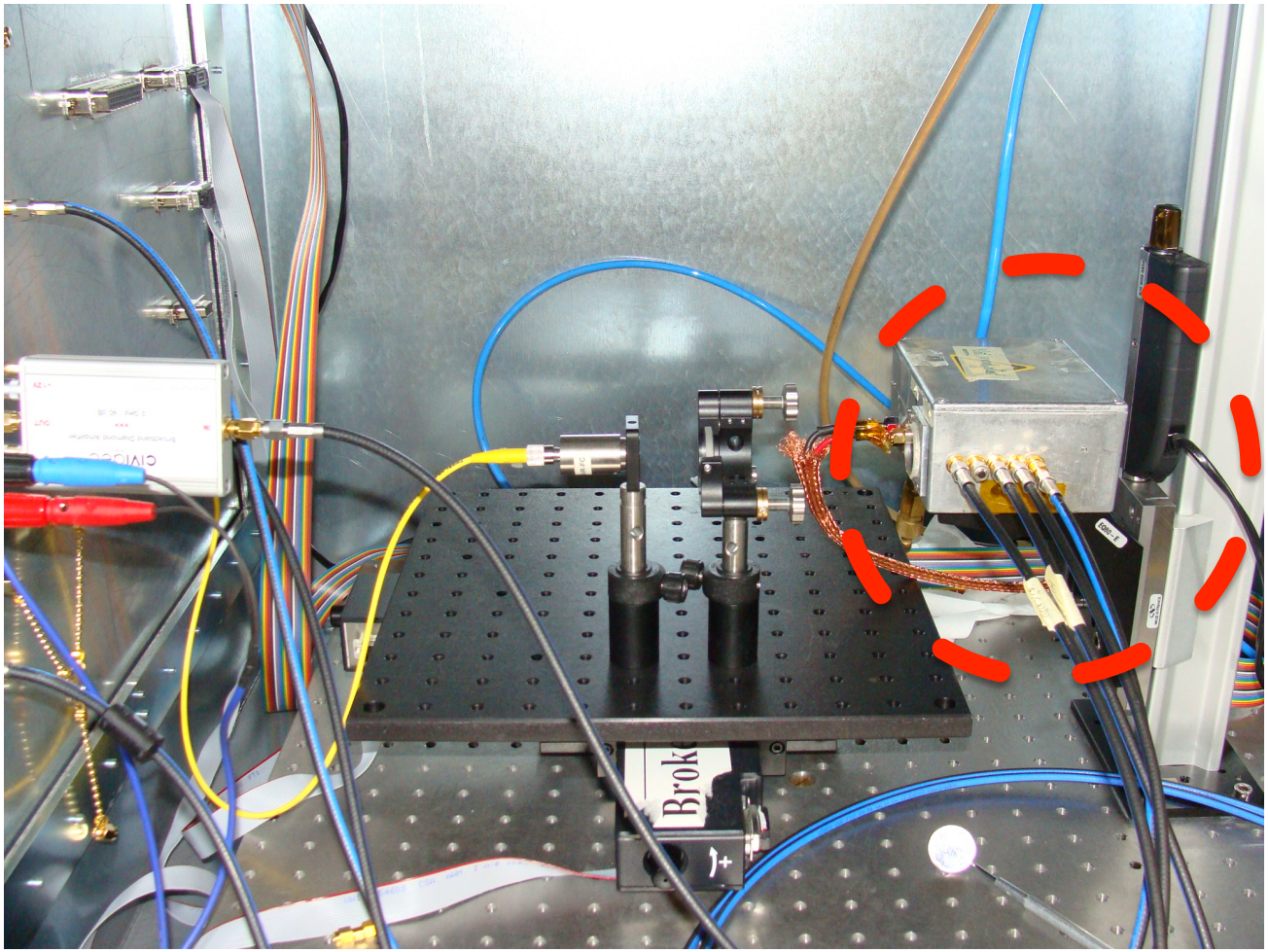


# Edge TCT principle

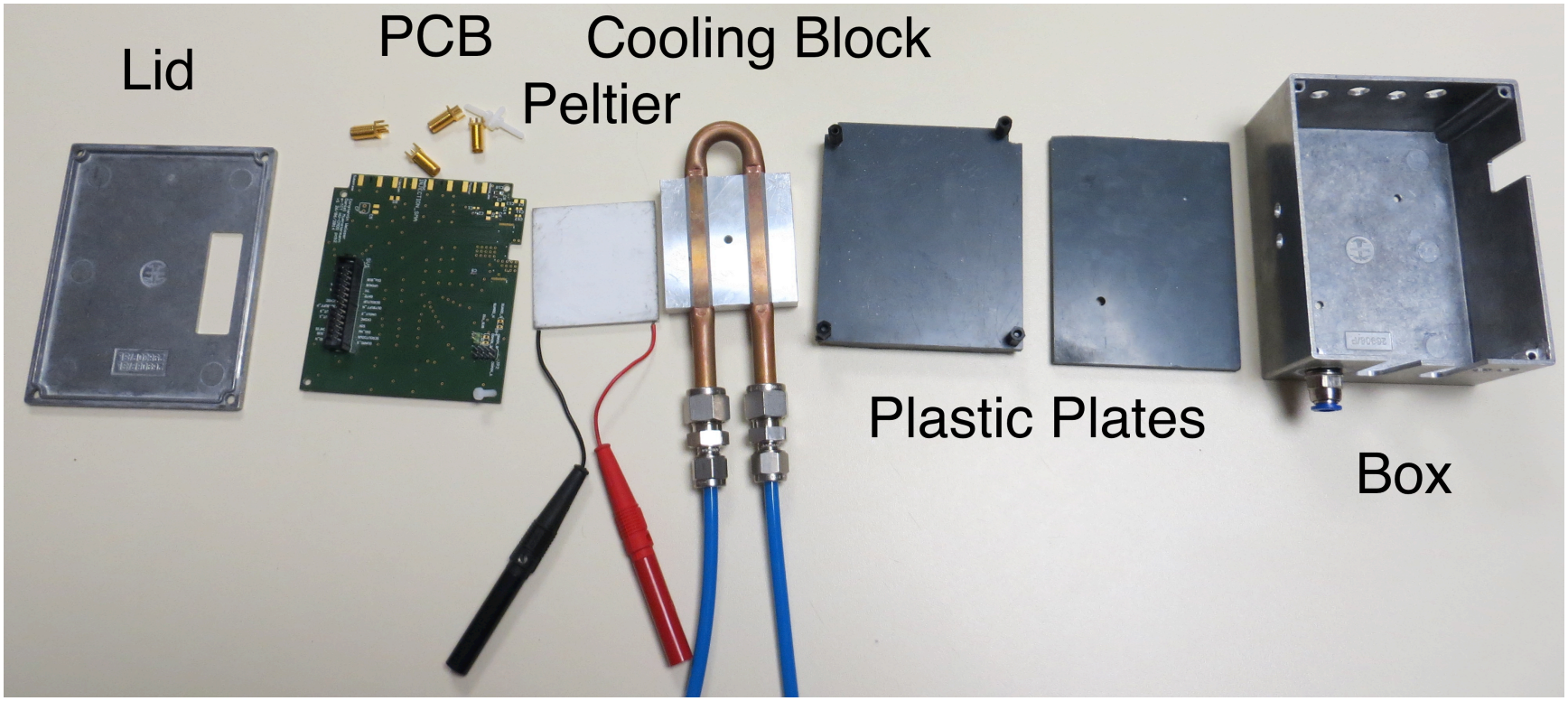



- Photon pulses from an infrared laser are focused in the detector.
- These photons then create electron-hole pairs that produce a signal.
- At the focal point the Gaussian $\sigma$ was 8 $\mu$m.

# eTCT apparatus CERN

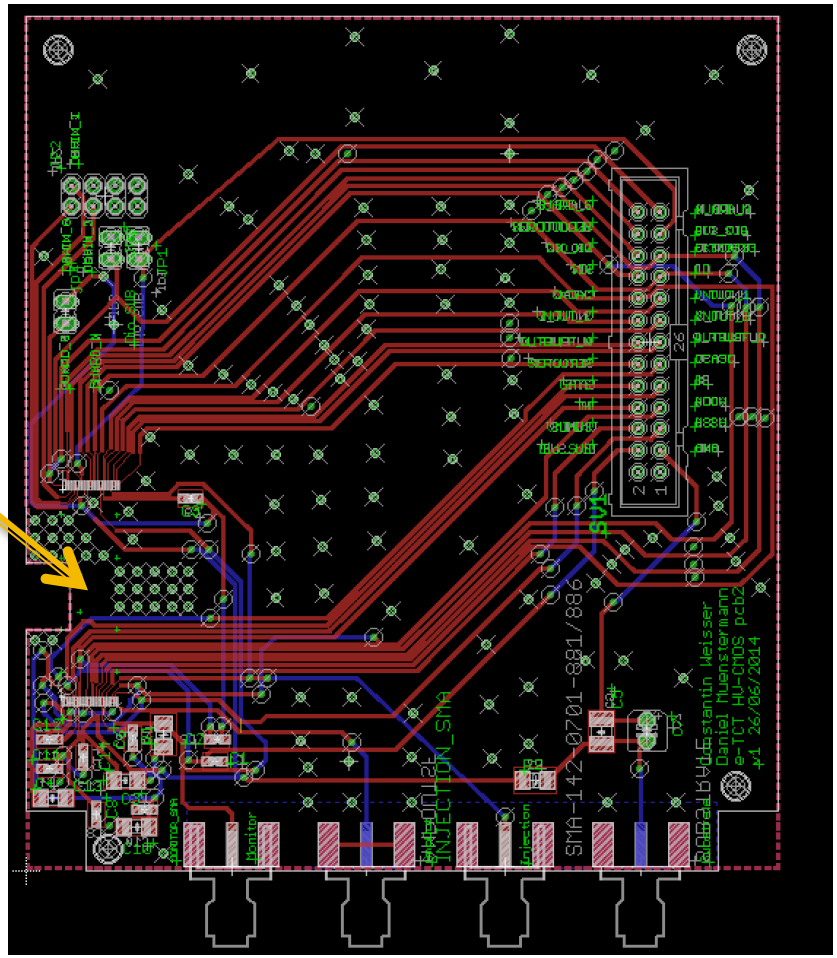


# Integration of HV CMOS and eTCT

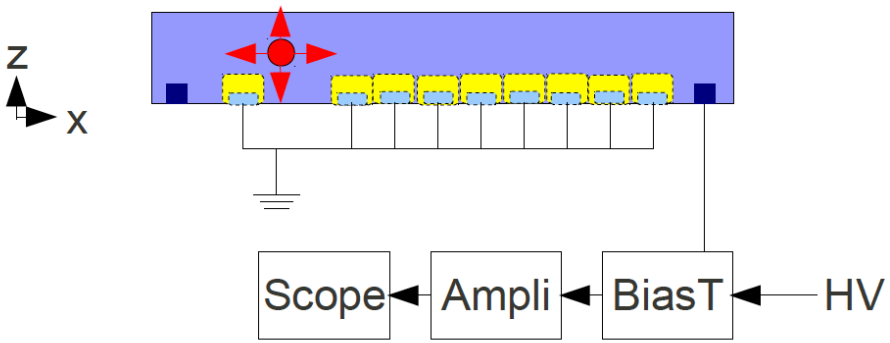


# PCB for readout

- Supports HV2FEI4 version 2 and 3
- No components near the sensor
- Vias for better heat transfer
- Readout of output of preamplifier of pixels possible

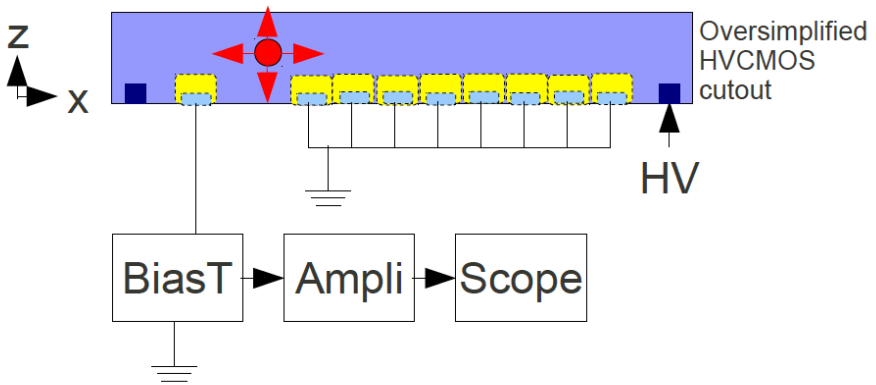


# Readout Configurations




Configuration 1: Full chip readout

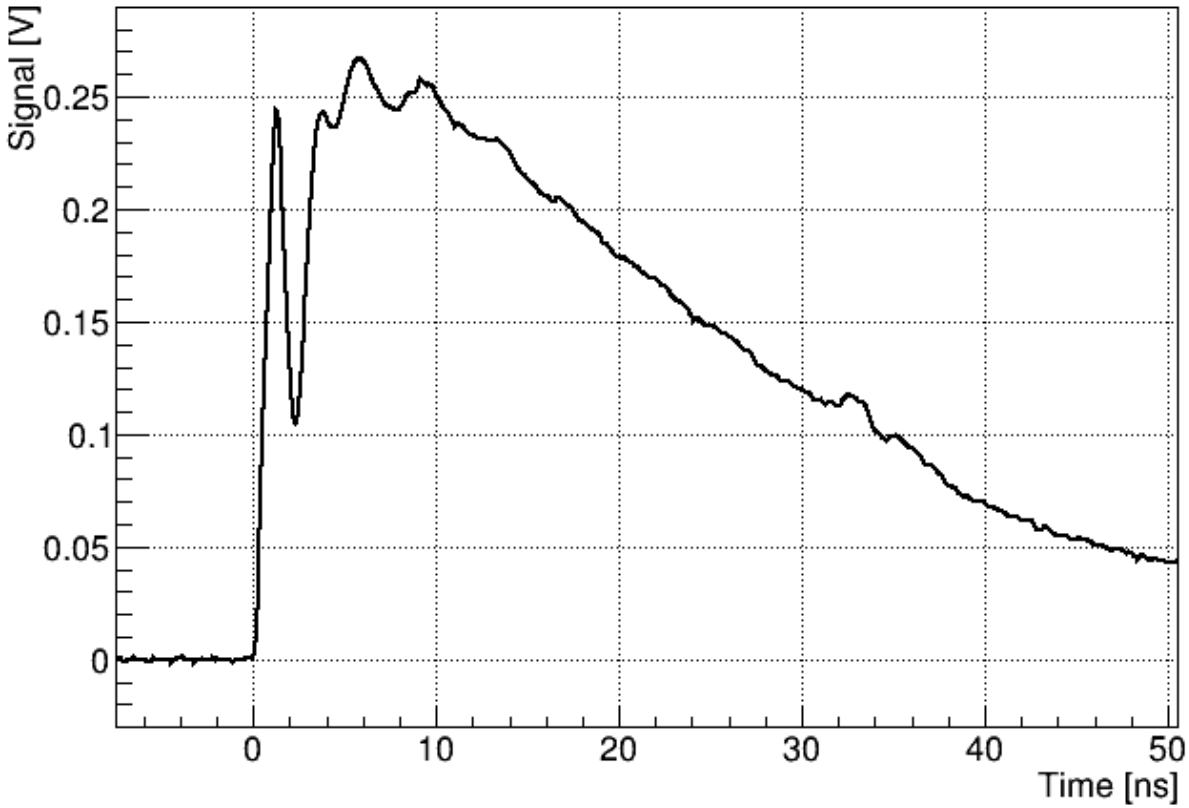
Applying a bias depleted the whole chip, which made it easier to find the active region




Configuration 2: Diode readout

Only the diode's signal was read out.

# Slow and fast signals for HVCMOSv3

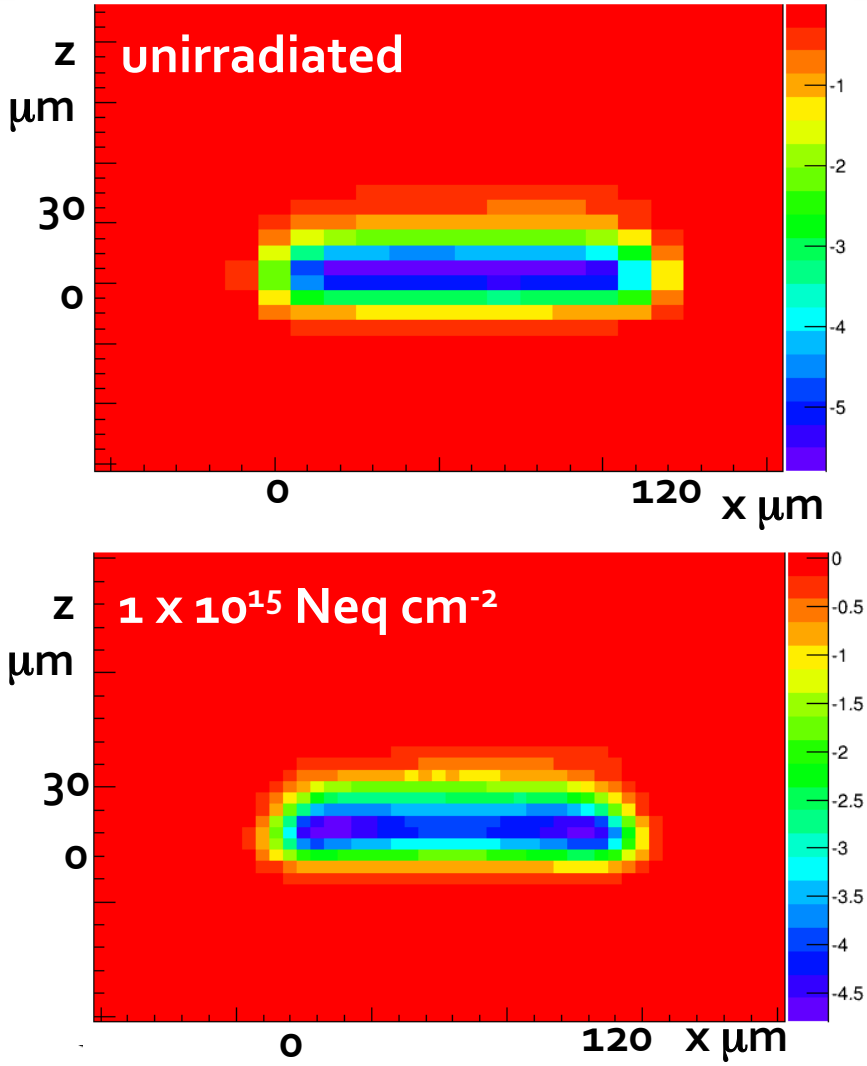



- "Fast" ( < 3 ns) and "slow" ( > 3ns ) contributions later interpreted as due to drift and diffusion, respectively.

Configuration 1

# Charge of quick signal ( < 3 ns )

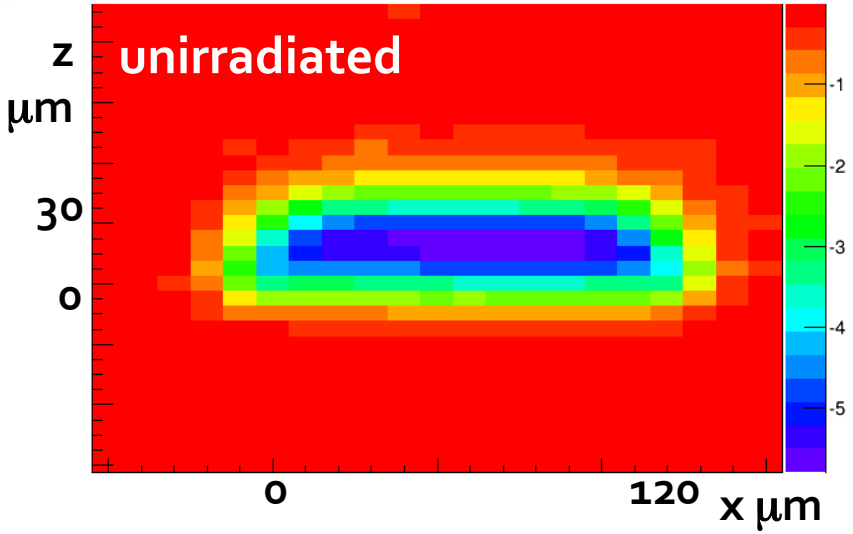
- Charge maps as a function of position in x and z
- For both samples the active region was slightly bigger than the width of the diode (100 μm) due to convolution with the laser .
- This region was interpreted to be the depletion region and had similar properties in both cases.

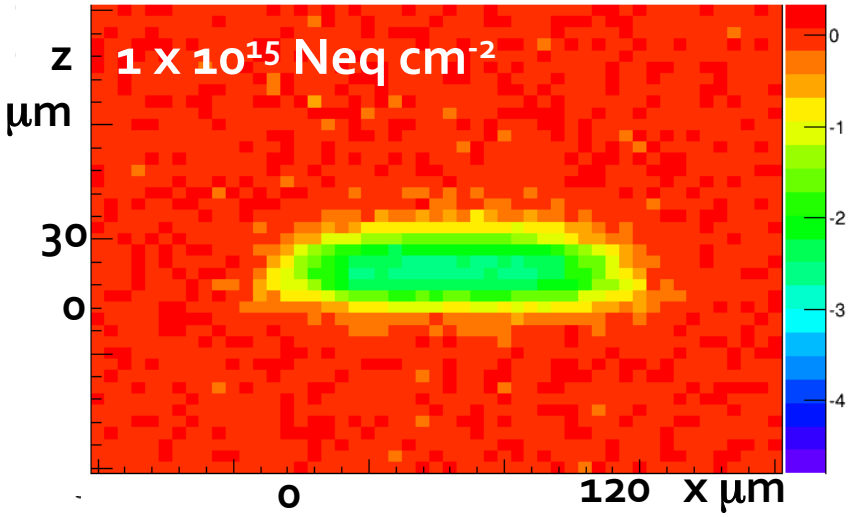



Measured at RT and -60 V

# Charge of slow signal ( 25 > t > 3 ns )

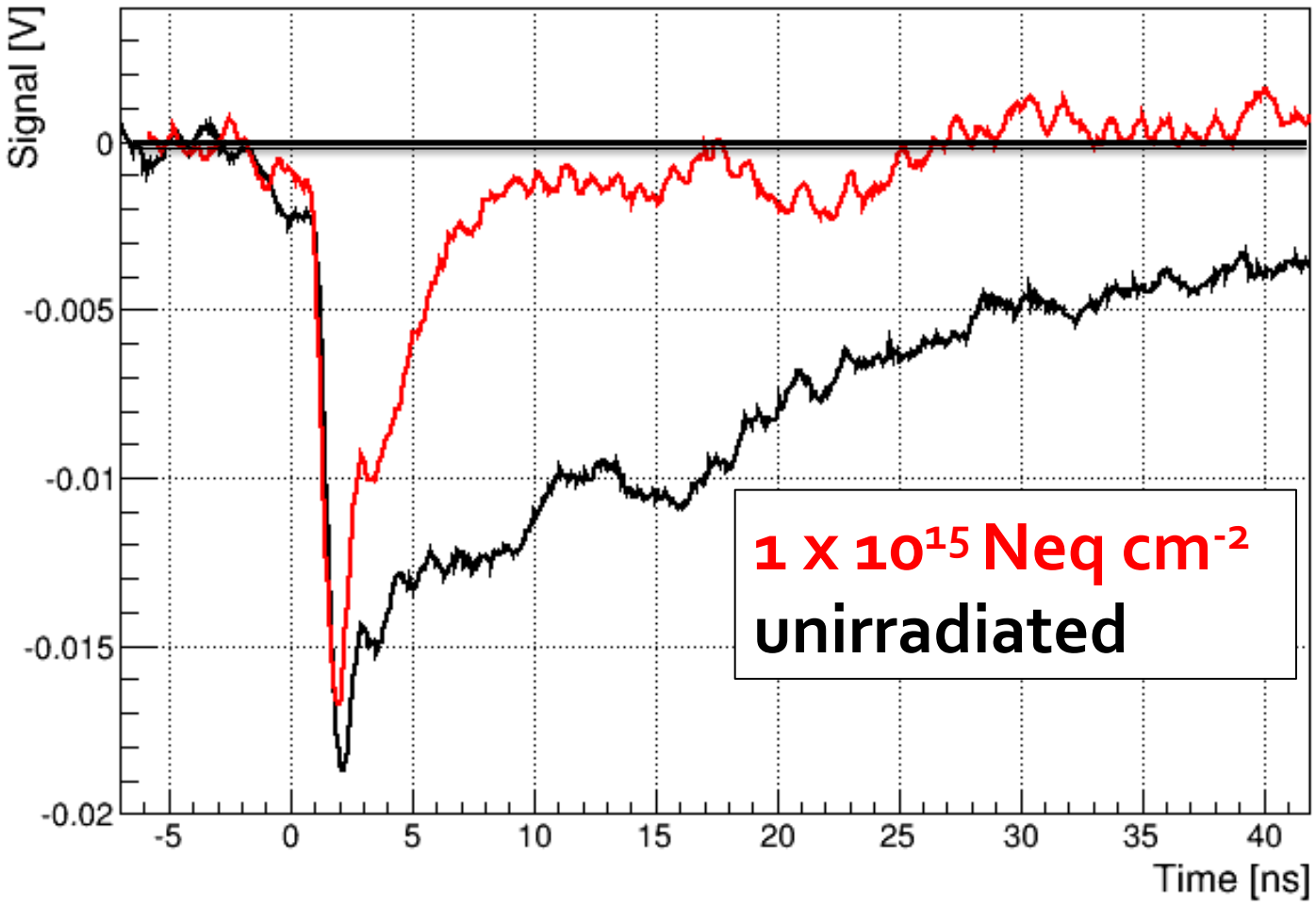
- For the unirradiated sample, there was a distinct slow charge of the same order of magnitude as the quick charge.
- For the irradiated sample this signal was significantly reduced.



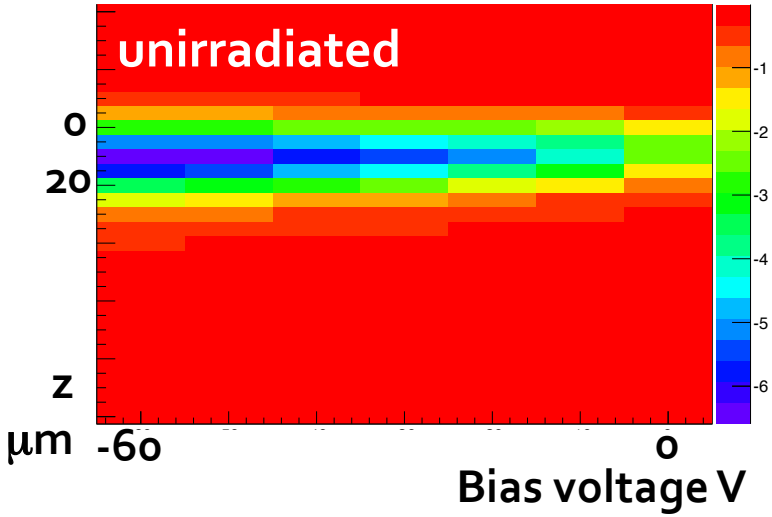

Measured at RT and -60 V

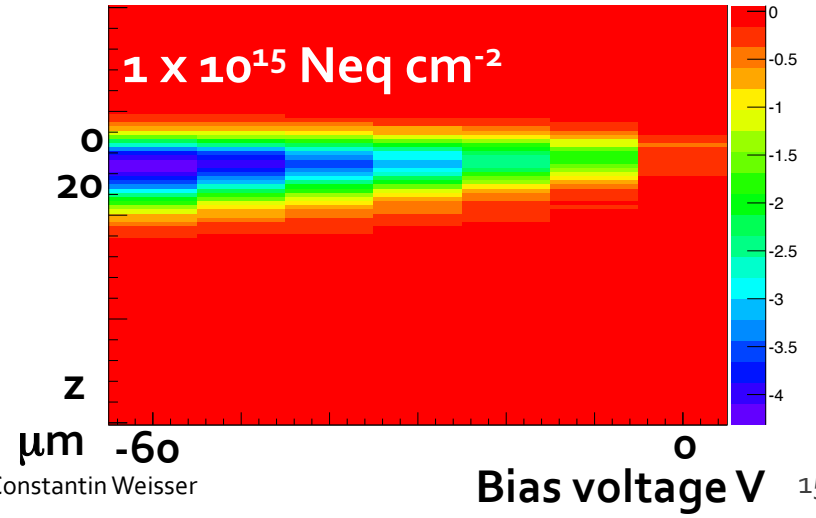
# Transients in region of slow charge



# Charge of quick signal bias voltage dependence

- Charge collected over 3 ns as a function as a bias voltage and depth of the detector
- The quick charge zone increased with bias
- Irrad 0 V: quick charge is significantly lower than for the unirradiated sample.



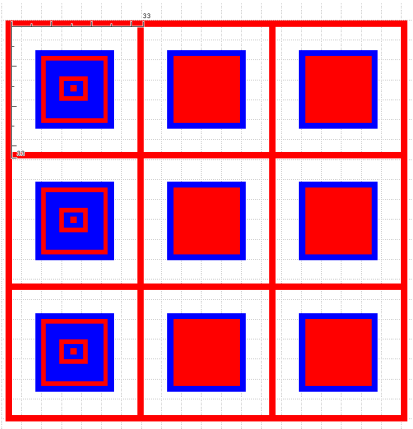

Measured at RT

# Findings

- When the HV2FEI4v3 sensor was irradiated its slow signal was reduced.
- A possible explanation could be trapping of charge carriers with expected mean lifetimes in the ns regime.
- The amplitude of the fast signal did not differ much between irradiated and unirradiated samples, while the slow signal was significantly reduced for the $1 \times 10^{15}$ $n_{eq}$ $cm^{-2}$.

# Outlook

- The reflections could be reduced by the professional design of a PCB with impedances of 50 Ω.
- In a new prototype (HVStripv1) the test diode has been included in a pixel matrix which will be read out.

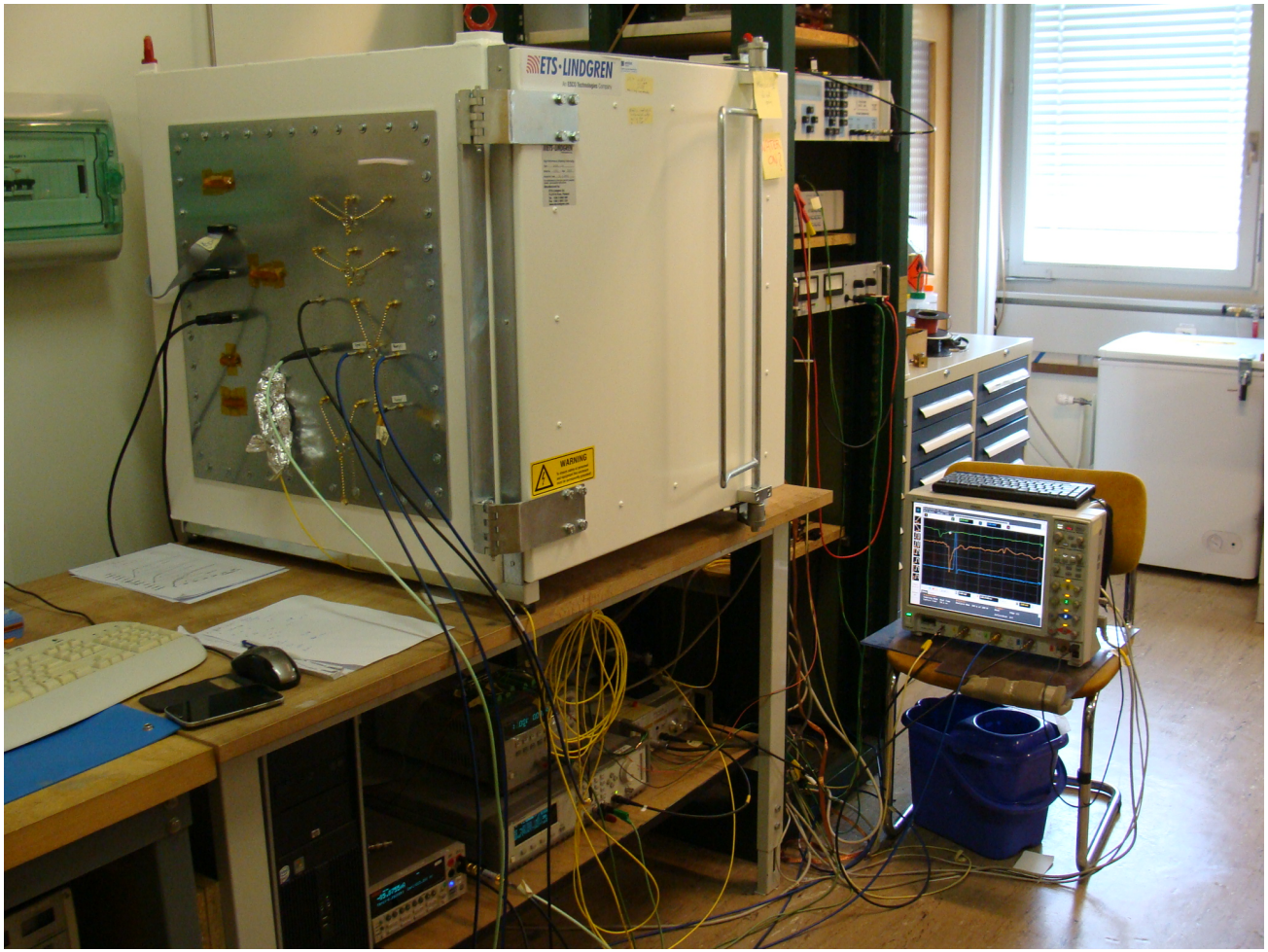


# Backup slides

# Acknowledgements


- Supervisor: Daniel Muenstermann
- Supervisor: Michael Moll
- PH-DT-DD-SSD: Marcos Fernandez Garcia
- PH-DT-DD-SSD: Christian Gallrapp
- Workshop: Pierre-Ange Giudici
- Wirebonding: Ian Mcgill
- Wirebonding: Florentina Manulescu
- Wirebonding: University of Geneva

# CERN PH DT DD SSD eTCT setup



# Box dimensions

## HV CMOS eTCT Box

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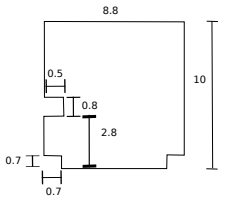
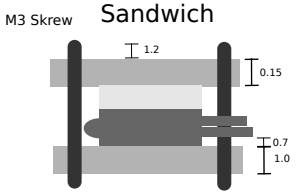
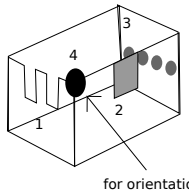
PCB



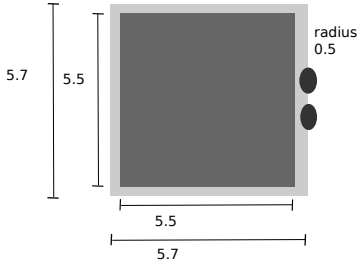

Side view Sandwich



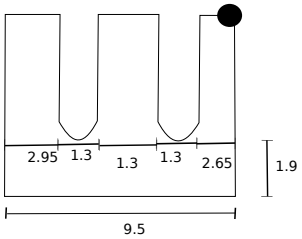

3D View Box Sides numbered



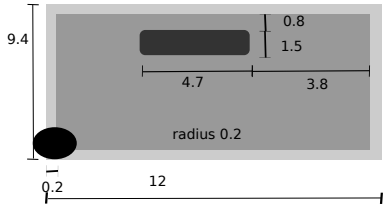

Top View Peltier Cooling Block




Box with slits Side View (1)




Box Lid Top View (3)




All lengths are in cm

## HV CMOS eTCT Box II

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Laser Side Side View (2)