

Temperature Impact on Timing, Trigger and Control Systems for High Energy Physics Experiments

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Introduction (1 of 5)

■ PH-ESE

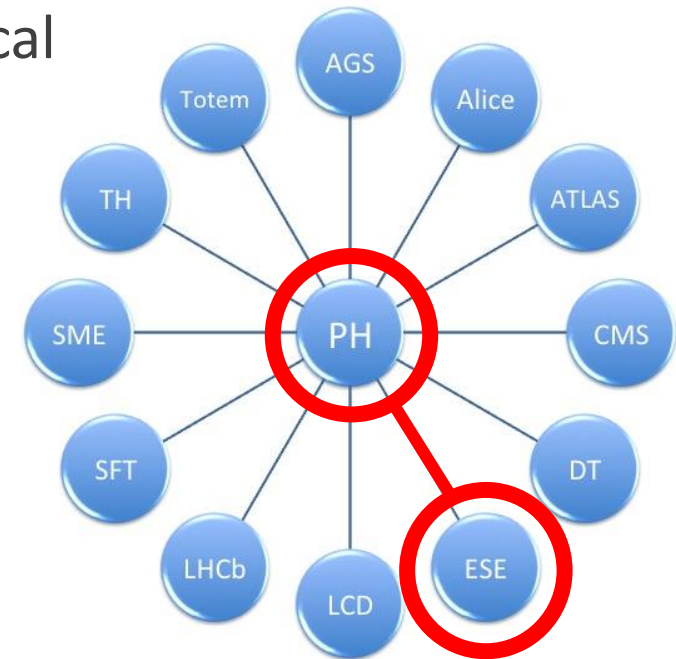
□ Physics Department (PH)

Carries out basic research in the field of experimental and theoretical particle physics.

□ Electronics Systems for Experiments Group (ESE)

(Group leader: P. Farthouat)

- BE – **Back End** Systems Section; Group Leader: F. Vasey
- FE – **Front End** Systems Section; Group Leader: F. Anghinolfi
- ME – **Microelectronics** Section; Group Leader: M. Campbell



Introduction (2 of 5)

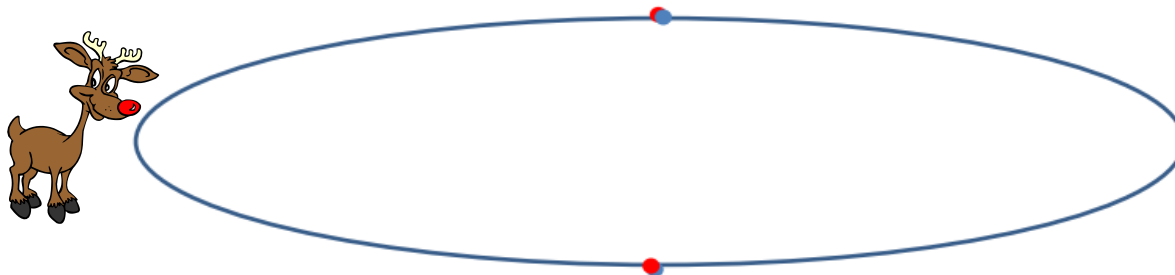
□ Time, Trigger & Control (TTC) system

Provides distribution of:

- ✓ synchronous **timing** with Bunch Clock(40.079MHz)*
- ✓ the level 1 **trigger** command
- ✓ broadcast and individually-addressed **control** commands

} Single optical fibre

***The Bunch Clock** is the frequency at which an observer sitting close to the ring could 'see' particles passing [1]



Simplistic case:

2 bunches,
2 beams,
1 observer

Introduction (3 of 5)

Jitter

Cycle-to-cycle Jitter

Short term variation in the clock period between adjacent clock cycles;

Period Jitter

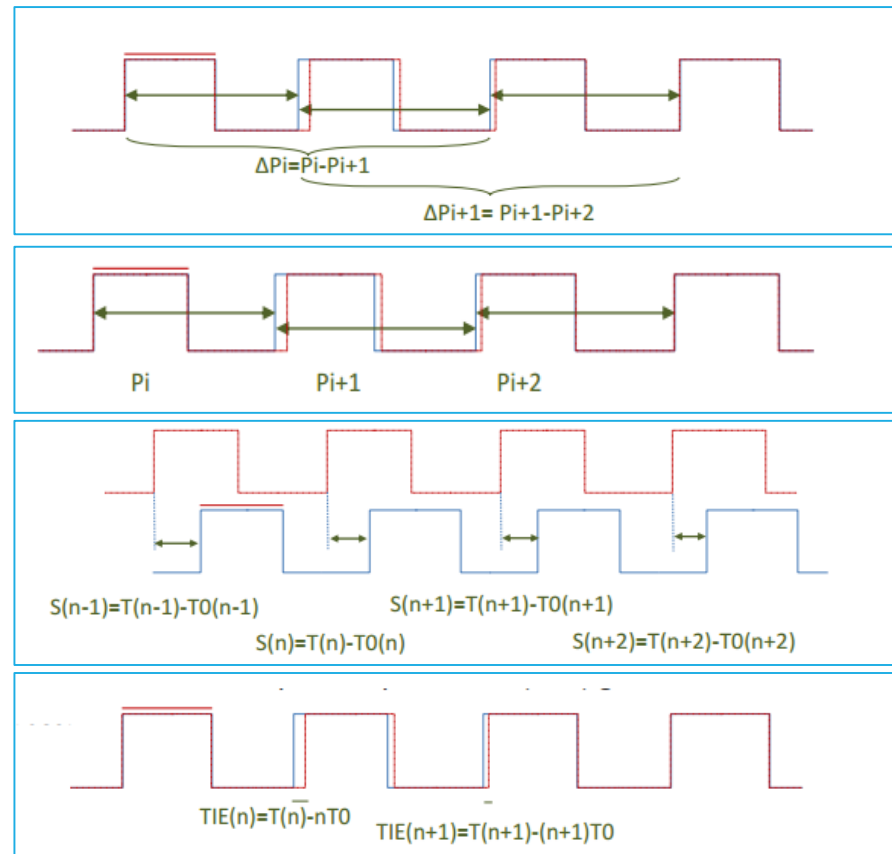
Short term variation in the clock period over all measured clock cycles, compared to the average clock period;

Skew Jitter

Phase error between the reference clock and the measured clock over all clock periods;

Time Interval Error Jitter

Actual deviation from the ideal clock period over all clock periods.



Introduction (4 of 5)

Jitter

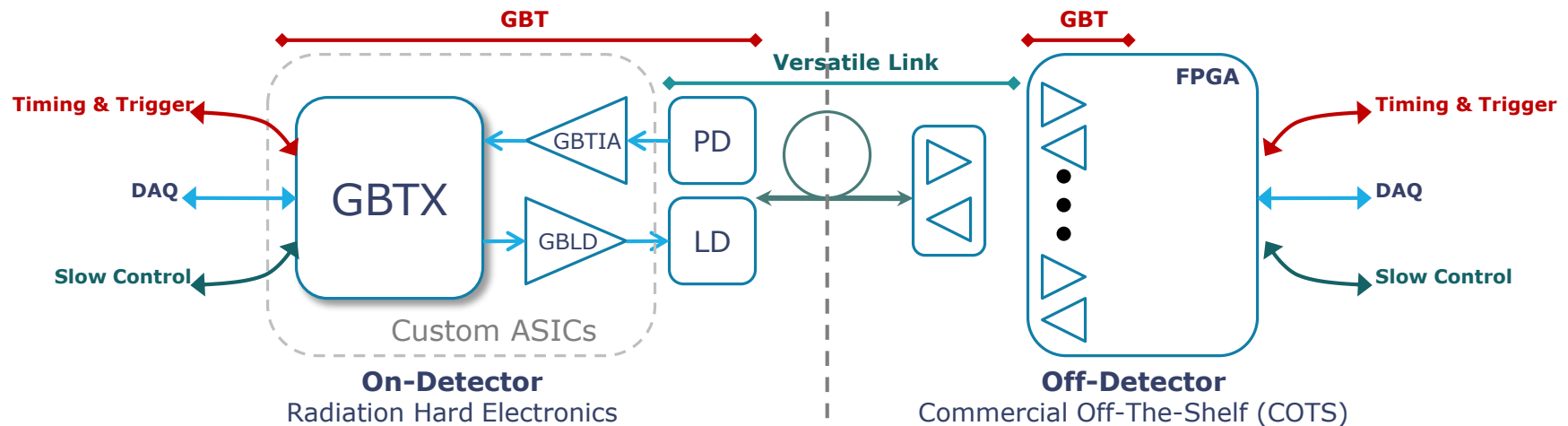
How temperature affects TTC systems?

Jitter varies with temperature!!

Introduction (5 of 5)

GBT project

- The **HL – LHC** will increase the amount of data (by 2020)
- A new **GBT – based high-speed rad-hard optical link under development**
- Most of LHC upgrades adopt the new GBT – based link (LHC, CLIC, ATLAS, CMS, ALICE, LHCb etc.)



The GBT-FPGA team: Mrs. Baron & Mr. Barros Marin

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Project Overview

Objectives

- ✓ Characterization of several components of a TTC system in terms of **Jitter VS Temperature**
- ✓ Verify the data transmission/reception with **fixed and deterministic latency capabilities of the GBT-FPGA** under different conditions (e.g. after power up, reset, temperature variations, etc.) with different FPGAs

Approach

- ✓ Implementation of a **fully automated test bench**

THEORY is when you know everything but nothing works.

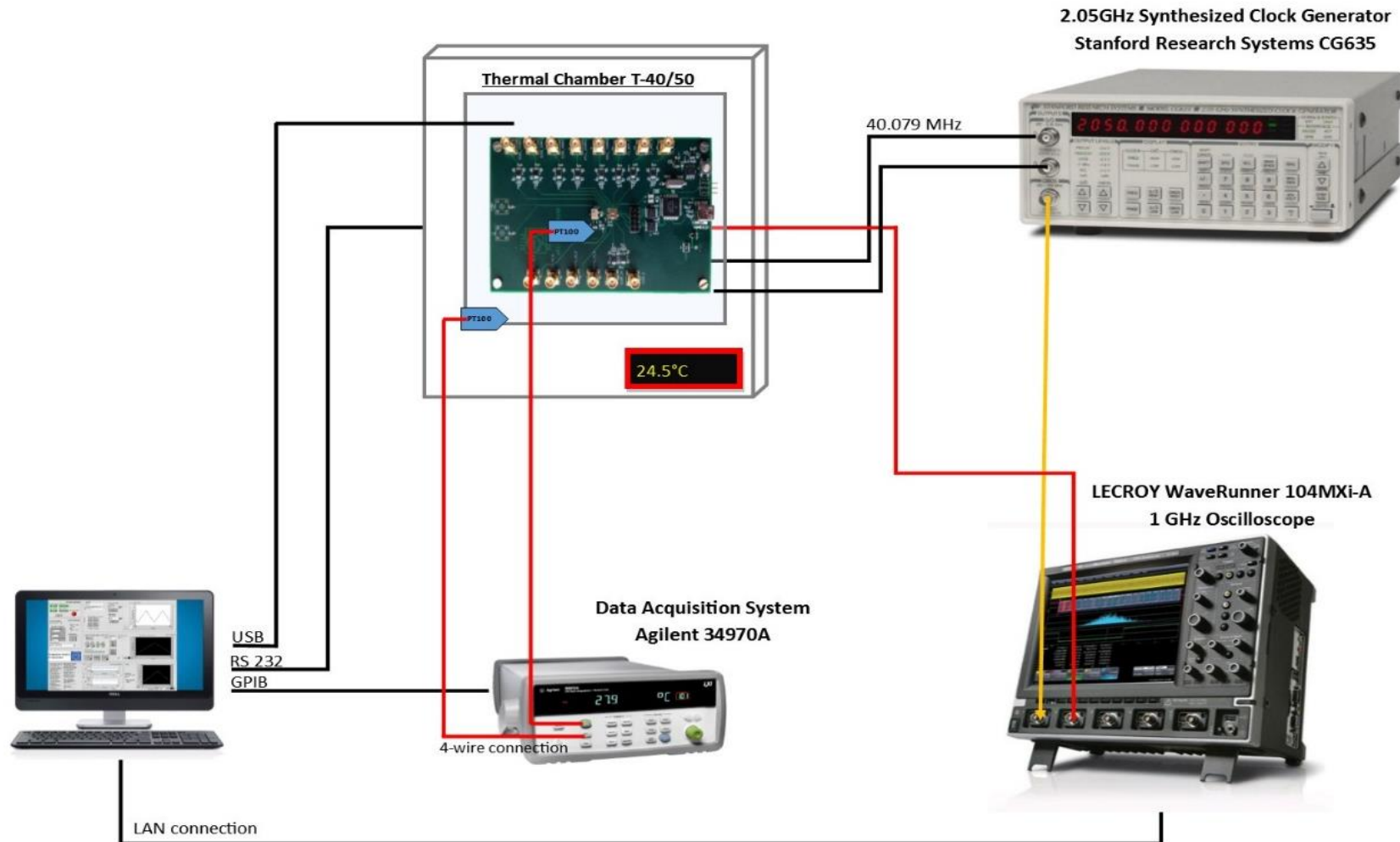
PRACTICE is when everything works but no one knows why.

In this lab, THEORY and PRACTICE are combined: nothing works and no one knows why.



Project Overview

Fully automated test bench



Project Overview

Fully automated test bench

Software :

Labview 2013

Python

TCL

Matlab

The screenshot displays a comprehensive LabVIEW test bench interface for a thermal chamber experiment. The interface is organized into several functional panels:

- Main Control Check Points:** Features status indicators for Thermal Chamber (OK), Oscilloscope (OK), Agilent 34970A (OK), and Phase Analyzer (Not connected). A prominent red Emergency Button is also present.
- VISA Agilent:** Configures the GPIB interface (GPIB0::8::INSTR) and provides Reset and Don't Reset options.
- Serial Port Configuration:** Sets the Serial Port (VICP::10.0.0.9::INSTR), Timeout Value (5000), Baud Rate (9600), and Flow Control (None).
- Channels:** Shows the Transducer Type (4-Wire RTD) and a table of Output Data from 2 Channels:

	Sensor1	Sensor2
1	27.54	32.008
0	27.772	31.843
	26.88	31.472
	25.674	30.932
- Graph of Temperature:** A real-time plot showing temperature oscillations between approximately 10°C and 60°C over time.
- MEAN Values and Standard Deviation:** Fields for calculating and saving statistical data to files.
- Control for FPGA:** A status panel with various LEDs and buttons for TX/RX link status, PLL locking, MGT Ready, and a General RESET button.
- Temperature Impact on Timing Systems:** A panel with a CERN logo, Start Value (021.9), SENT Temperature (10.45), and a START button.
- Oscilloscope LECROY:** A panel for timing analysis with fields for STD Period, Mean Period, STD TIE, Mean TIE, STD Skew, Mean Skew, STD Cycle to Cycle, Mean Cycle to Cycle, STD Period, Mean Period, STD Skew Between Flags, and Mean Skew between Flags.
- STD Skew Between Flags:** Two plots showing skew values over time.
- Timing:** A panel showing Duration of the experiment (21600 s) and Elapsed Time (0 s), along with a Temperature Sweeps graph.

Project Overview

Fully automated test bench

Firmware:

Language: VHDL

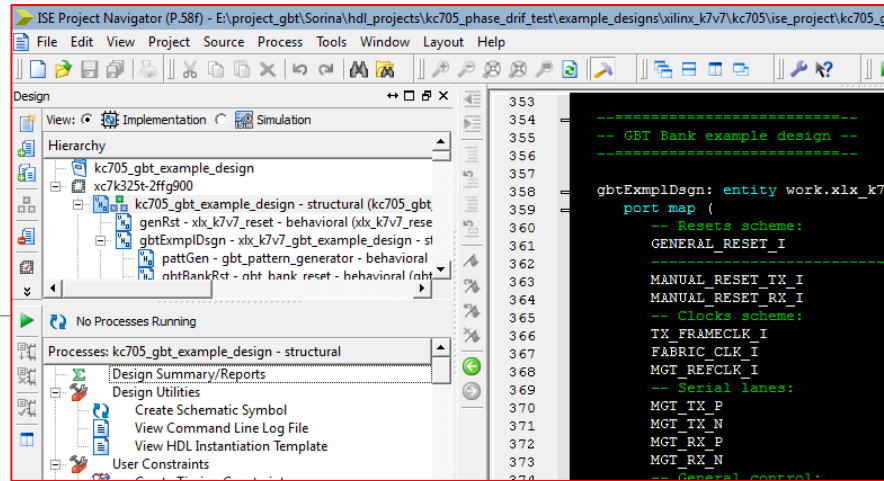
EDA tools:

➤ Xilinx:

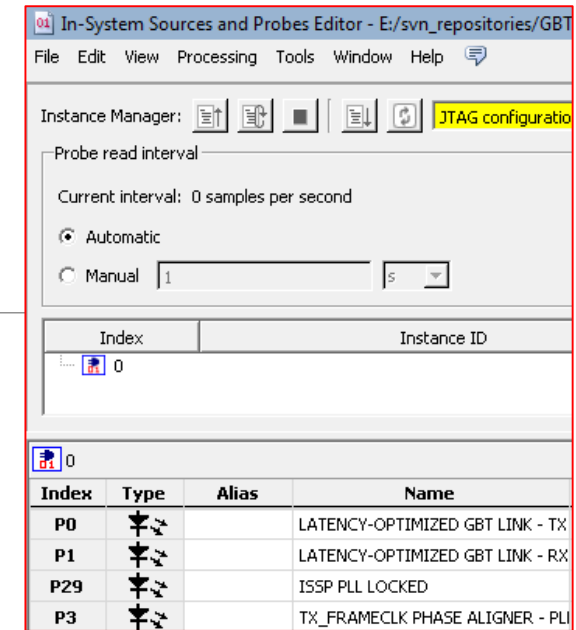
- ISE
- ChipScope

➤ Altera:

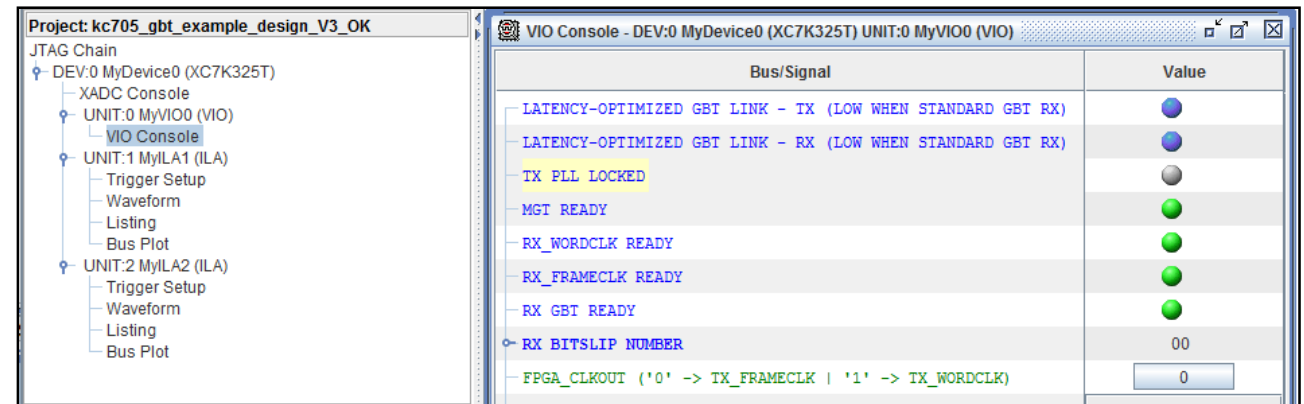
- Quartus II
- In-System Sources & Probes



ISE (Xilinx)



Quartus II (Altera)



ChipScope (Xilinx)

Project Overview

Example of Device Under Test (DUT)

Attention!

Before starting the tests, remove all non-electronics objects!

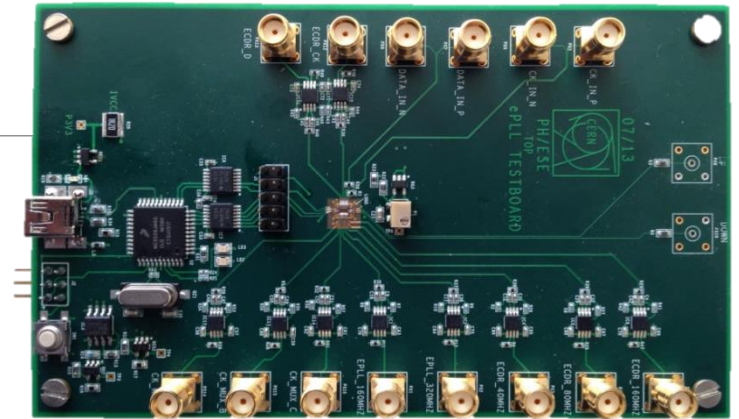


Project Overview

Example of Device Under Test (DUT)

eCDR-PLL test chip (Clock and Data Recovery)

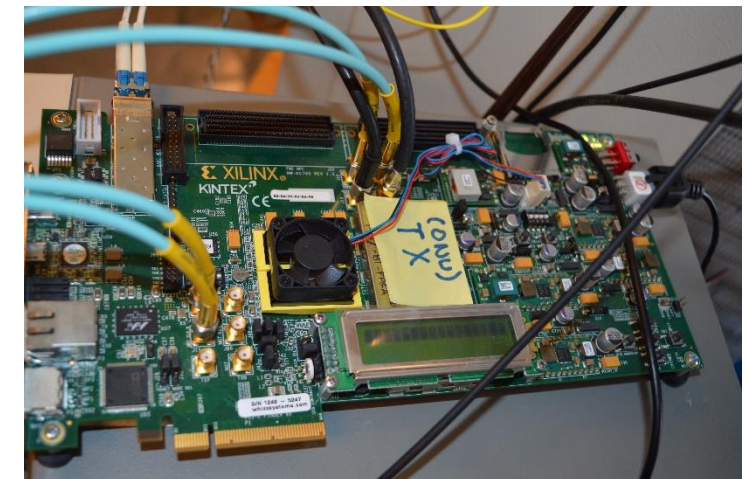
- data rate: 40, 80, 160 or 320 Mbit/s;
- output clocks: 40, 80, 160 and 320 MHz;
- **Tests performed:** jitter evaluation for several clock and data inputs versus temperature (reset or no reset of the board).



eCDR Board

GBT – FPGA core on Xilinx FPGA (Kintex 7)

- Board: kc705
- Optical link at 4.8Gbps
- Connectivity
 - Loopback
 - Board-to-board
- **Tests performed:** Clocks skew jitter and data latency evaluation versus temperature (reset or no reset of the board)



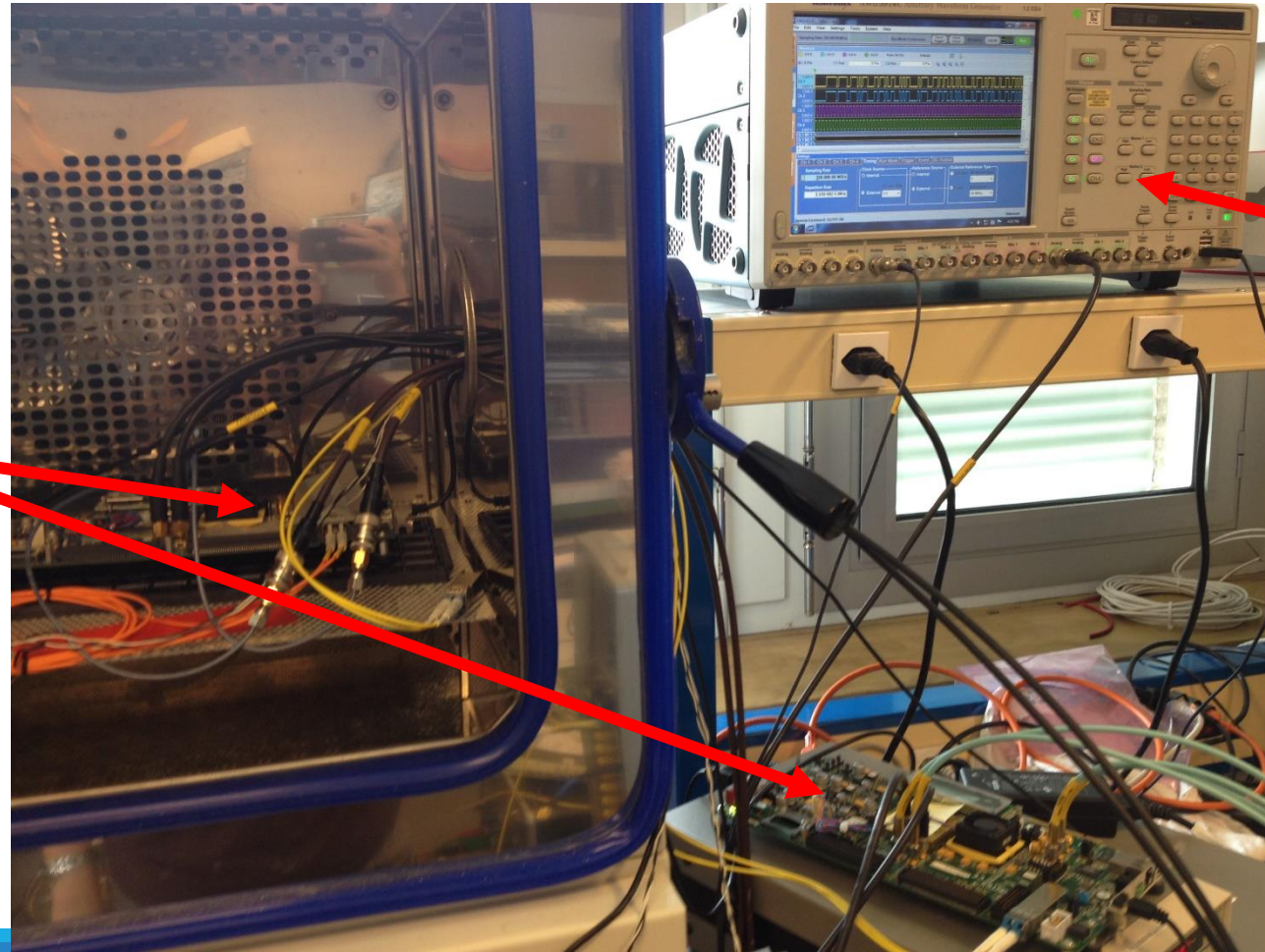
GBT – FPGA on KC705

Project Overview

Example of Test Implementation

Implementation:

Two FPGAs
communicating
with each other



Waveform
Generator

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Example results

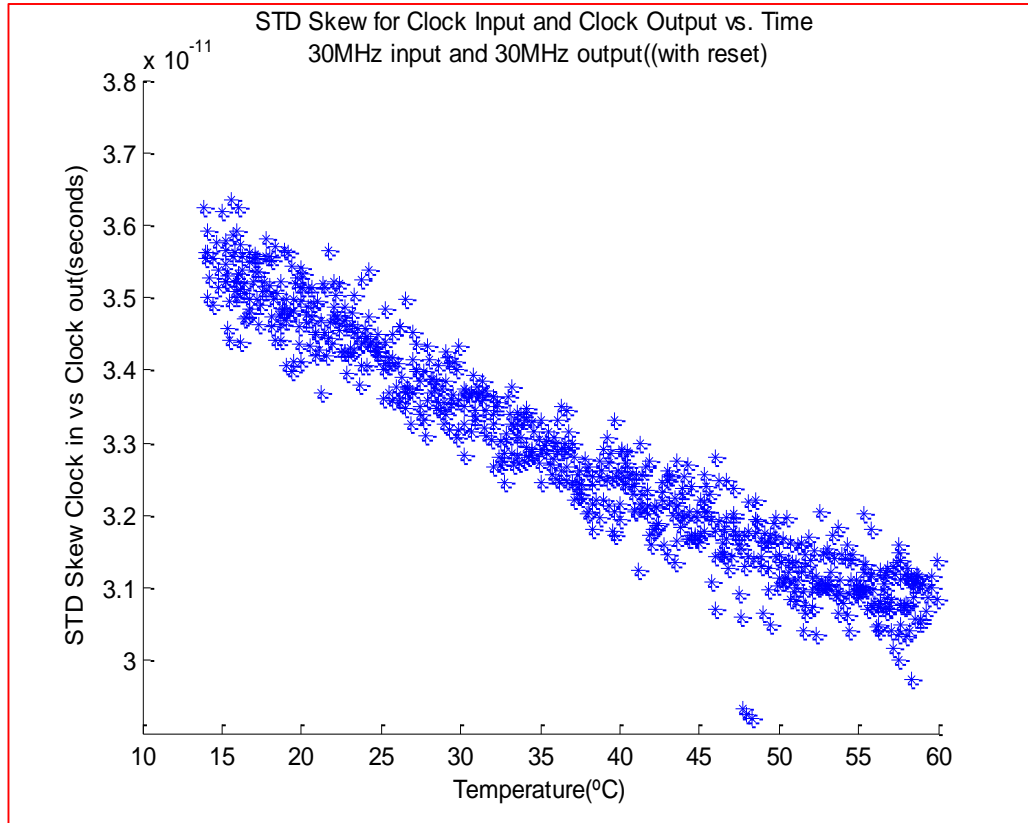
eCDR (Clock and Data Recovery)

Type of Test	Jitter	Mean Values			Standard Deviation Values		
		Min Temp (10°C)	Min Temp (60°C)	Δ	Min Temp (10°C)	Min Temp (60°C)	Δ
eCDR mode with 320Mbps data input (PRBS)	Cycle to Cycle	constant (2 fs)		0	12 ps	14 ps	2ps
	Period	constant (6.25 ns)		0	7.5 ps	8 ps	0.5 ps
	TIE	0	0	0	12.5 ps	11.5 ps	1 ps
	Skew between clocks	0.2 ns	0.3 ns	0.1 ns	17 ps	16 ps	1 ps
	Skew between clock and data	1 ns	0.7 ns	0.3 ns	5.62 ns	5.68 ns	0.06 ns

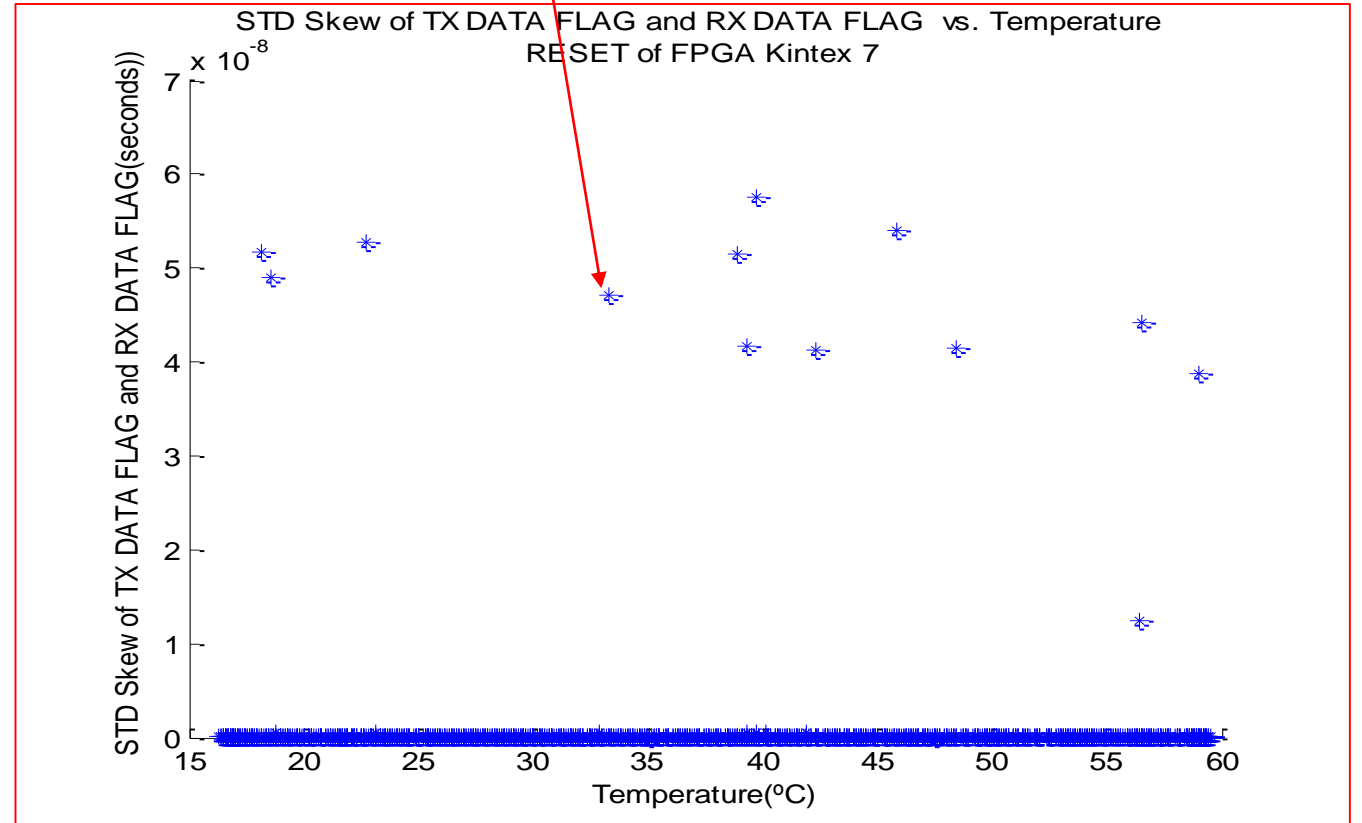
GBT – FPGA on Xilinx FPGA (Kintex 7)

	Skew Value
Standard Deviation	46 ps
Mean	215 ns

Example results



eCDR results



GBT - FPGA results

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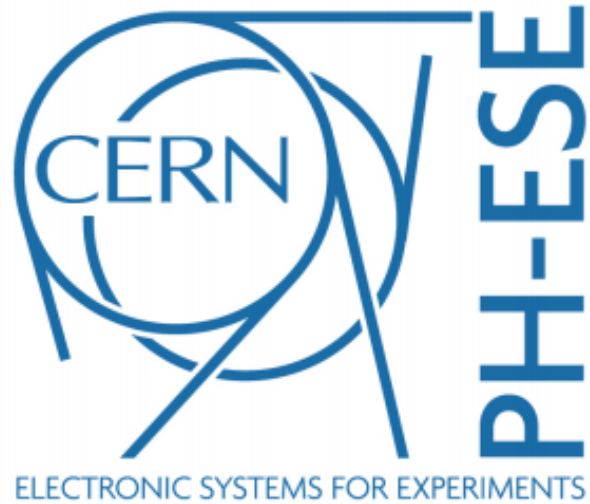
Summary & Outlook

Summary

- ❖ Characterization of jitter and latency of components of a TTC system
- ❖ Implemented fully automated test bench
- ❖ Several units already tested

Outlook

- ❖ **Finish ongoing tests** (e.g. GBT-FPGA on Xilinx FPGA (Kintex 7), Si5338, TTCrq)
- ❖ **Perform new tests** (e.g. LMK32000, GBT-FPGA on Altera FPGA (Cyclone V), TTC-PON clock and data recovery with KC705)



Acknowledgments

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Mr. Pedro Leitao

Mr. Dimitrios Kolotouros

Mr. Marcos Oliveira

Mr. Steven Wilcox

Summer Student Team: Mrs. Roxana Banica, Mrs. Jennifer Dembski and Mrs. Sharon Hobson



References

- [1] The TTC system and Jitter in LHC experiments (Author: S. Baron) PH-ESE seminar 18 Dec. 2012
- [2] GBT – FPGA User Guide (Author: S. Baron and M. Barros Marin)
- [3] Jitter - Impact on clock distribution in LHC experiments (Author: S. BARON) - TWEPP 2012
- [4] A primer on Jitter, Jitter Measurement and Phase-Locked Loops AN687 Silicon Labs
- [5] Jitter Analysis Techniques for High Data Rates – Application Note 1432 Agilent Technologies
- [6] Jitter – Understanding it, Measuring It, Eliminating It (Part I, II and III), High Frequency Electronics (April 2004)
- [7] Jitter and Wander Measurement Guide
- [8] Clock and Data Recovery for Serial Digital Communication, Rick Walker, Palo Alto, California

Units Under Tests

Boards/devices			Standard tests		Additional tests		Contact persons	Priority
			Temperature scan – no reset	Temperature scan with reset	Locking range	Power consumption		
DEVICES	TTCrq	TTCrx	Ok	tbd	x	x	Paulo, Sophie	5
		QPLL	Ok	tbd	x	x		
	Si5338		Ok	tbd	x	x	Peter Lichard, Vito Palladino, Sophie	2
	LMK32000		tbd	tbd	x	x	Dimitris, Sophie	5
	ePLL-CDR	CDR – FM 40MHz	Ok	Ok	tbd	Ok	Pedro, Paulo, Sophie	1
		CDR – FM 30MHz	Ok	Ok	x			
		CDR – internal calibration	Ok	Ok	x	Ok		
CDR – external calibration		Ok	Ok	x	Ok			
FPGAs	GBT-FPGA on KC705	Tx	Ok	Ok	x	x	Manoel	3
		Rx	Ok	Ok	x	x		
	GBT-FPGA on Cyclone V	Tx	Tbd*	Tbd*	x	x		
		Rx	Tbd*	Tbd*	x	x		
	TTC-PON clock and data recovery with KC705	standard	Tbd*	Tbd*	x	x		
With internal VCXO		Tbd**	Tbd**	x	x			