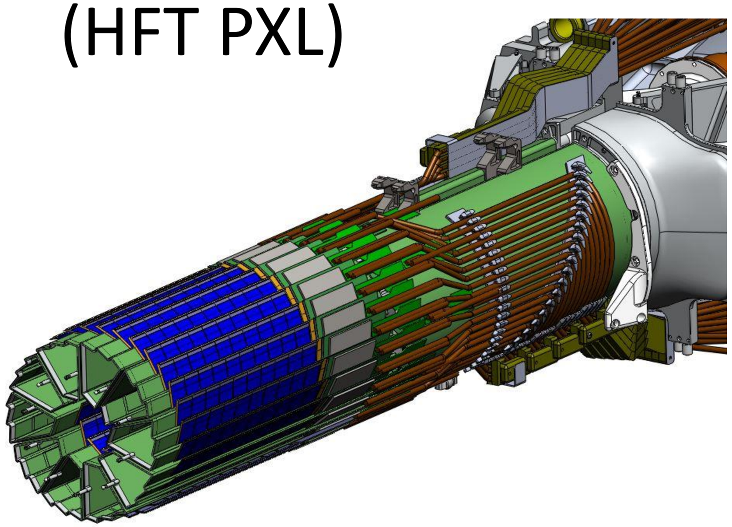
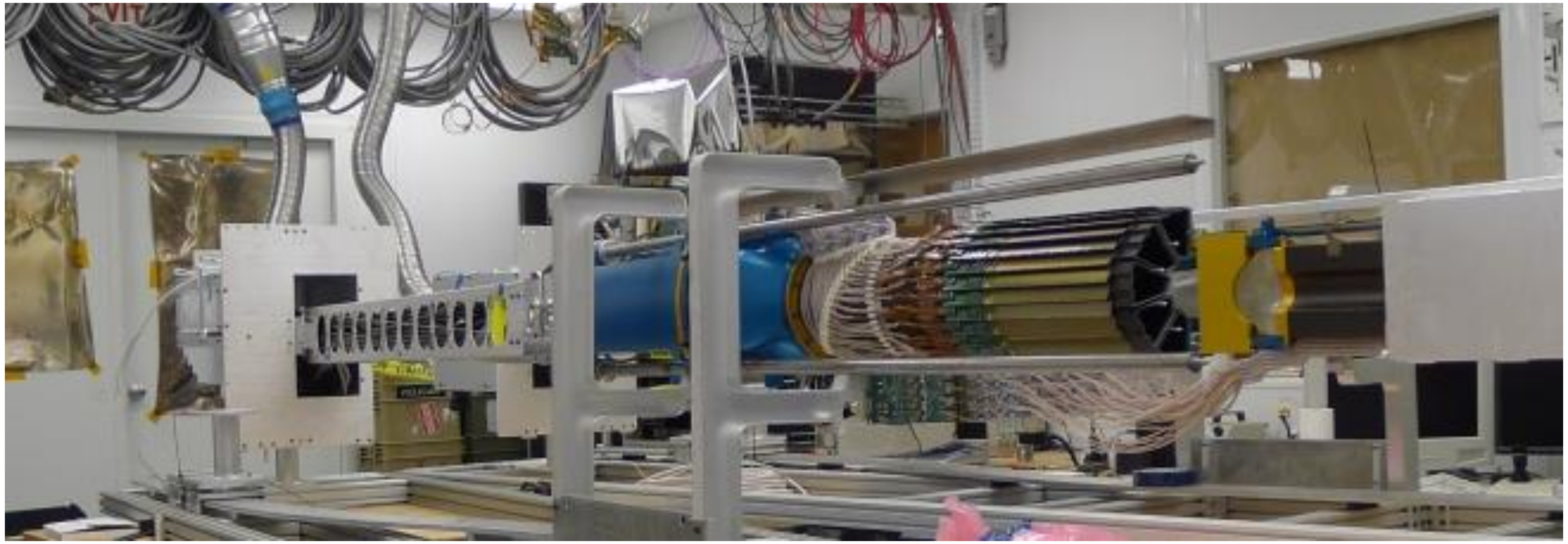
STAR HFT

Heavy Flavor Tracker Pixel Detector (HFT PXL)



Howard Wieman
LBNL
for HFT collaboration



First operational vertex detector based on Monolithic Active Pixel Sensors (MAPS) or also called CMOS Pixel Sensors (CPS)

CPS developed by PICSEL group of IPHC-Strasbourg (Marc Winter et al.)

Outline

- Introduction, description of HFT PXL and purpose
- Requirements and fit to MAPS technology
- Credit the IPHC group that developed the detector chip
- Briefly cover how the chip works
- What we can expect in detector chip development and how it can benefit STAR

HFT PXL in STAR Inner Detector Upgrades

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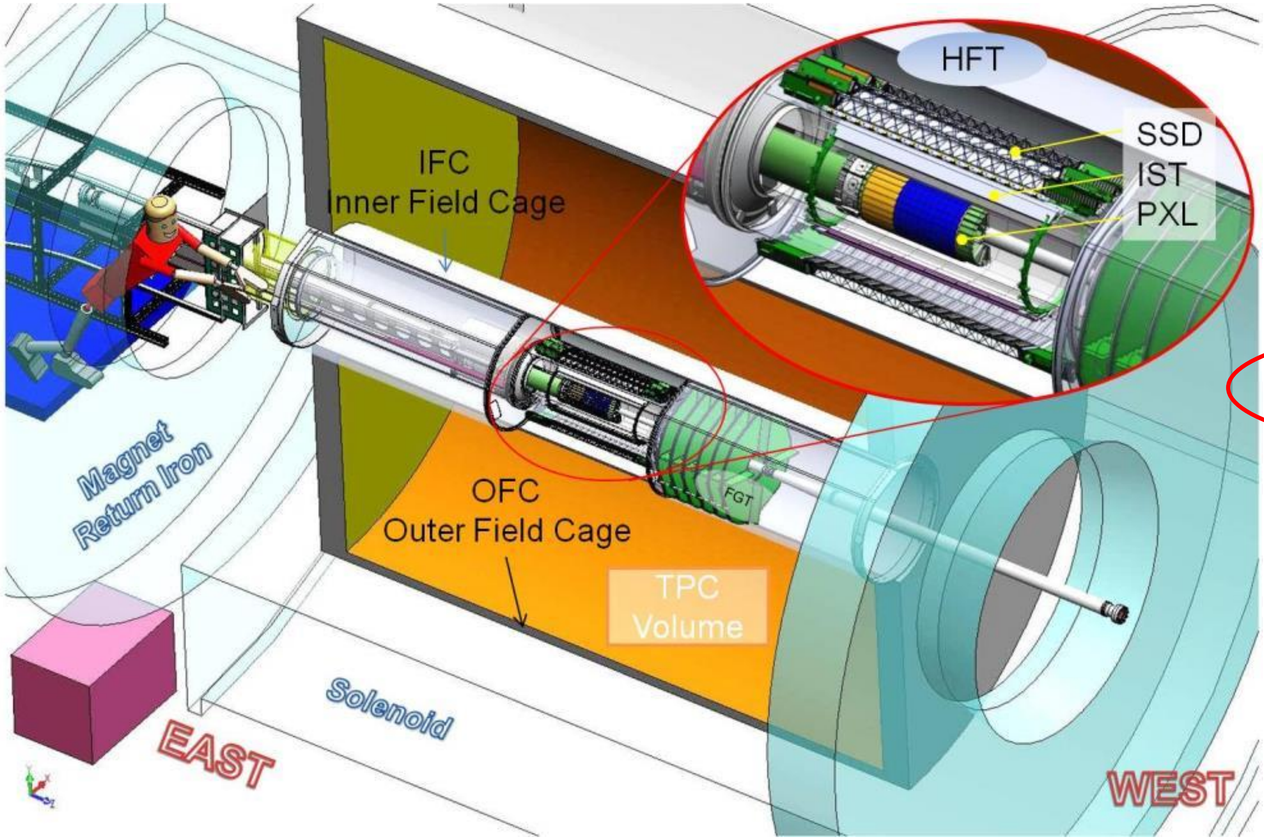
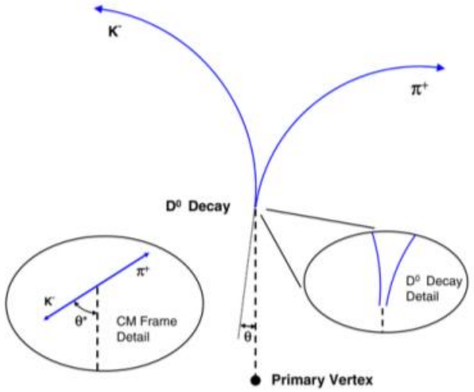


TPC – Time Projection Chamber (main tracking detector in STAR)

HFT – Heavy Flavor Tracker

- SSD – Silicon Strip Detector
    - r = 22 cm
- IST – Inner Silicon Tracker
    - r = 14 cm
- PXL – Pixel Detector
    - r = 2.8, 8 cm



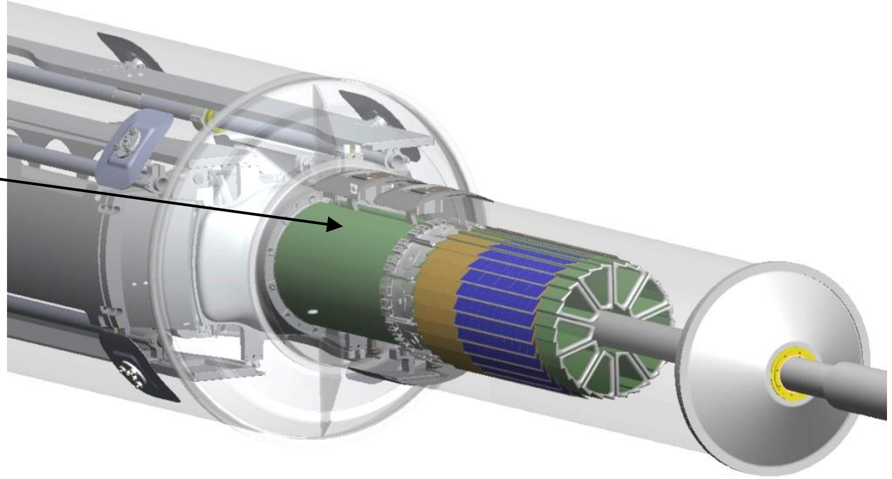
Direct topological reconstruction of Charm

We track inward from the TPC with graded resolution:

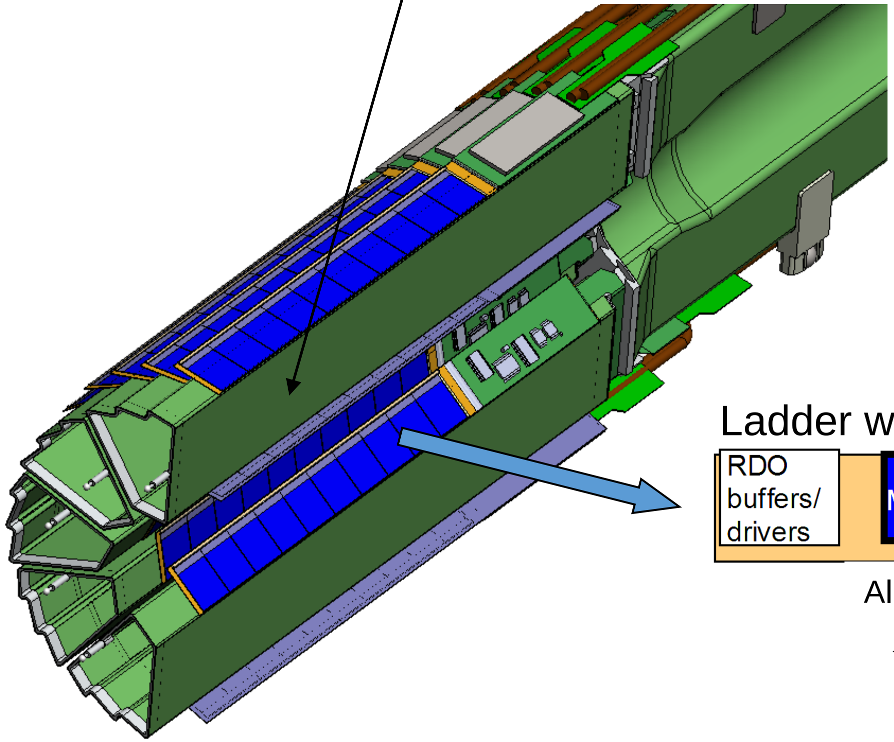
TPC → ~1mm → SSD → ~300µm → IST → ~250µm → PXL → <30µm → vertex

PXL Detector Design

Mechanical support with kinematic mounts (insertion side)

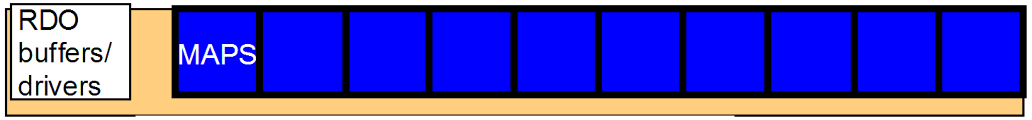


carbon fiber sector tubes (260 µm thick)



Insertion from one side
2 layers
5 sectors / half (10 sectors total)
4 ladders/sector
5 ladder weight 11.2 gm

Ladder with 10 MAPS sensors (approx. 2×2 cm each)



Aluminum conductor Ladder Flex Cable

← 20 cm →

PXL Detector Design Characteristics

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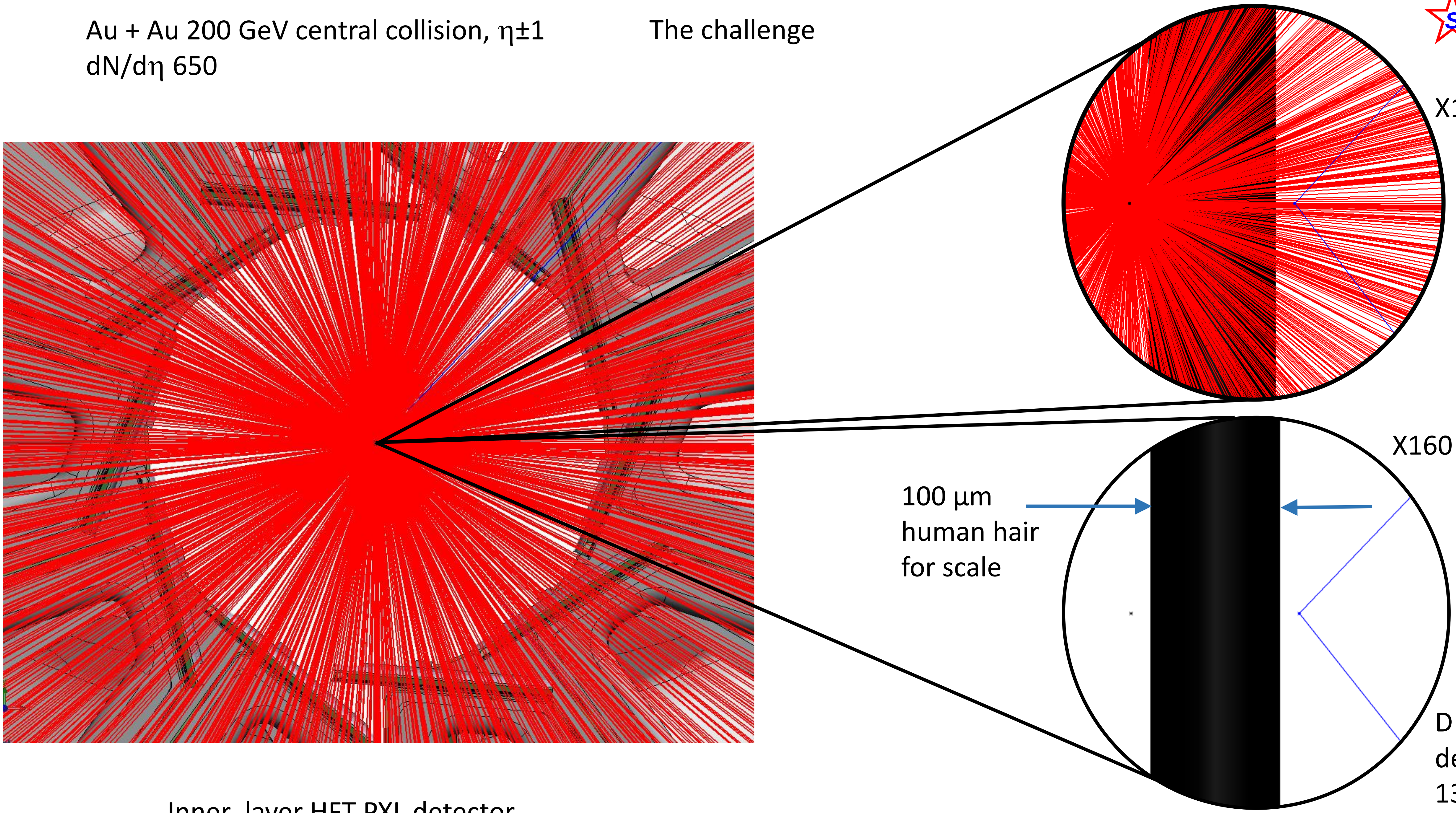
DCA Pointing resolution	$(12^* \oplus 24\ \mathrm{GeV}/p\cdot c)\ \mu m$
Layers	Layer 1 at 2.8 cm radius Layer 2 at 8 cm radius
Pixel size	20.7 μm X 20.7 μm
Hit resolution	3.7 μm (6 μm geometric)
Position stability	6 μm rms (20 μm envelope)
Radiation length first layer	X/X_0 = 0.39% (Al conductor cable)
Number of pixels	356 M
Integration time (affects pileup)	185.6 μs
Radiation environment	20 to 90 kRad / year $2{*}10^{11}$ to 10^{12} 1MeV n eq/cm^2
Rapid detector replacement	~ 1 day

356 M pixels on ~0.16 m^2 of Silicon

* Simple geometric component, cluster centriod fitting gives factor of ~1.7 better.

Au + Au 200 GeV central collision, $\eta \pm 1$
$dN/d\eta$ 650

The challenge



Inner layer HFT PXL detector

Requirement:
The detector should resolve vertex locations as precisely as possible.
Which means:

1. Thin, reduced multiple coulomb scattering
2. Small high position resolution pixels
3. Stable, limited vibration and low position drift
4. Inner layer close to the beam

Additional requirements:

5. Fast, to reduce pileup which compromises hit to track association
6. Radiation hard

MAPS are particularly well suited to satisfying item 1 because they can be thinned to 50 µm, they don’t need an additional silicon readout layer, and they are relatively low power and can therefore be cooled with air, avoiding more massive cooling systems.

MAPS satisfy item 2, they have smaller pixels than alternative technologies. This is more important than one might think and will be addressed in more detail in the next slide.

MAPS are limited in satisfying items 5 and 6, pileup and radiation hardness. This is where one can expect improvements in the future. Some of these expectations will be covered.

The advantage of improved spatial resolution and reduced radiation length

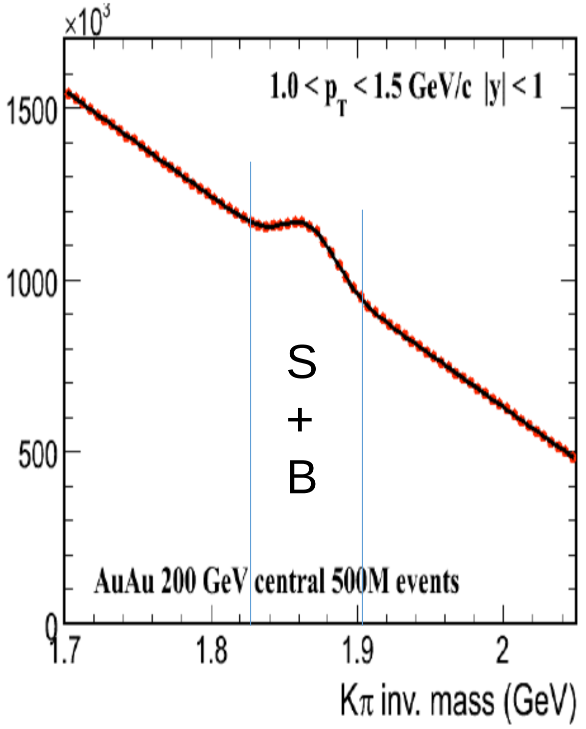
Compare simulated detector performance in number of events required to reach a given significance:

$$\frac{signal}{\sqrt{signal+background}}$$

Simulation results

	Pixel size	radiation length	0.5 GeV D_0 relative number of events	1.5 GeV D_0 relative number of events
hybrid	50 μm x 450 μm	1.4%	36	200
MAPS	27 μm x 27 μm	0.6%	1	1

parameters used in the simulation, but actual HFT PXL parameters are smaller



Marc Winter's IPHC MAPS Team in Strasbourg:

Design, testing, integration

2000: 3 FTE ➔ 2014: ~25-30 FTE

~ 20 Ph.D students involved in the development

Designed and developed the STAR PXL detector chip

from CPIX14 15-17 September 2014, University of Bonn, IPHC christine.hu@in2p3.fr

Institut Pluridisciplinaire Hubert Curien (IPHC)

Worked closely with LBNL with significant interaction with Leo Greiner and his team adjusting design to provide diagnostic and testing features.

Arranged for Michal Szelezniak to move to LBNL help with integration of MAPS in our project

Their graduating students have moved on and done well at other detector design centers:

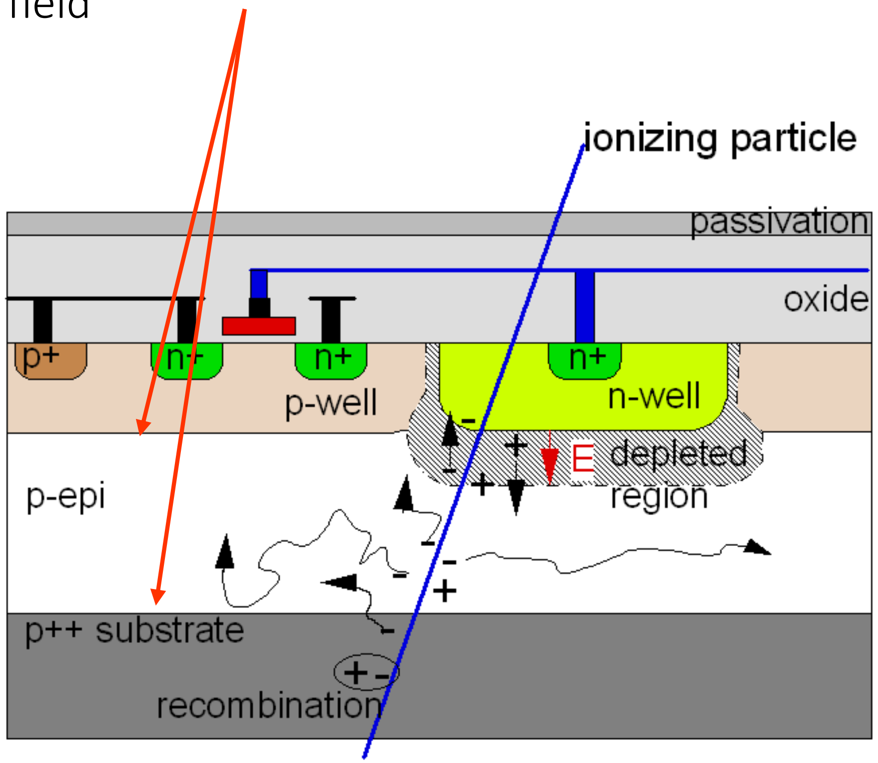
Grzegorz Deptuch, group leader at Fermi Lab

Renato Turchetta, group leader at Rutherford Appleton Lab

Some features of the CPS in HFT PXL

STAR HFT

charge reflection where p doping changes generating an E field

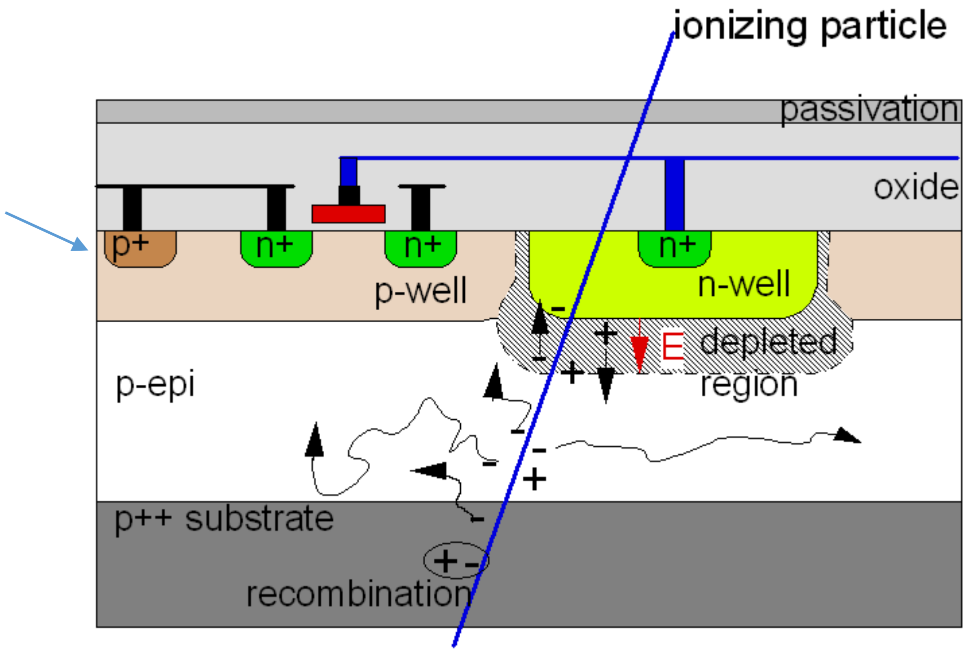


basic sensing diode in traditional CPS

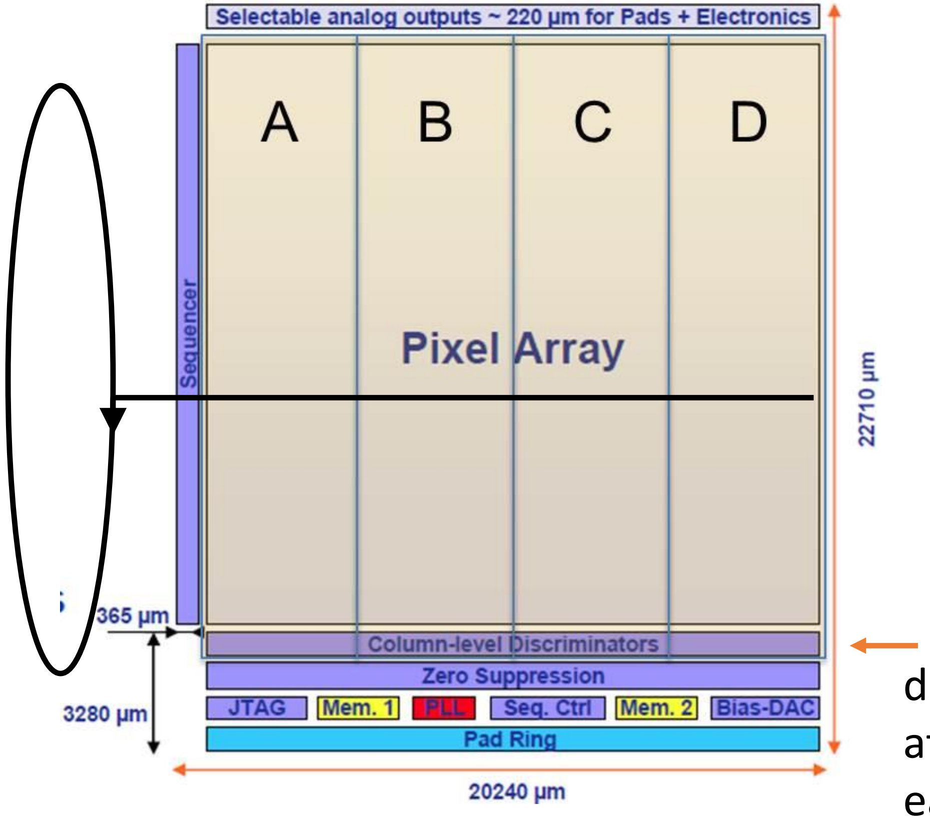
- Ion ionizing radiation generates electron hole pairs
- Electrons in the depleted region drift (rapid transfer to the n well)
- Electrons in the non depleted p-epi feel no field and randomly diffuse (a slow process) before the reach a depleted region and are captured
- On the detection time scale the diode is electrically isolated so that the voltage on the diode is a step function with $\Delta V = \Delta Q/C$. This voltage change is recorded through Correlated Double Sampling (CDS)

Some features of the CPS in HFT PXL

The PXL chip has an amplifier and CDS built into each PXL. This allows a single discriminator be used to successively to record hits for multiple pixels.



Some added comments while this picture is up:
Over the development time of the PXL detector, improvements in the CMOS available to IPHC lead to important improvements. The available p-epi layer went from 10 Ω cm to 400 Ω cm, that is the p-epi is less heavily doped and consequently the depletion region thickens. This improves the signal to noise because C is smaller resulting in better signal to noise (remember $\Delta V = \Delta Q/C$). This and the reduced charge collection time improves radiation hardness. Reducing the charge collection time means less probability for electrons to be trapped on the radiation induced defects. Slow electrons in the diffusion region are more likely to be trapped than the fast electrons in the depleted drift region.



discriminator at the end of each column

Rolling shutter readout

- A row is selected, and each pixel in the row is connected to it's column
- Once the column line has settled the discriminator at the end of the column identifies whether the pixel contained a hit and then the row counter advances to the next row to repeat
- A hit is recorded for any particle that passes between interrogations, so cycling faster reduces pileup

readout time of STAR PXL chip: 186 μs

Rows: 928
Columns: 960

With this scheme the frame time or readout frequency is limited by the power vs time trade off of charging the long column lines connecting the pixel to the discriminator. It is for this reason that many groups are working on methods to include the discriminator within the pixel. Having a discriminator in each pixel can lead to a significant reduction in the readout time, more on this later.

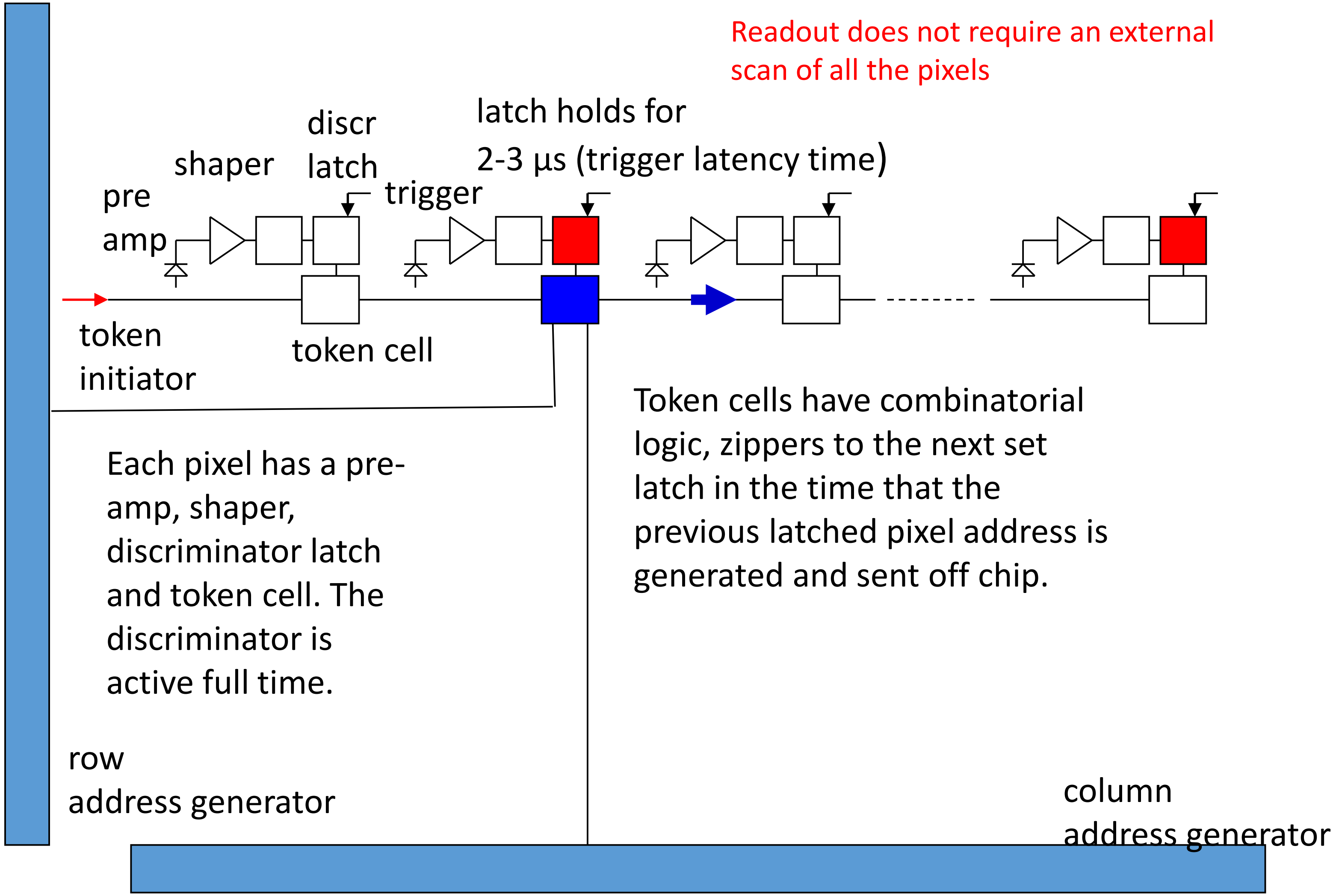
The current version of the HFT PXL detector is cutting edge and will allow for the first time topological reconstruction of Ds in a heavy ion environment.

But, there is room for improvement. A much shorter read out time would be big for the following two reasons.

- Reduced pileup to improve hit to track association and allow operation at higher luminosities
- Allow use of PXL data in the trigger definition

Next, what we can expect from improved technology

One example, a faster readout based on the token approach.



tokens, a concept used in hybrid technology, FPIX, 1999, Fermi Lab

- If a pixel is hit the latch remains on for a few μs
- If a trigger arrives during that time then the latch is held active
- The token stops at the next active pixel and the pixel connects to the address generators. Since this is a logic connection settling time is short compared to an analogue connection. Plus only hit pixels get connected to the perimeter. This is the big time saver over the current HFT PXL chip.
- The token is released and ripples through to next active pixel. The pixel to pixel ripple through is very fast since it is local logic not requiring a clock.

The main point of the last slide was to show that with a discriminator on each pixel there are ways to read out a chip without interrogating each pixel from the perimeter of the chip and that greatly speeds up the readout of the chip.

Walter Snoeys and Luciano Musa at CERN are developing the ALPIDE chip which has an amplifier and discriminator on each pixel and also uses asynchronous (combinatorial) readout logic. It accomplishes the same thing as the token approach, namely only hit pixels get clocked out to the periphery.

See:

Marc Winter's talk: "CMOS Pixel Sensors Developed for the ALICE-ITS Upgrade" Workshop on CMOS Active Pixel Sensors for Particle Tracking (CPIX14) 15-17 September 2014, University of Bonn
http://indico.cern.ch/event/309449/session/20/contribution/9/material/slides/

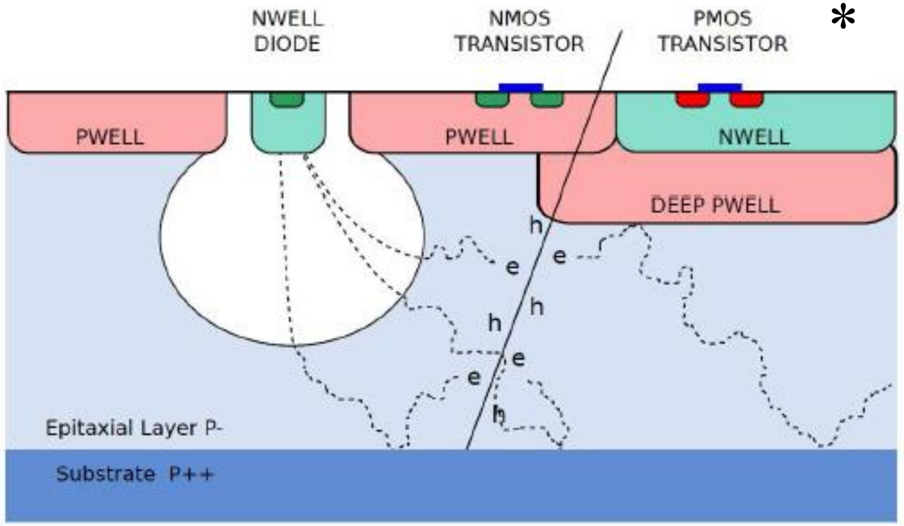
also:
The ALICE Collaboration, J. Phys. G: Nucl. Part. Phys. 41 (2014) 087002, 2.5.4 ALPIDE, p. 22

Requirements for an on pixel discriminator

- Need more signal for operation with a simple on pixel discriminator. This is required to overcome variations in discriminator thresholds.

Two options being studied

1. Deep p-well so that both p channel and n channel FETs can be placed in the pixel. Better amplifies that can provide a larger signal require both p and n channel FETs. With traditional CMOS technology only n channel FETs can be used.
2. 3D technology where the amplifiers and other electronics are in one layer and the sensor silicon is a separate layer directly bonded and coupled to the electronics layer. This is in the same spirit as earlier hybrid pixel designs, but the coupling technology provides higher pixel densities than can be achieved with traditional bump bonding. By having a separate sensor silicon one can use a thicker high resistive silicon and full depletion to produce a larger signal. Also, both NMOS and PMOS is available for the Read Out Integrated Circuit (ROIC).



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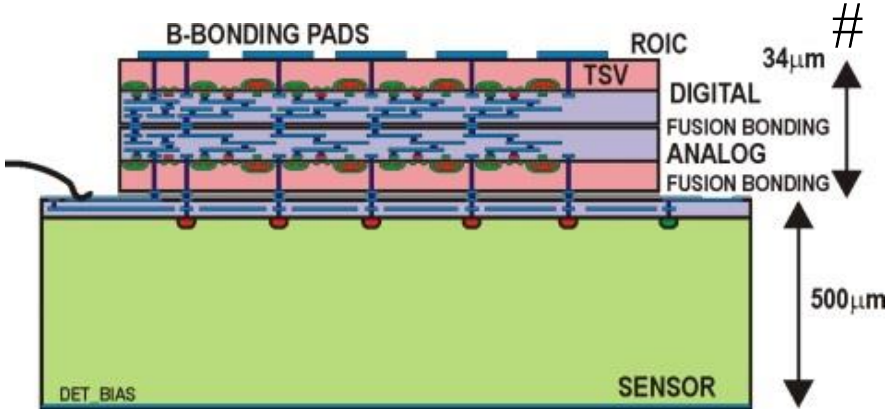
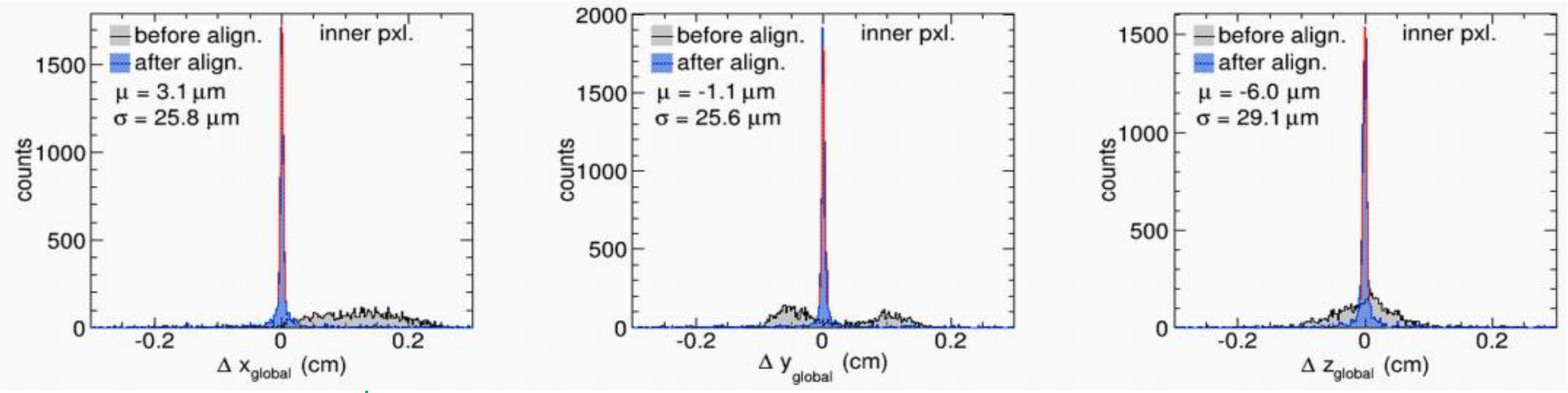
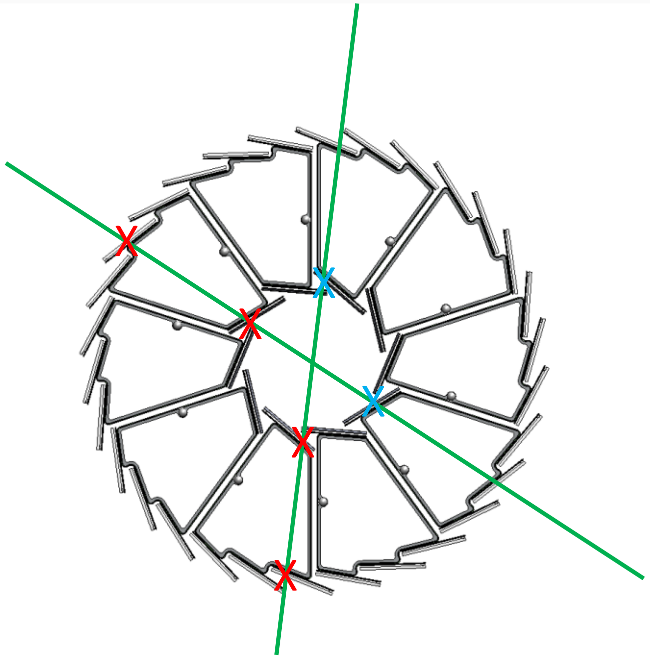


∗ Fig. from Marc Winter's talk: "CMOS Pixel Sensors Developed for the ALICE-ITS Upgrade" Workshop on CMOS Active Pixel Sensors for Particle Tracking (CPIX14) 15-17 September 2014, University of Bonn

Fig. from Grzegorz Deptuch's talk: "MAPS are for amateurs, professionals do 3D" Workshop on CMOS Active Pixel Sensors for Particle Tracking (CPIX14) 15-17 September 2014, University of Bonn

In conclusion the HFT PXL detector installed in STAR is providing excellent pointing resolution





Cosmic ray result
Excellent half to half pointing, sub 30 μm
But after half to half alignment which was required to correct poor reproducibility of kinematic mount seating

Xs shows how hits are selected for projective distance of closest approach comparison

AND

We are well positioned with our quick change mechanics to take advantage of expected new pixel technologies that will both allow operation at increased luminosities and use of pixel information in trigger decisions.

backup

Deptuch chip: 400 mW or 100 mW/cm^2

ALPIDE: 50 nW/pixel or 48 mW for 980^2 pixels

Reduce pileup and improve hit to track association

Roughly where we are now with the HFT PXL at current luminosity

$\sigma = 120\mu m$ combined position uncertainty between a track and a hit on the inner layer

$\rho = 65 \cdot cm^{-2}$ hit density on the inner layer, scales with luminosity and integration time

$$P = \frac{1}{2 \cdot \pi \cdot \sigma^2 \cdot \rho + 1} = 94 \cdot \%$$ probability of correctly associating the hit with the track

Pileup hit density will be increasing with luminosity further compromising the ability to correctly associate hits with tracks.
The solution is reduced readout time/integration time for accumulating pileup hits.