Preliminary results with capacitively coupled pixel detectors for CLIC

Daniel Hynds
(on behalf of many people)

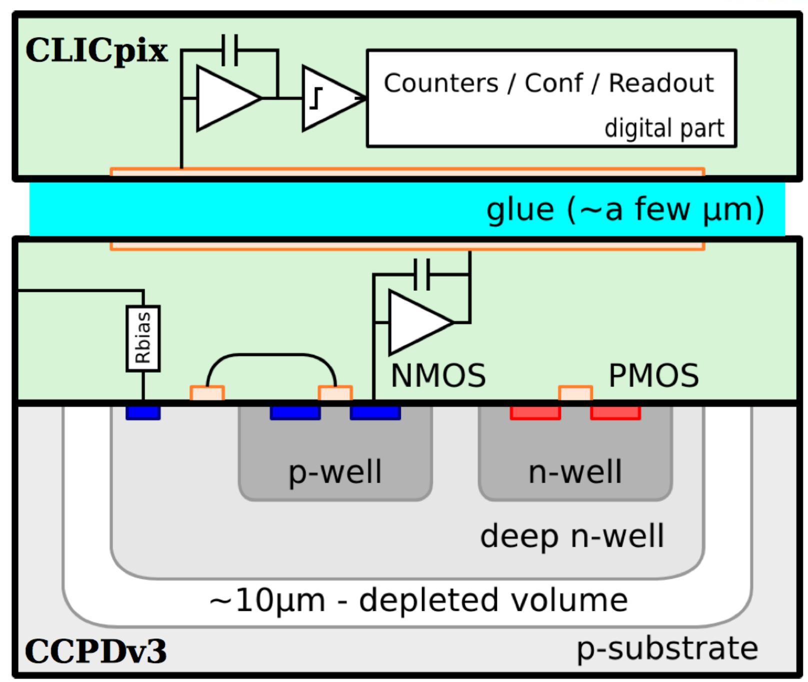
Capacitively coupled hybrid pixel detectors

- Baseline technology for CLIC vertex detector assumed to by hybrid pixel detectors. Requirements are tight:
  - Minimal power consumption, high spatial precision, fast timestamping, infinitely thin…
  - R&D directed toward small pitch hybrid pixel detector (CLICpix demonstrator in 65 nm) bump-bonded to thin sensor - ultimately 50 μm sensor on 50 μm thinned ASIC

- Emerging technology in particle physics: high voltage/high resistivity CMOS
  - Aim to replace passive diode sensors with "smart" sensors containing signal amplification
  - Use capacitive coupling instead of bump bonding

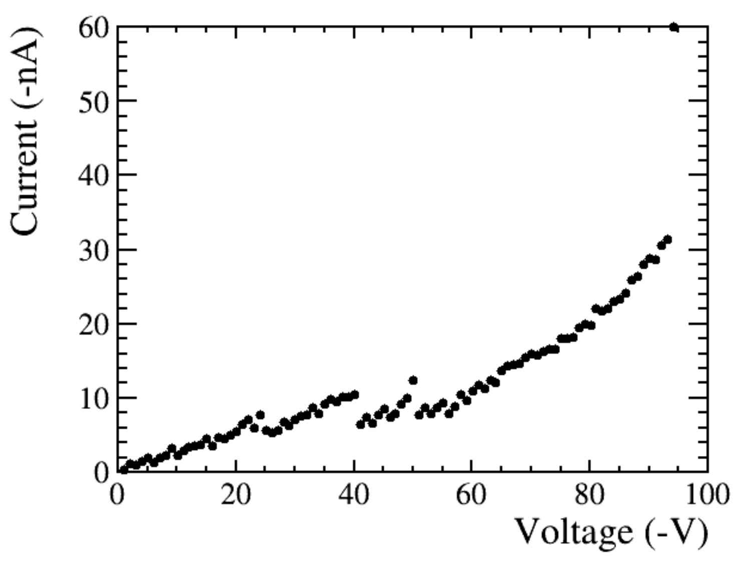
- Industry-standard process
  - Use deep n-well to shield electronics and allow application of a (mild) bias voltage to the substrate => fast drift signal from depleted region

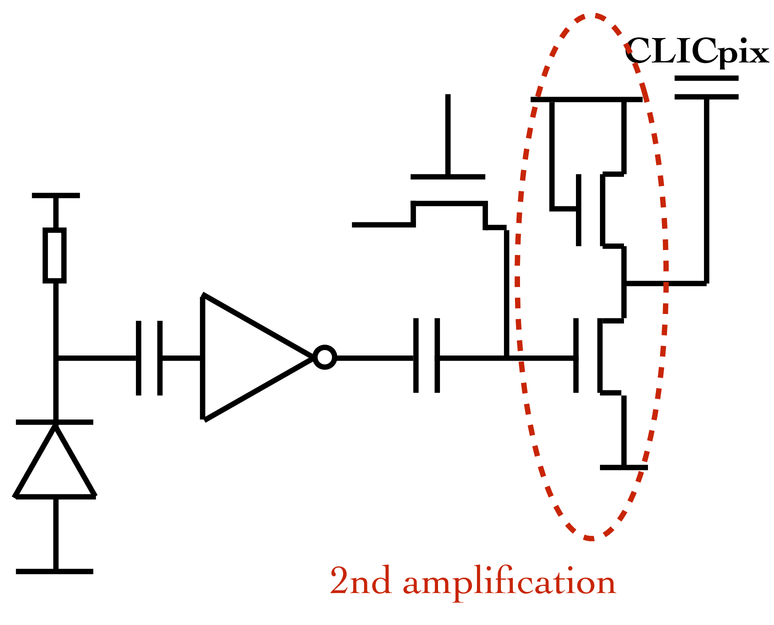
- Prototype assemblies under investigation for CLIC



HV-CMOS, the CCPDv3 chip

- CCPD (Capacitively Coupled Pixel Detector) version 3 designed by I. Perić
  - Fabrication in 180 nm AMS technology (deep n-well shielding, ~60 V rated, ~90 V tolerant)
  - 25 µm square pixels, 64 × 64 matrix designed to fit the CLICpix prototype readout ASIC
  - 4 columns contain a single amplification stage (positive signal), while 60 columns contain two-stage amplification (negative signal)
  - Relatively simple pixel architecture, limited standalone readout capabilities (analogue output possible from ~few pixels for debugging)

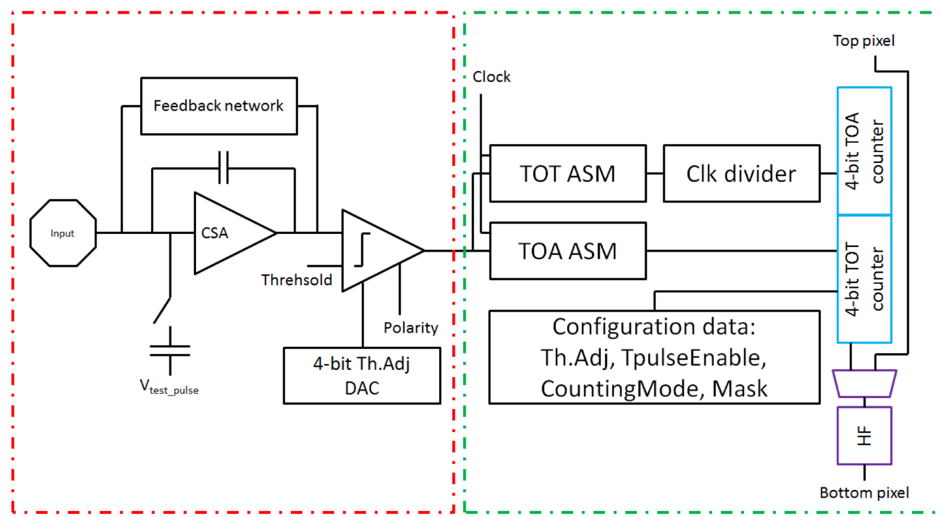




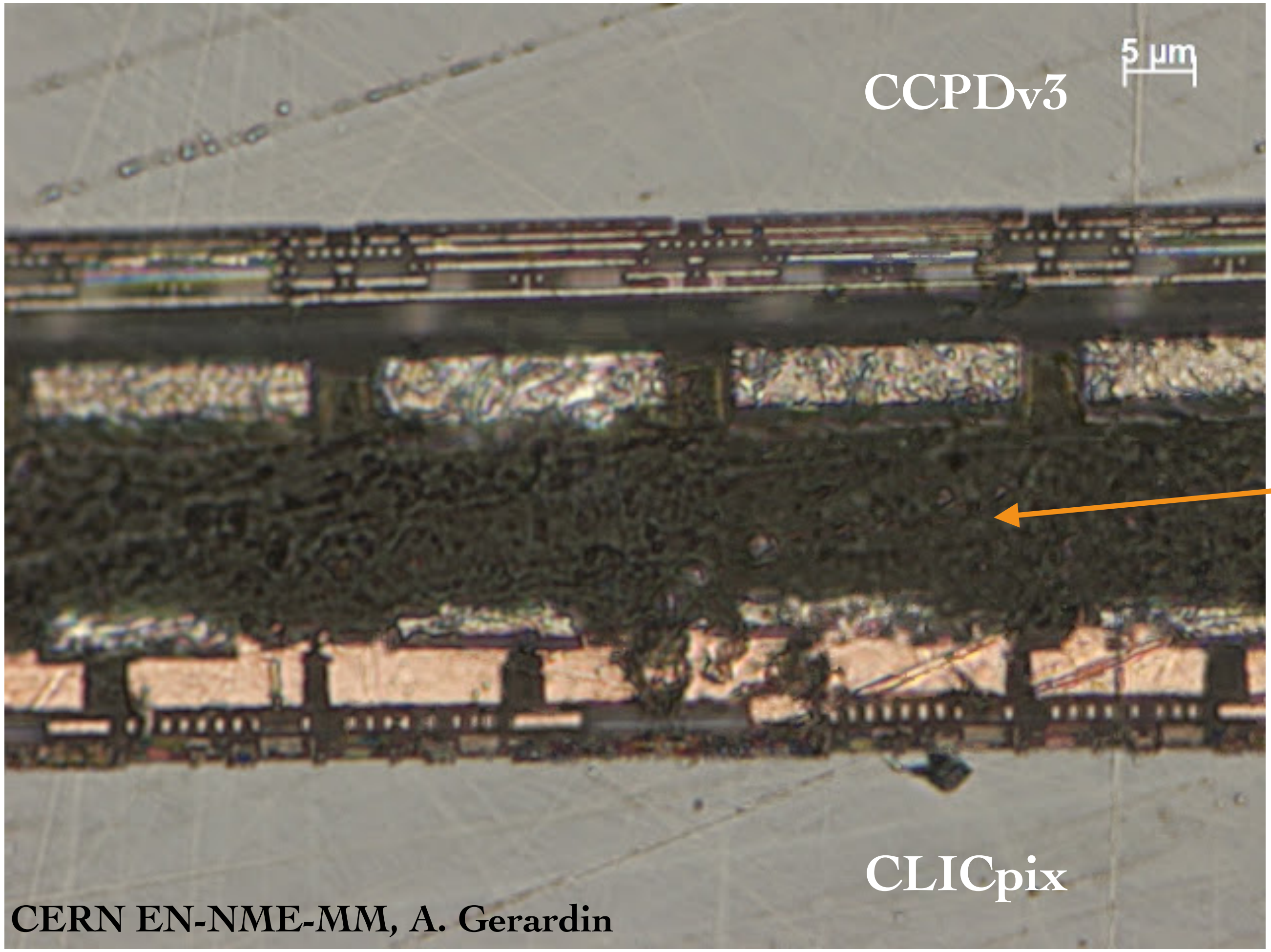
CLICpix

- CLICpix is the prototype readout ASIC designed to fit CLIC vertex detector specifications
  - Manufactured in 65 nm CMOS with small pixel size (25 µm × 25 µm) and containing a matrix of 64 × 64 pixels
  - Two 4-bit counters on each pixel for simultaneous ToT and ToA (or ToT and counting…)
  - Shutter-based data acquisition but with optional on-chip data compression
  - Power pulsing of the pixel matrix

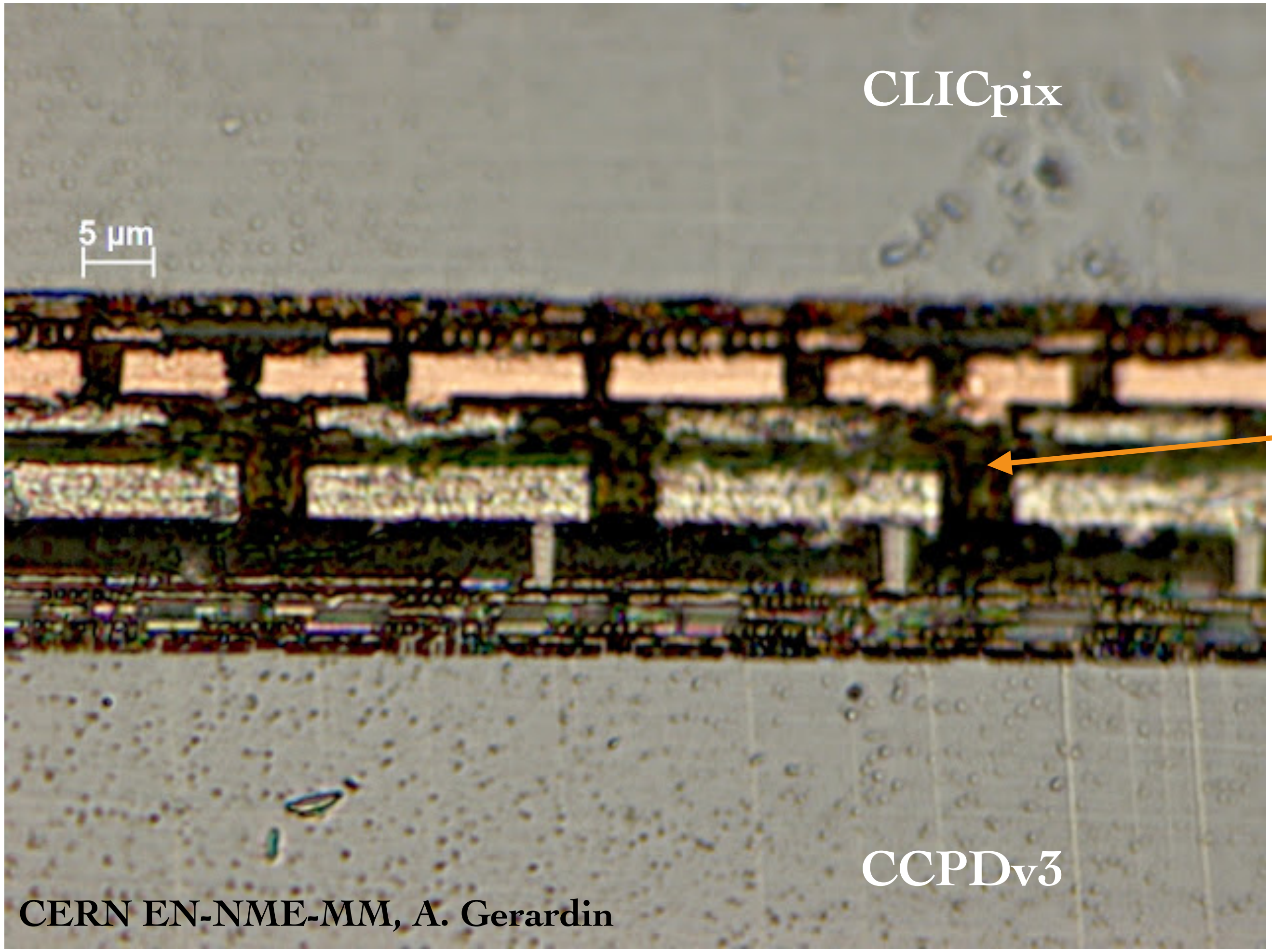
- Known issues:
  - Small overlap of discriminator signal line with CSA input pad => negative pulse injected into the front end when the discriminator starts firing
  - Will add signal to negative pulses, subtract signal for positive pulses



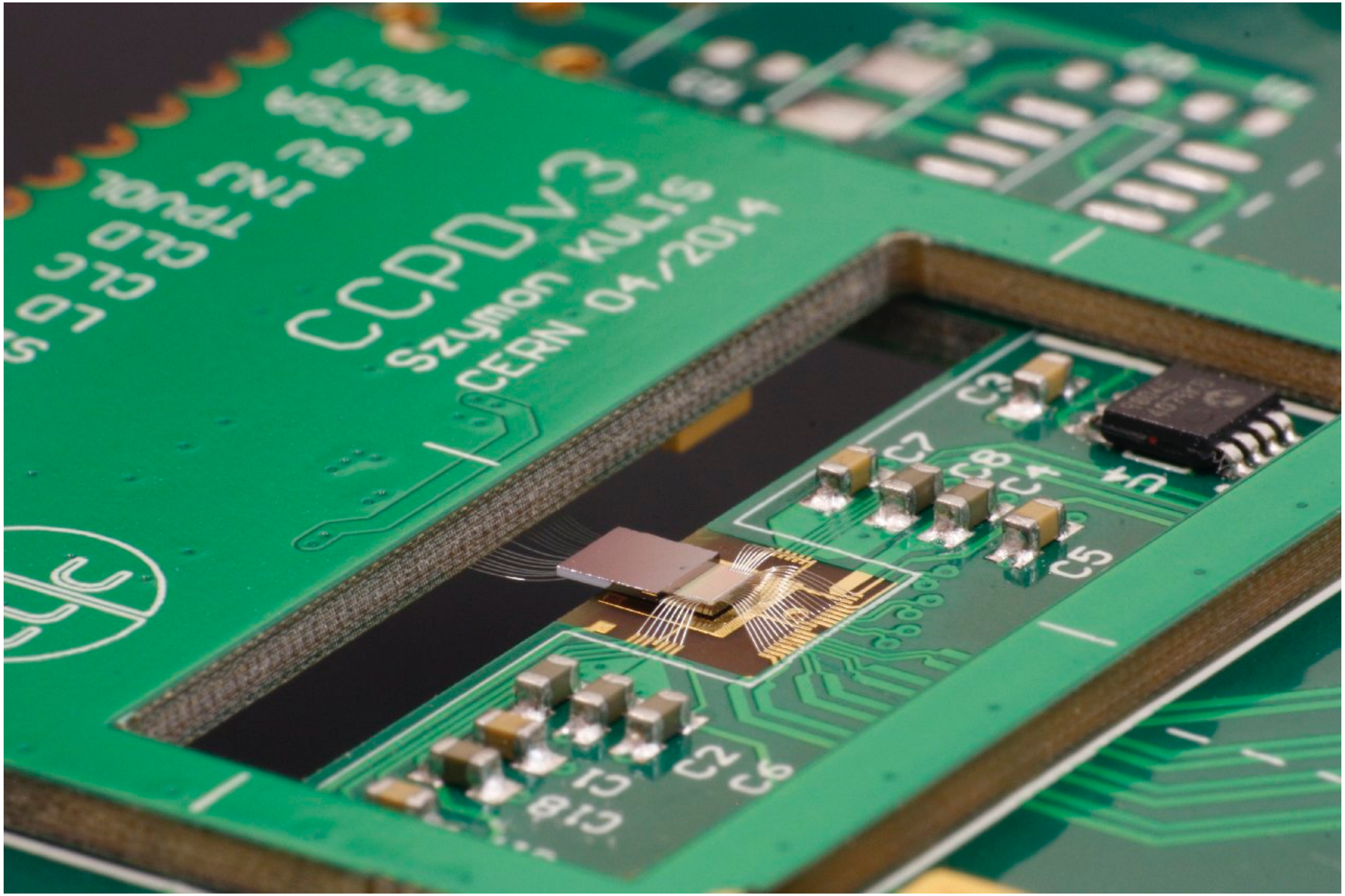
Assembly



Assembly

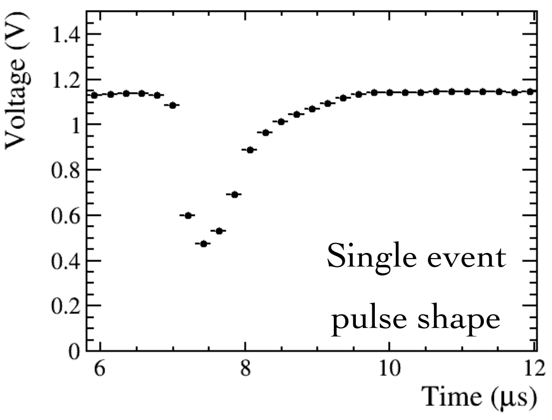


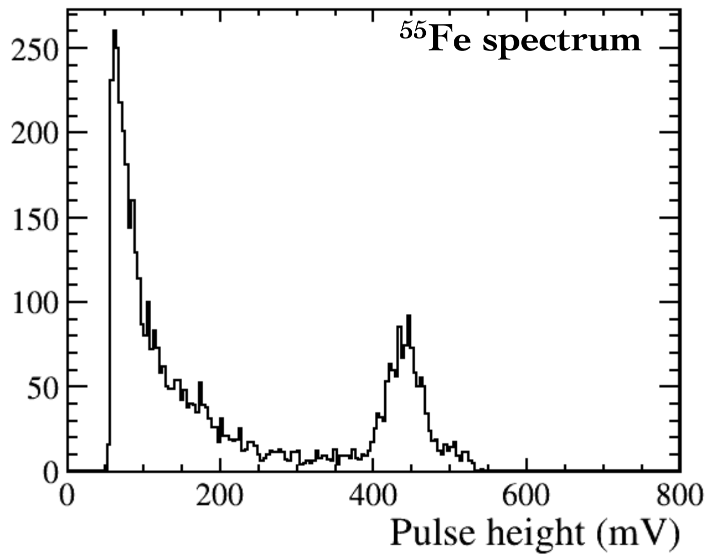
Lab measurements

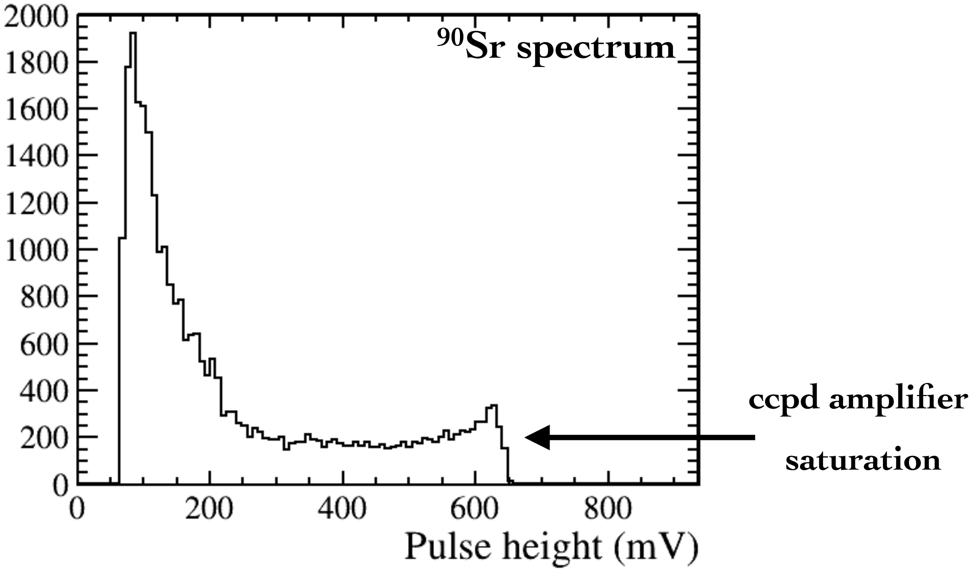


Charge spectra with HV-CMOS

- Lab tests performed on the HV-CMOS using single pixel analogue output to investigate signal shape and charge spectra with sources
  - Front-impinging ^{55}Fe on bare HV-CMOS assembly (~6 keV)
  - Back-impinging ^{90}Sr on full HV-CMOS + CLICpix assembly
  - (results shown for 2-stage amplifier design)



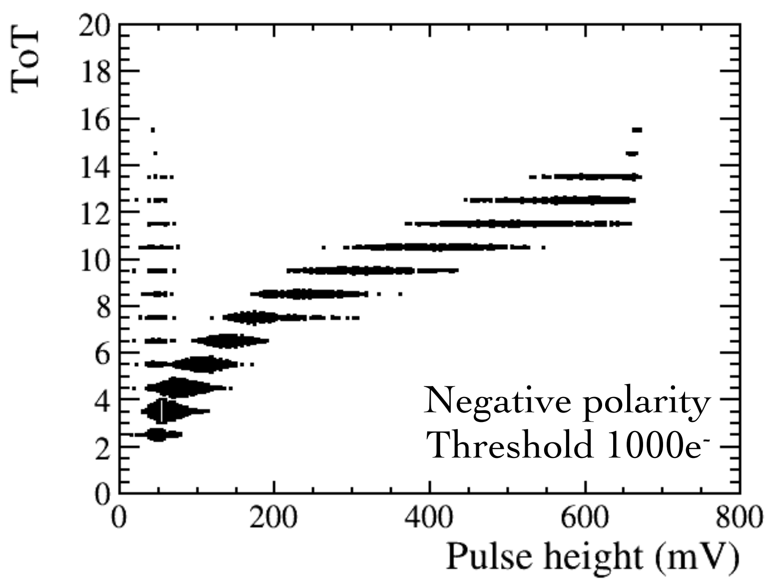


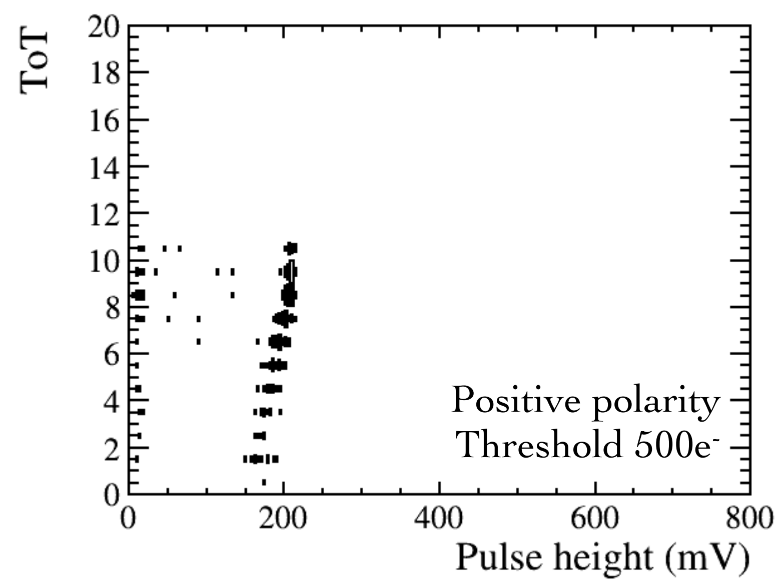


Induced signal in CLICpix

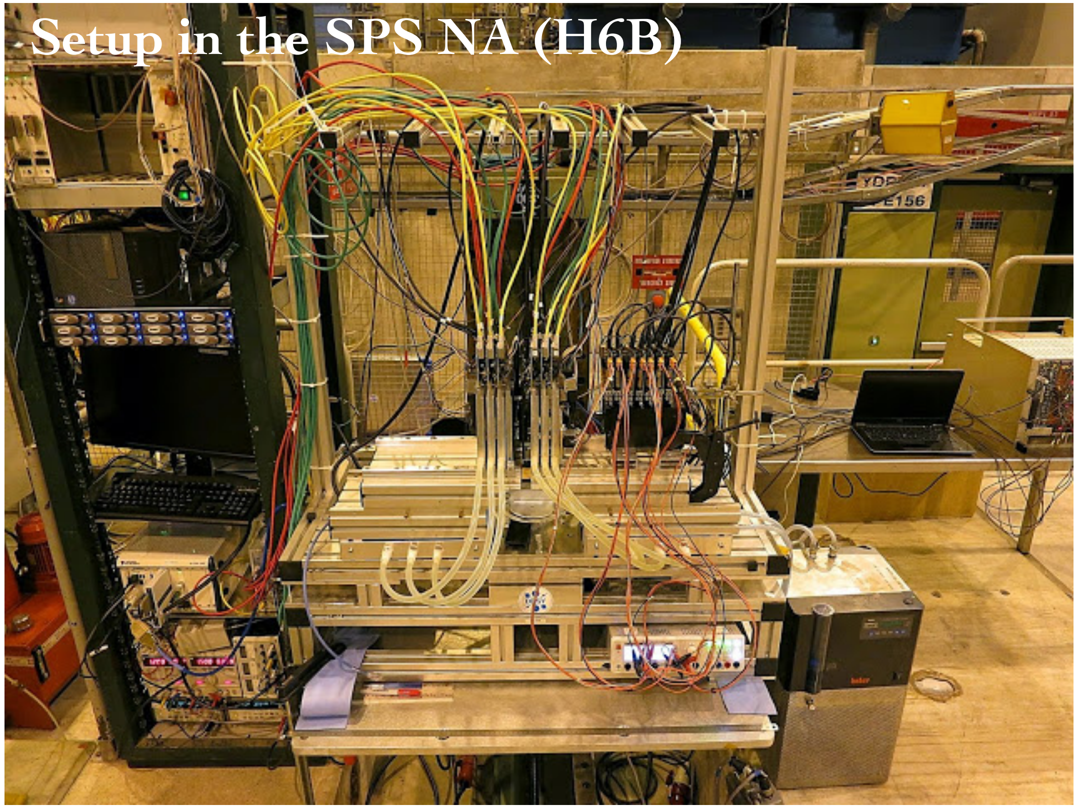
- Analogue output from several pixels on the HV-CMOS device can be monitored individually
  - Can take data in parallel with the CLICpix, correlate the pulse shape with the ToT
  - Open shutter, wait for signal on scope, close shutter and read out before subsequent hits

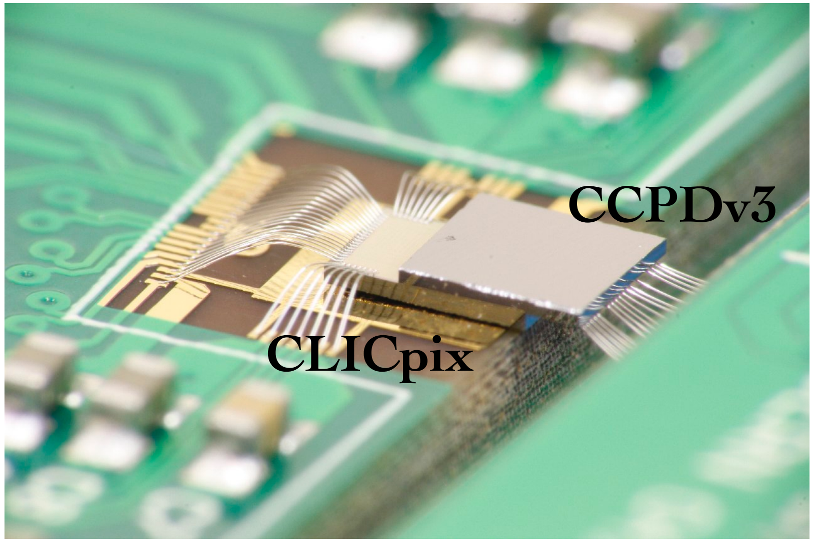
- Can see the difference between polarities
  - Injected negative charge gives a lower effective threshold when operating with negative polarity, higher effective threshold when operating with positive
  - Using nominal values of threshold this gives roughly 625 e^- injected charge



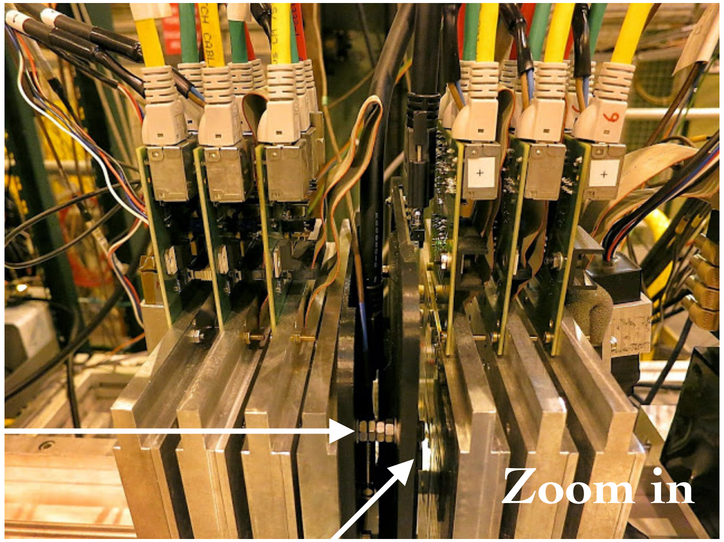


Beam data





Timepix3

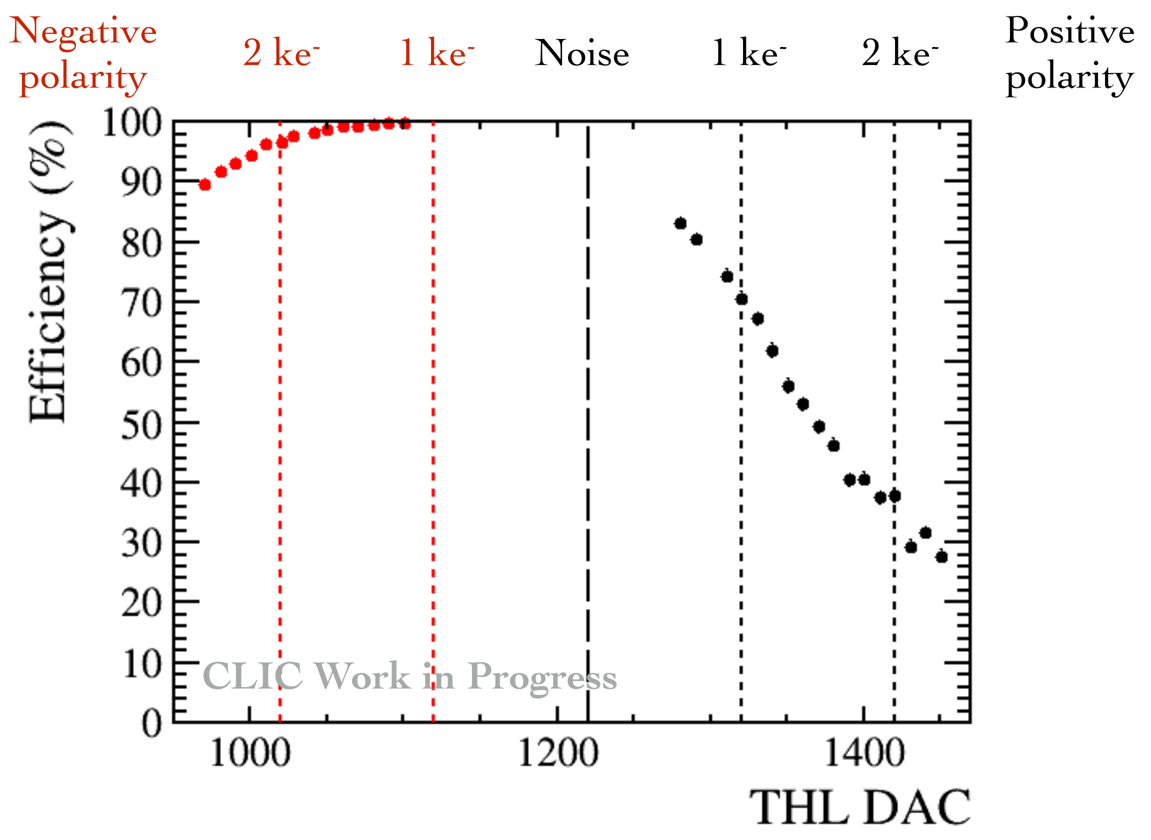


CLICpix

Threshold scan

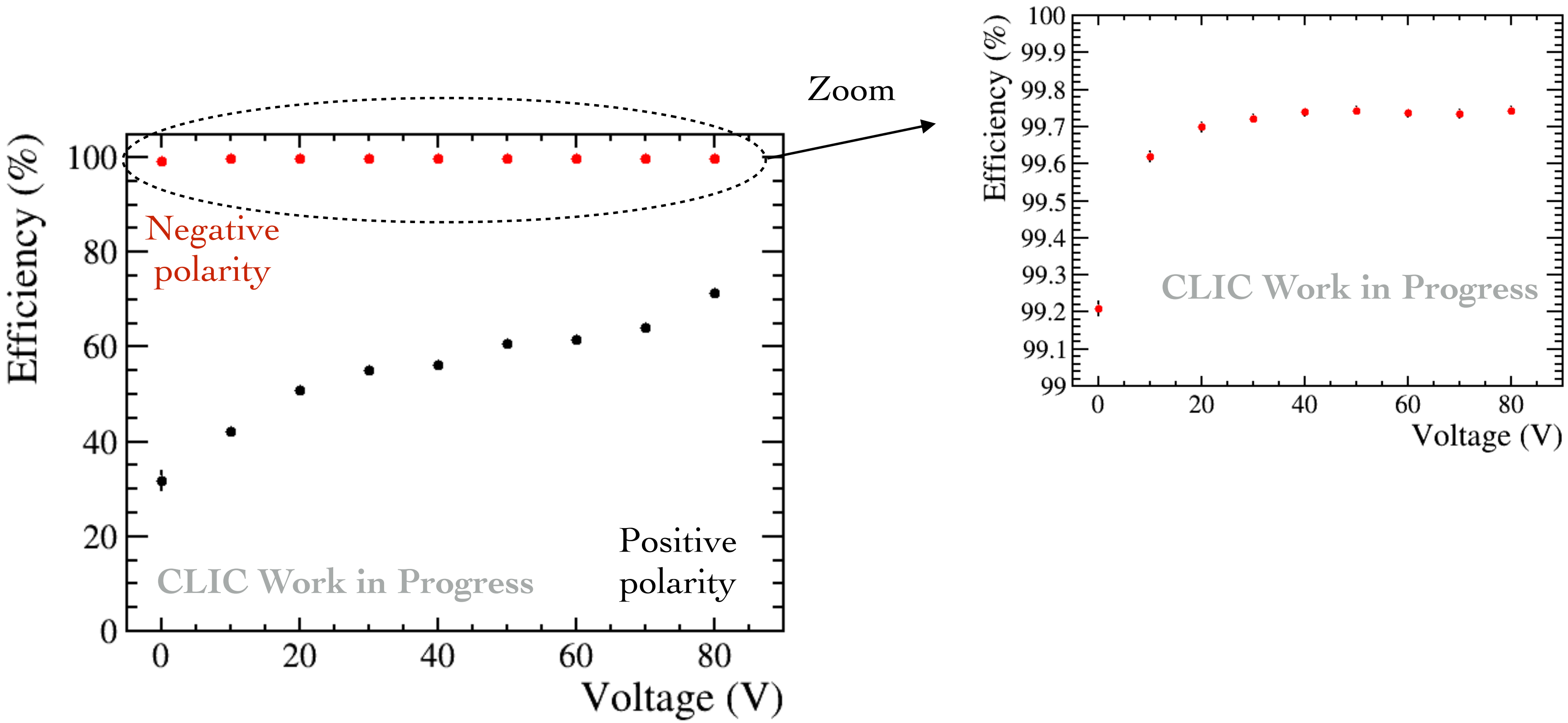
- Efficiency versus threshold for both polarities measured (60 V)
  - Pointing resolution from the telescope estimated < 2 μm

- Clear difference in performance
  - Able to reach high efficiency in negative polarity mode (2-stage amplification) with threshold ~ 1100 e^-
  - Single amplification stage pixels suffer from lower signal **and** subtraction of charge, but given fall off in 2-stage pixels it seems likely that with a new chip 500 e^- threshold will require 2nd stage



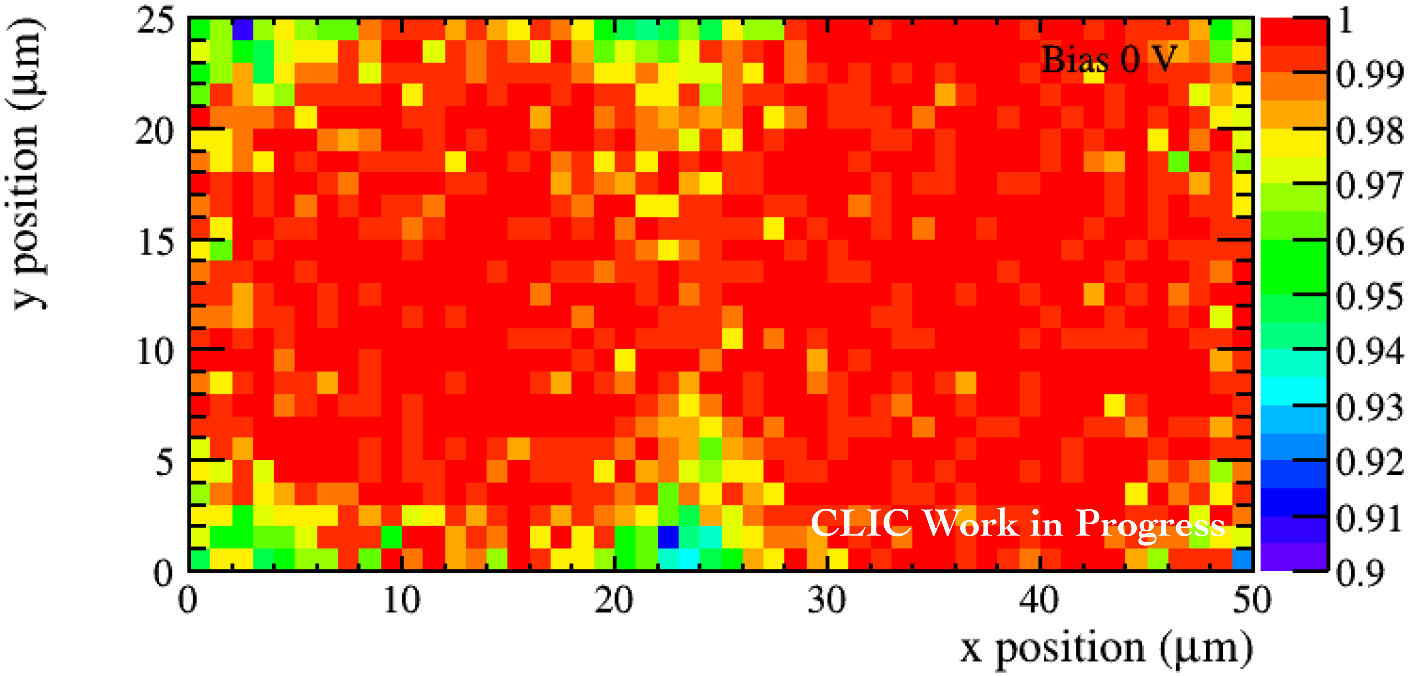
Bias scan

- High efficiency observed in negative polarity mode without bias on the HV-CMOS
  - Large component of collected charge from diffusion? Or large built-in depletion layer?
  - Estimates for depleted region vary, but typically ~10 μm at 60 V



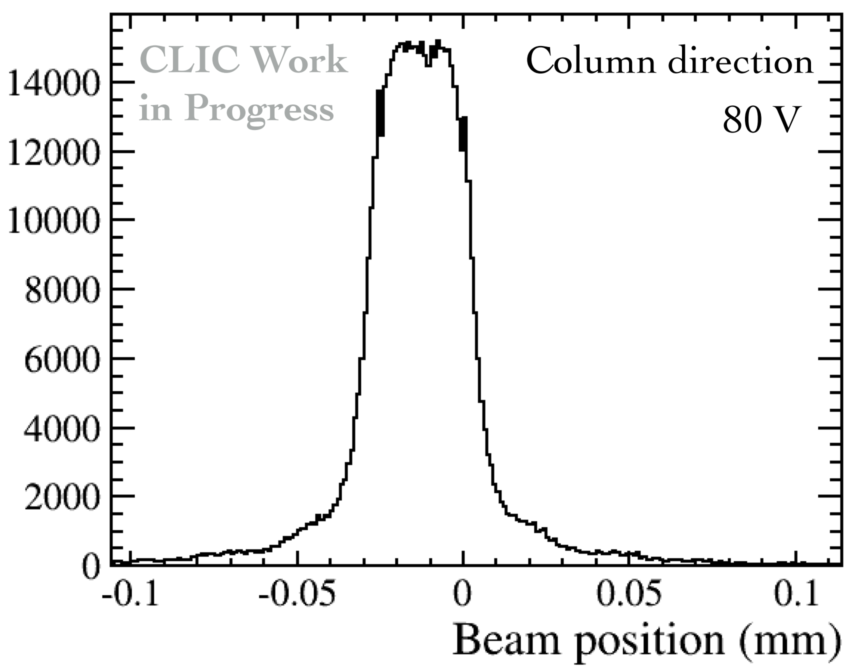
Bias scan - negative polarity

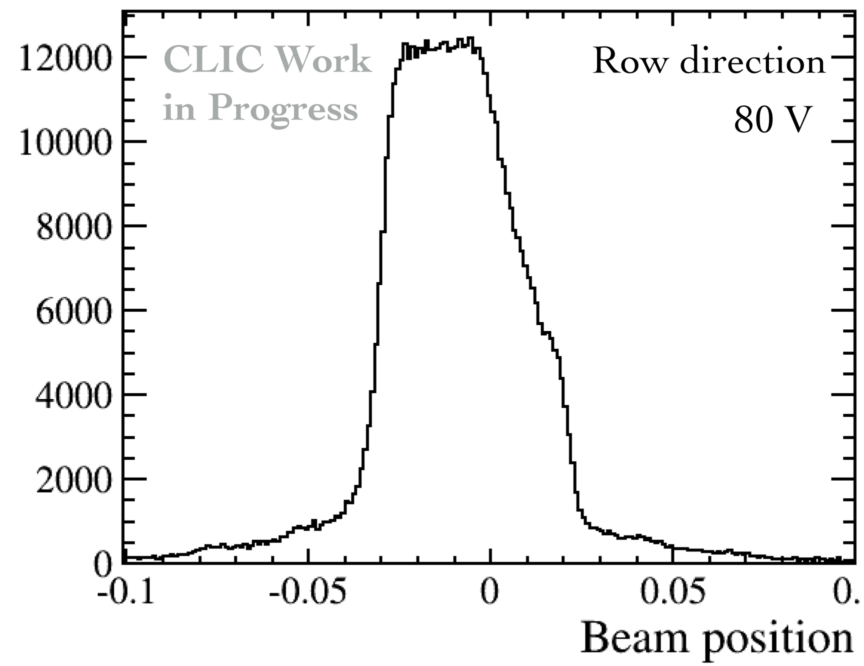
- Can map the variation in efficiency across the 2-pixel unit (charge injection differs between odd and even columns due to layout of signal routing)
  - Efficiency loss in the pixel corners for no applied bias (low threshold)
  - Clear difference between columns



Pixel cross-coupling

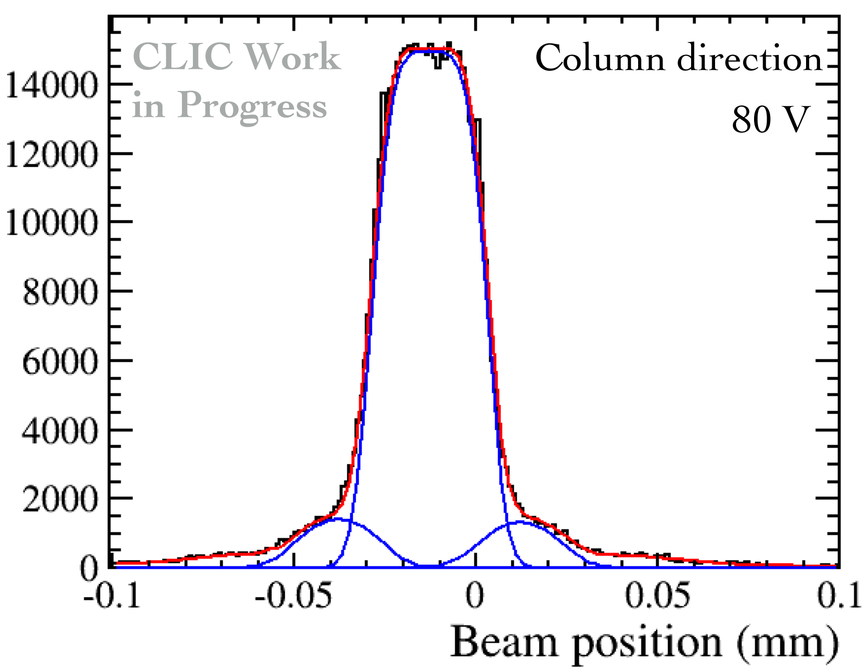
- Signal transfer between CCPDv3 and CLICpix via capacitive coupling - might have some cross-coupling between pixels on the same/different device(s)?
  - Scan the beam across the matrix and observe the behaviour of all pixels
  - Look at when pixel starts responding, and when it stops
  - Ideal function should be top hat function with width described by the lateral charge diffusion

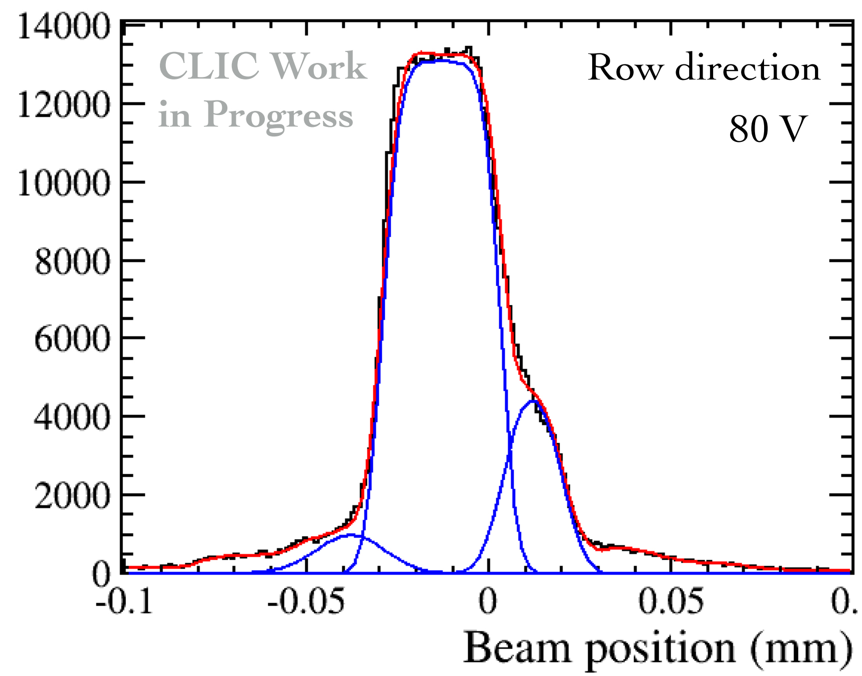




Pixel cross-coupling

- Different response in row and column directions
  - In each case can fit for the contribution from each pixel - clear signal from coupling to neighbours
  - In the row direction there is a large contribution from the pixel immediately to the right => strongly suggests misalignment in the row direction
  - Glueing studies planned to evaluate precision of the flip-chip machine





Summary and plans

- Promising early results from capacitively coupled assemblies
  - Simple pixel layout with 2-stage analogue amplification shows high (>99%) efficiency
  - High efficiency without applied bias voltage, 30 - 40 V required to reduce inefficiencies between pixels
  - **Paper** in preparation (pre-draft going through first comments)

- Fabrication steps
  - Larger (and injection-free) version of CLICpix under development
  - New HV-CMOS devices planned on higher resistivity substrate (increased drift region) - possible digital version(s) in addition to straightforward 2-stage amplifier

- Future studies
  - Measurements of coupling capacitance (and cross-capacitance) due to gluing
  - Beam measurements to evaluate power-pulsing of the front end and timewalk of the assembly
  - Active depth measurements to determine drift region and contribution of diffusion

BACKUP

Beam data - overview

- Full matrix appears responsive (negative polarity)
  - Small number of hits observed on positive polarity pixels, due to undershoot of the signal pulse
  - Reconstruction performed and residuals good
  - Slight variation in hits with column?