AGH UNIVERSITY OF SCIENCE AND TECHNOLOGY

Development of readout ASIC for luminosity calorimeter in future linear collider

Marek Idzik for AGH-UST group

Faculty of Physics and Applied Computer Science
AGH University of Science and Technology
Cracow Poland

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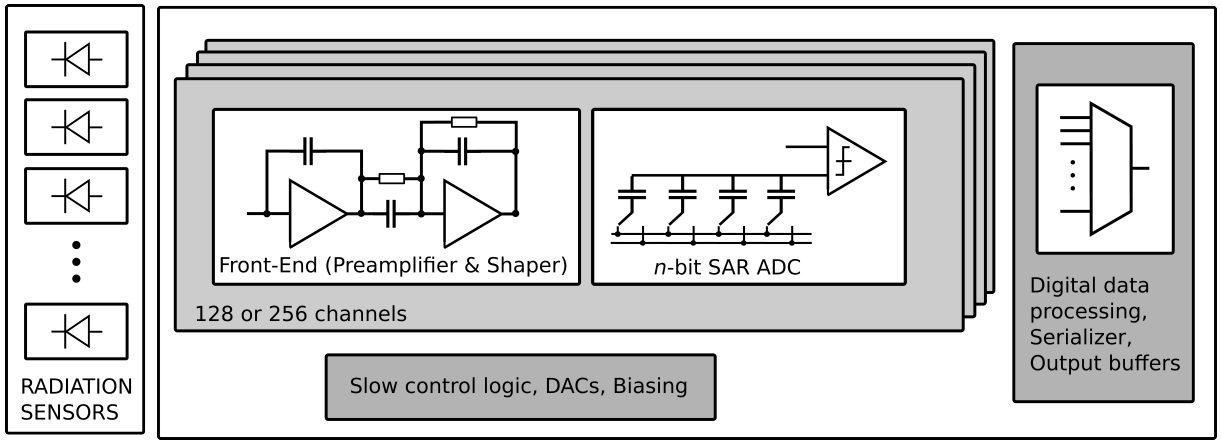
Outline

- General considerations on readout architecture and technology
- Readout architecture and prototype designs under development at AGH-UST
- Summary

What kind of readout ASIC do we need to build compact calorimeter, and not only…



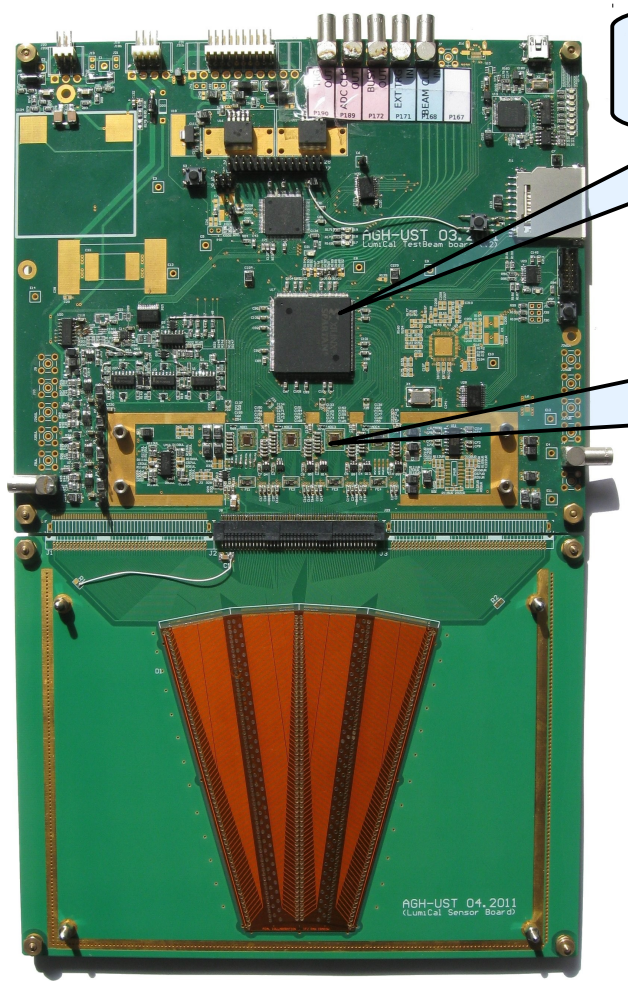
We need multichannel readout ASIC with:

- All functionalities implemented and configured through internal registers,
- All biasing internal,
- Pads - fewer the better: inputs, outputs, power supply,
- No external components (except decoupling caps and maybe reference voltage),
- Ultra-low power, rad-hard, ….
- Maybe some parameters not perfect – FUTURE experiments, PRESENT beam-tests

We need Sytem on Chip (SoC) readout ASIC – very complex,

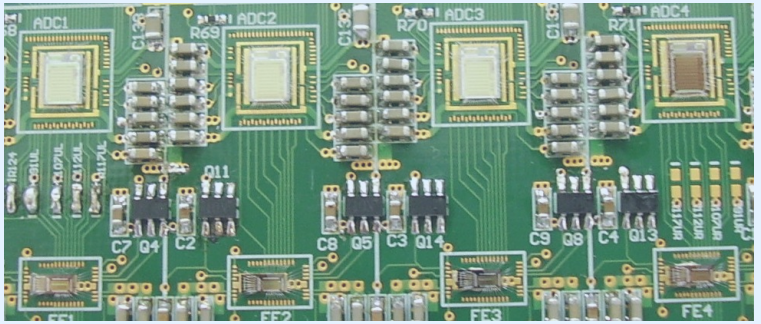
But such development requires a lot of manpower !

What kind of readout we have for LumiCal



FPGA based
back-end electronics

4 pairs of front-end + ADC



A 32-channel detector module contains:

- Four 8 channel front-end ASICs (CMOS AMS 0.35um technology)
- Four 8 channel ADC ASICs (CMOS AMS 0.35um technology)
- FPGA based back-end electronics (developed at AGH-UST)
- Sensor board with kapton fanout

Pros – complete readout

Cons – too many external components/functionalities (e.g. biasing) – NOT COMPACT

What kind of readout architecture and which technology should we choose ?

Architecture

- It is a bit a matter of choice, there are always Pros&Cons
- Probably there is not THE BEST architecture for all applications
- See next slides for our choice...

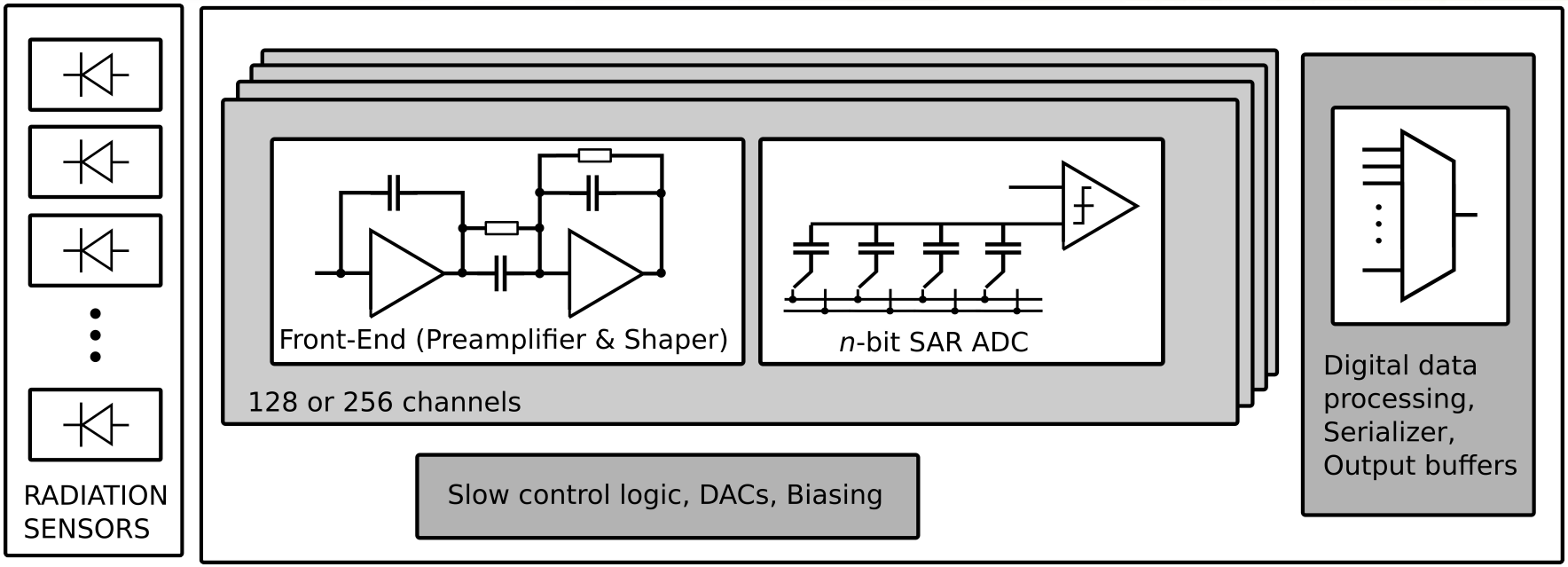
Technology

- Baseline technology at CERN for future experiments is CMOS 130 nm.
- For some (mainly pixel) readouts CMOS 65 nm seems a good choice
- Both 130 nm and 65 nm CMOS offer high speed, very low power, and radiation hardness

Since there is an agreement signed by TSMC, CERN and other groups, which allows to exchange information/blocks for designs in both 130 nm and 65 nm TSMC CMOS, a natural choice is to use these technologies.

We have started with CMOS 130 nm (although we do not exclude 65 nm)

Readout architecture chosen for LumiCal
Maybe also good for other CLIC readouts ?



We have chosen multichannel readout ASIC architecture comprising:

- A dedicated front-end and a **fast low-power sampling ADC in each channel**,
- Data serialization and a fast data transmission
- All functionalities/blocks (e.g. biasing DACs, PLL, DSP,...) needed for SoC ASIC

Such ASIC:

- Allows good amplitude and time measurement
- It is not optimal for all readouts but maybe for some of them...

Fast sampling ADC in each channel the key block of our readout architecture

Motivation - development of CMOS technologies and SAR ADC architecture made it possible to build ultra-low power, fast ADCs with good amplitude resolution

Amplitude measurement

- Resolutions from few bits up to 10-12 bits possible in standard SAR ADC design

Time measurement & sampling frequency

- Time may be obtained from sampling time instance – sampling frequencies up to ~100MSps (depends on number of bits) possible in standard implementation
- More precise timing possible from samples – e.g. using simple CR-RC shaping and deconvolution one can achieve a precision of few % of sampling period. We use deconvolution in the existing FCAL readout

Synchronous/asynchronous operation

- With asynchronous SAR logic ADC does not need a clock and so the ADC trigger may be both: synchronous/asynchronous

Power pulsing

- Using dynamic circuitry the power pulsing is for free: no trigger = no power

Design of SAR ADC at AGH-UST
Status of prototypes in IBM CMOS 130 nm

Main features	LHCb ADC	LumiCal ADC
Resolution	6	10
Sampling frequency [Ms/s]	>80	>40
Power cons. [mW] @40Ms/s	0.35	1
Size [mm^2]	0.016 40 x 400	0.087 146x600
DNL/INL [LSB]	<0.4	~1.0
SINAD@40MS/s[dB]	37.5	>56
ENOB[bits]	5.8	9.3 (at <=20Msps)
FOM [fJ/conv]	~150	~50

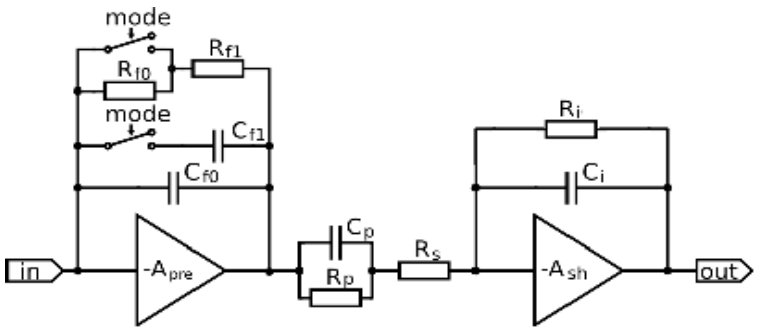
Performance of our ADCs is similar to State-of-the-Art designs

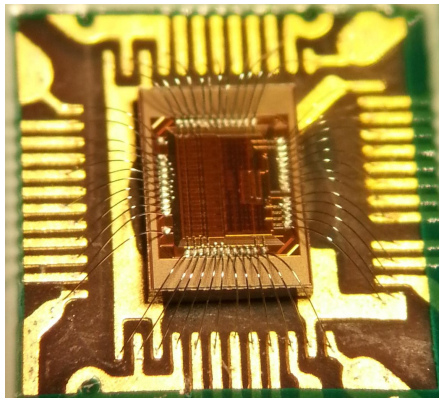
ADC consumes less power than the analog front-end !

M. Firlej, T. Fiutowski, M. Idzik, J. Moroń and K. Świentek, A fast, low-power, 6-bit SAR ADC for readout of strip detectors in the LHCb Upgrade experiment. Journal of Instrumentation, JINST 9 P07006, July 2014

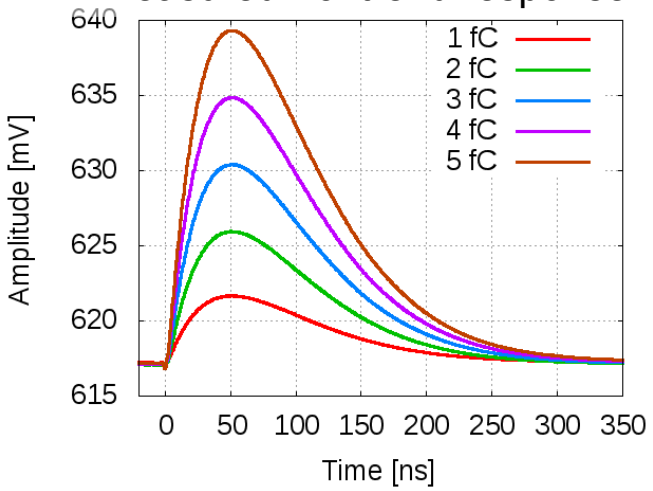
Simple CR-RC front-end for LumiCal in IBM CMOS 130 nm

Channel schematic diagram





Measured front-end response



Main specs:

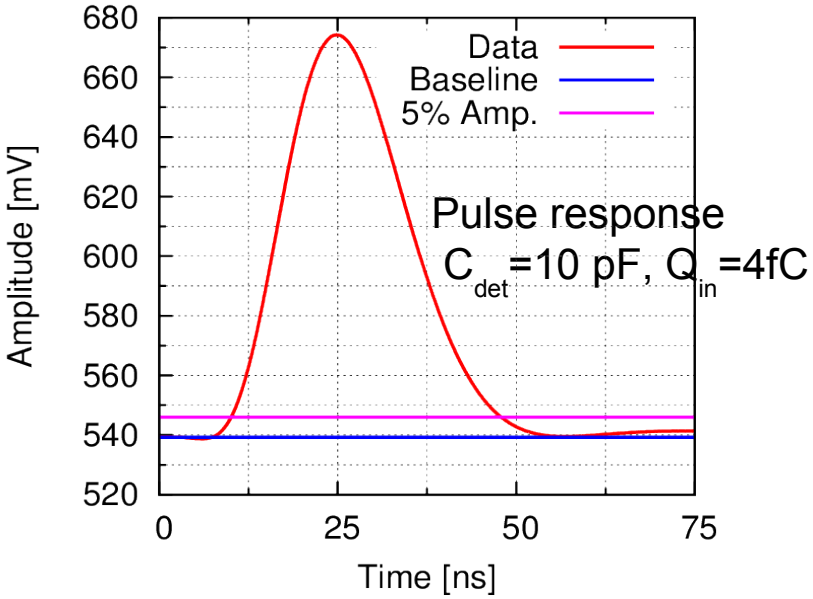
- 8 channels
- Cdet ≈ 5 ÷ 50pF
- 1st order shaper (Tpeak ≈ 50 ns)
- Variable gain:
  - calibration mode - MIP sensitivity
  - physics mode - input charge up to ~5 pC
- Power pulsing implemented
- Power consumption ~1-1.5 mW/channel

We have not decided yet whether it is a final architecture for the LumiCal but we use it because it works well and allows simple implementation of deconvolution.

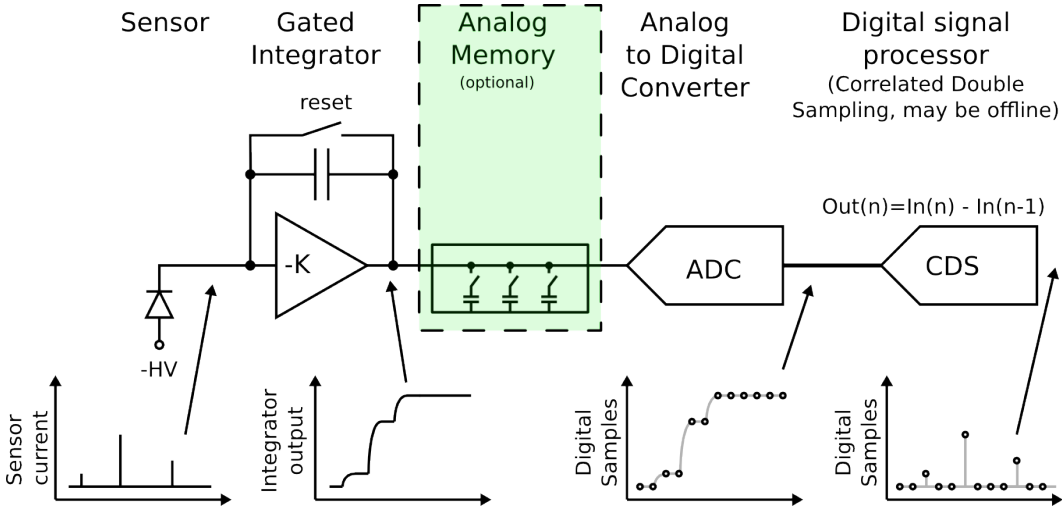
J. Moroń, K. Świentek, M. Firlej, T. Fiutowski, M. Idzik,K. Świentek "Development of front-end electronics for LumiCal Detector in CMOS 130 nm Technology", TWEPP2014 22-26 September 2014, Aix en Provance France, Journal of Instrumentation in print...

Other possible front-ends

For LHCb tracker we have designed in CMOS 130 nm a front-end with Tpeak~25 ns and very symmmetrical pulse



For CLIC we have proposed a front-end with a simple Gated Integrator + CDS. It was not yet designed – manpower...



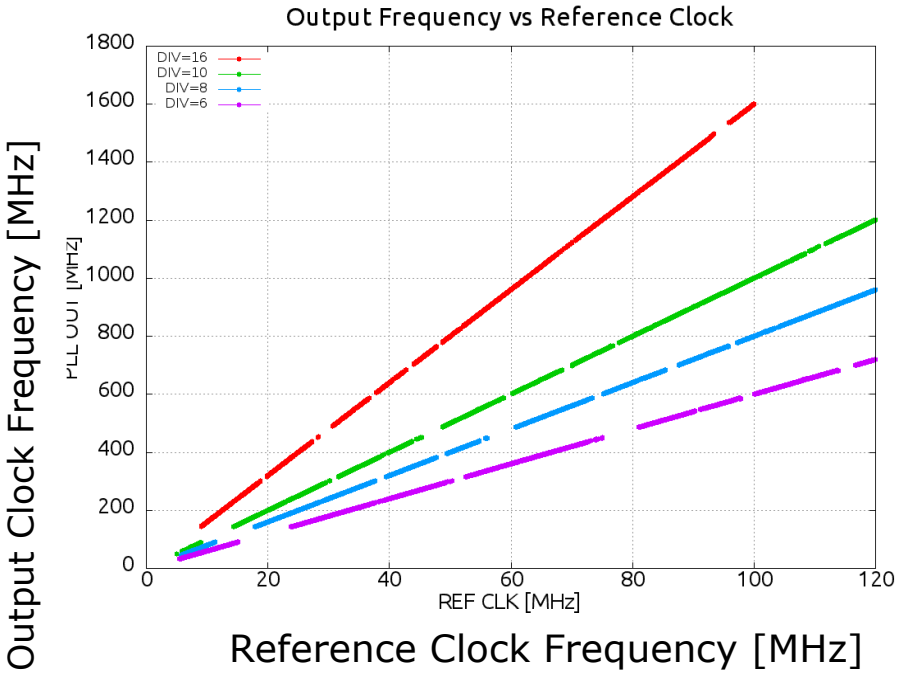
Depending on application various front-ends may be used in our readout architecture

M. Idzik, "A dedicated front-end for readout of strip detectors in the LHCb Upgrade experiment", TWEPP2014 22-26 September 2014, Aix en Provance France

Design of serializer&transmission circuitry PLL, fast I/O interface and other...

Example PLL prototype:

- General purpose PLL block
- Very wide output frequency range: 20MHz – 1.6GHz (SLVS limit.)
- Power consumption ~0.6mW @ 1GHz
- Different loop division factors: 6, 8, 10, 16
- Size 300um x 300um

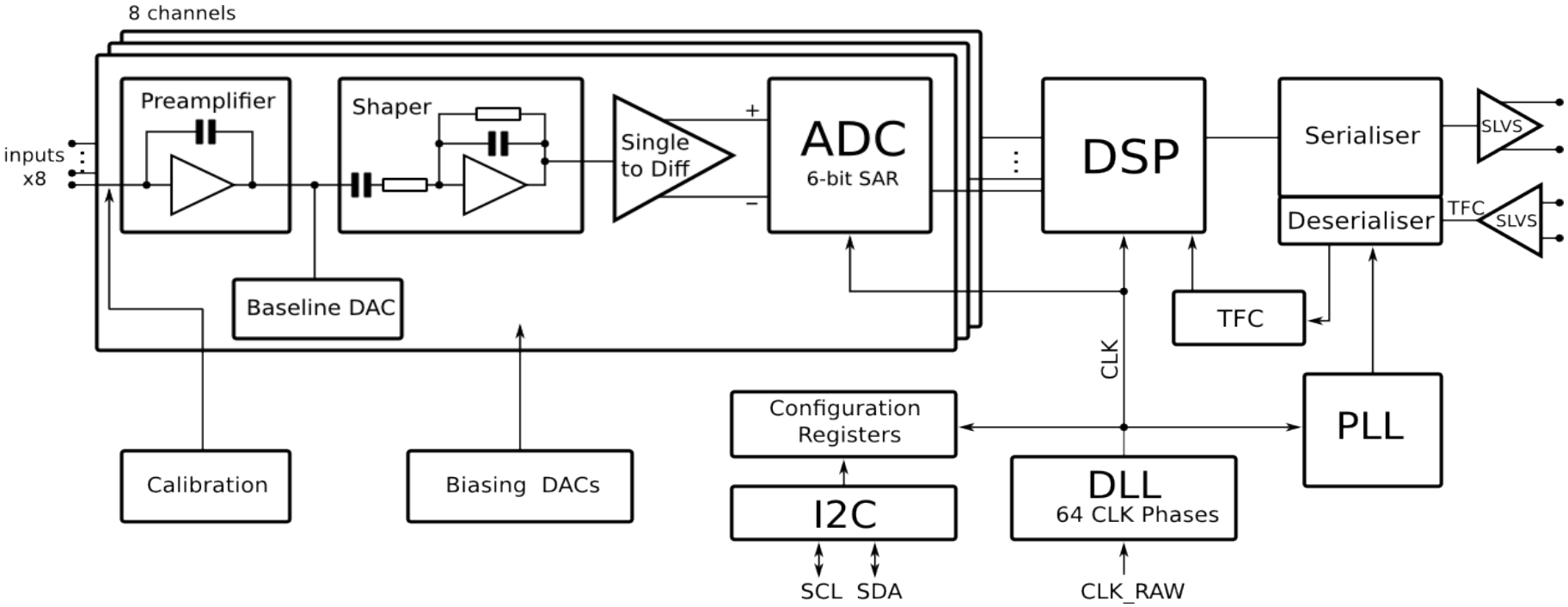


Fast I/O interfaces:

- We have designed and implemented in our chips SLVS I/O working up to ~1 GHz.
- For faster (>=5Gbps) data transmission we started development of CML/SST I/O

M. Firlej, T. Fiutowski, M. Idzik, J. Moroń, K. Świentek, "Development of variable frequency, power Phase-Locked Loop (PLL) in 130nm CMOS technology , TWEPP2013 23-27 September 2013, Perugia Italy

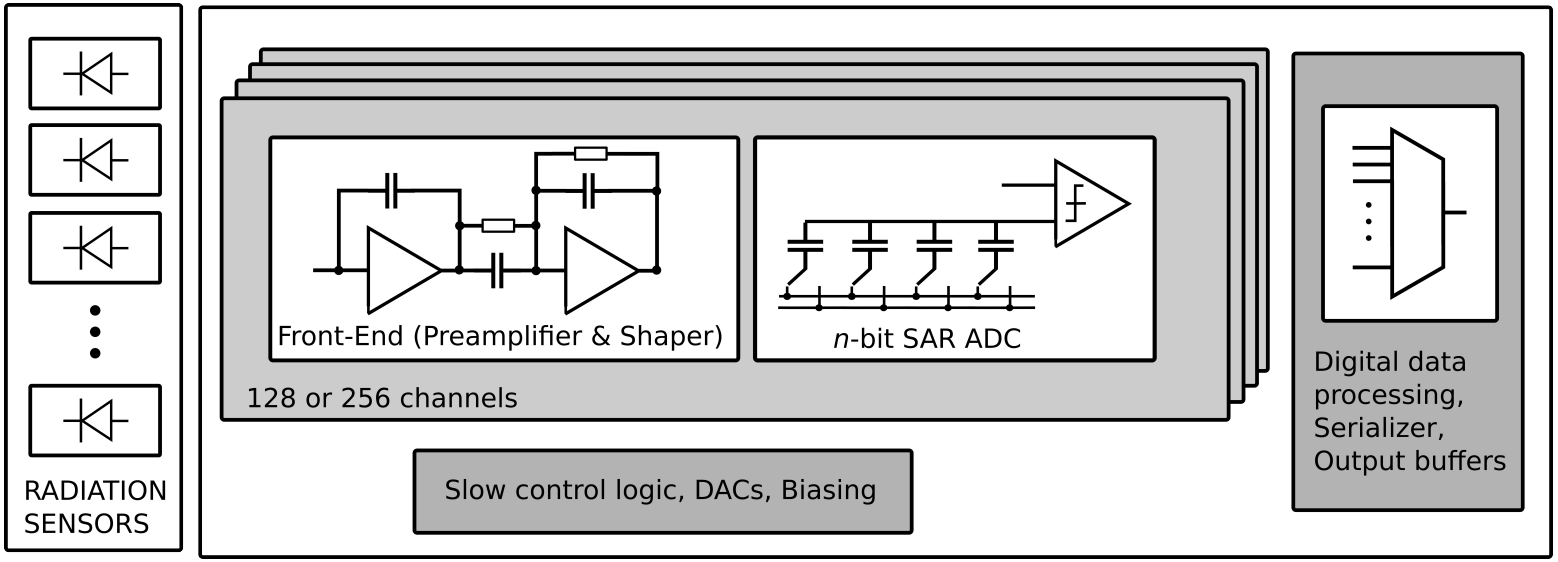
Lets put all blocks together
Example of readout ASIC for LHCb strips in TSMC 130 nm, almost ready for submission...



We are just completing the design of 8 channel prototype ASIC for LHCb readout. This ASIC will offer almost full functionality of the final 128 channel chip, and will contain:

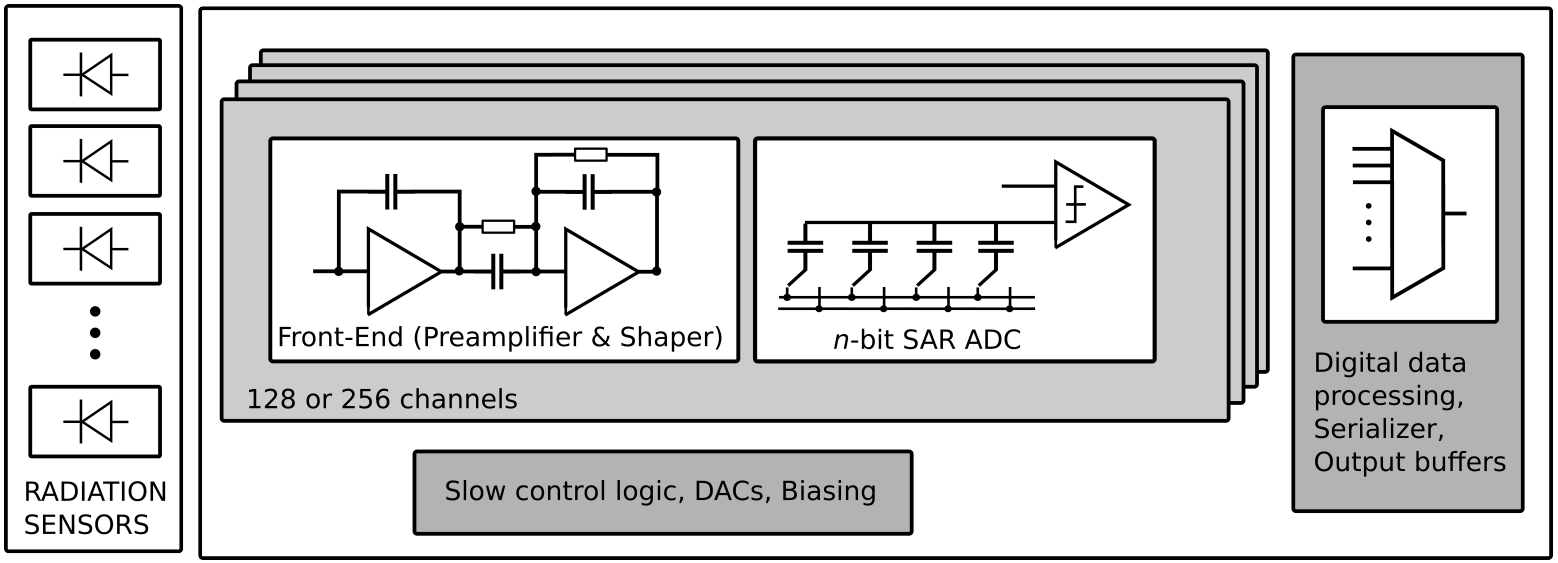
- Pre-amplifier, Shaper, Single-2-Diff converter, 6-bit SAR ADC, DSP (bad channel masking, pedestal and common mode subtraction, zero suppression), PLL, DLL, I2C, SLVS I/O, serializer, deserializer, various DACs.

Plans for LumiCal – short term (this year)



- In 2015 we'd like to submit an ~8-channel CMOS 130 nm chip containing front-end (probably CR-RC, for deconvolution) and ADC in each channel + serialization (one digital output per channel - output frequency 10 x f_{sample}) + all biasings + digital control
- In principle it should be good enough for COMPACT calorimeter

Plans for LumiCal – longer term



- In next ~2 years we would like to add DSP and very fast (>=5Gbps) serialization/data transmission and fabricate it in CMOS 130 nm (maybe even 65 nm...)

Summary

- Our experience says that the chip becomes really useful only when it contains most of funtionalities/biasings and does not need many external components/settings, so our goal is a SoC type readout ASIC
- For LumiCal readout we have chosen the architecture containing fast sampling ADC in each channel and we are working on several components of such readout. Maybe it could be interesting also for other CLIC readouts...
- We would like to submit a small readout ASIC (~8 channels) for LumiCal in 2015

Thank you for attention