

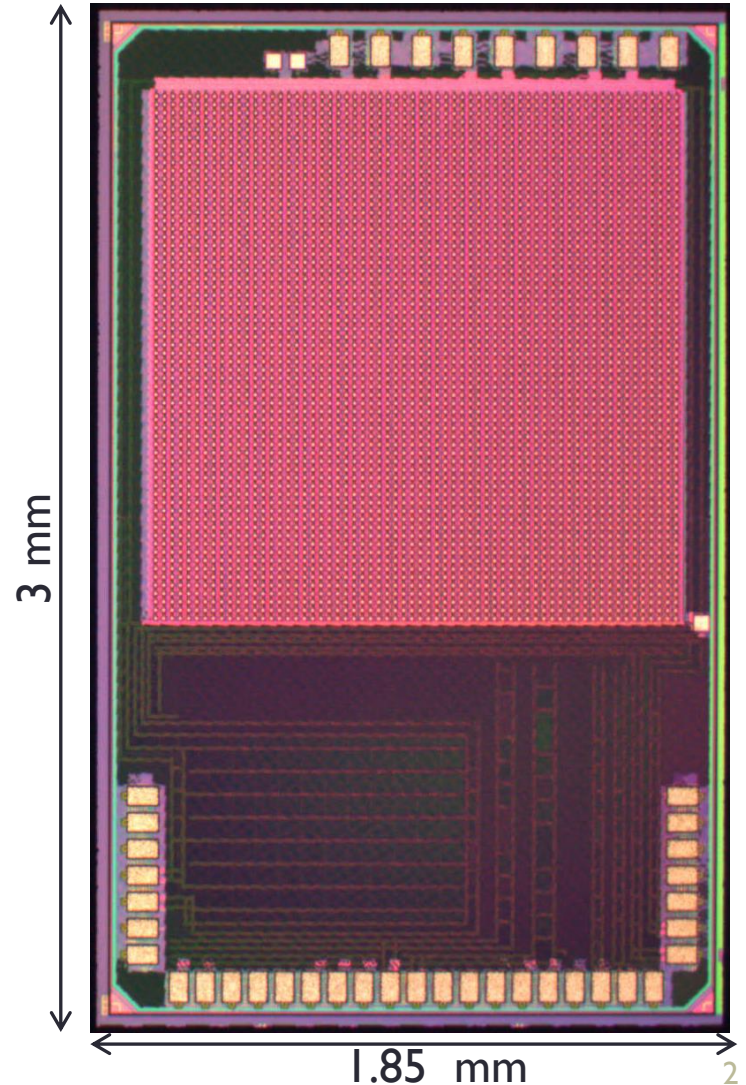
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# **DESIGN CONSIDERATIONS FOR CLICPIX2 AND STATUS REPORT ON THE TSV PROJECT**

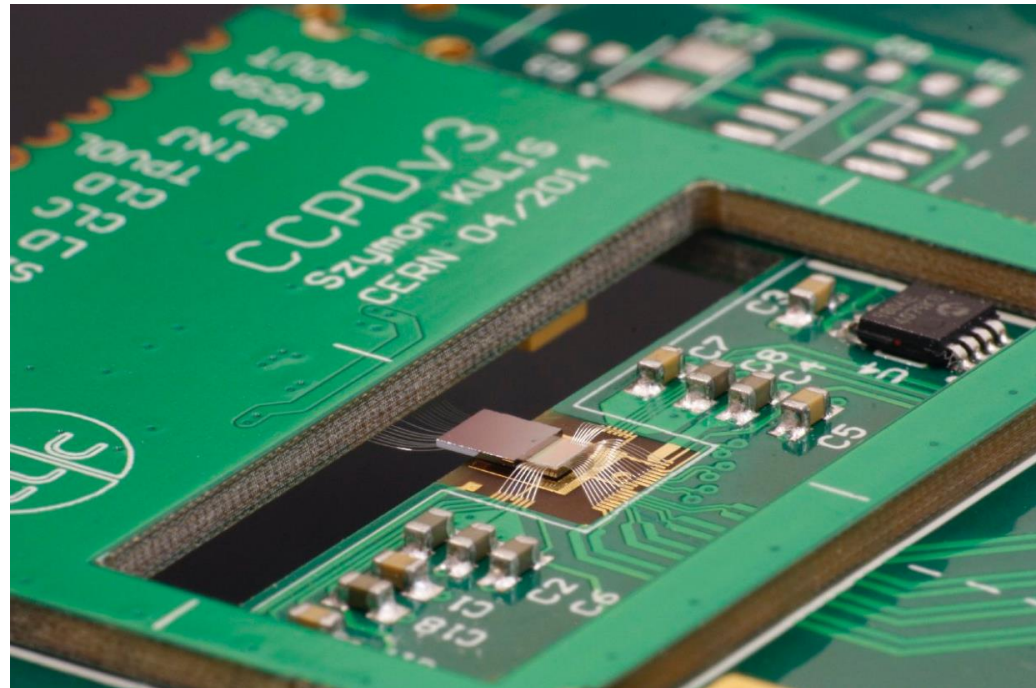
# CLICpix

- CLICpix is a **hybrid** pixel detector to be used as the CLIC vertex detector
- Main features:
  - small pixel pitch ( $25\ \mu\text{m}$ ),
  - Simultaneous TOA and TOT measurements
  - Power pulsing
  - Data compression
- A demonstrator of the CLICpix architecture with an array of  $64 \times 64$  pixels has been submitted and tested



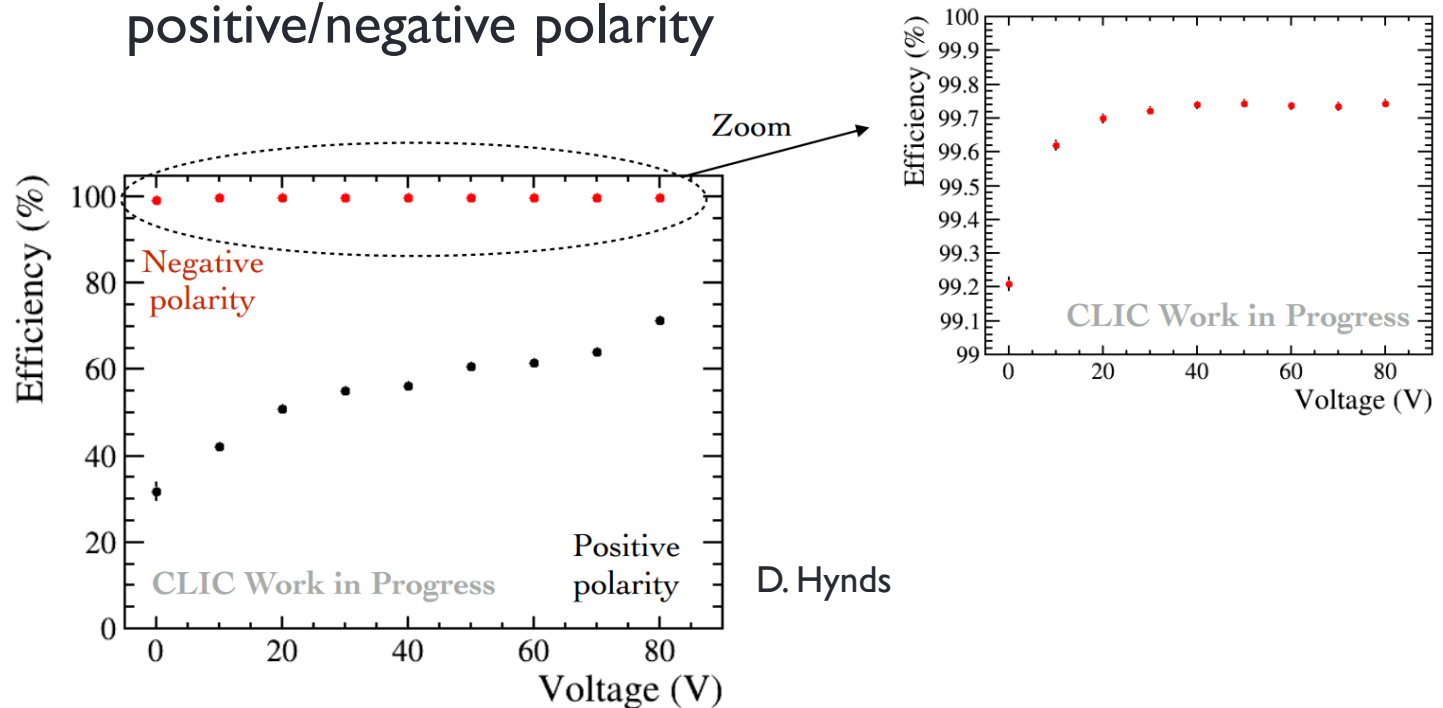
# Current results

- Latest results on CLICpix were presented by Daniel Hynds before
- The chip works well and it provides a good proof-of-concept for a CLIC vertex detector built with current technology
- CLICpix has been tested in a test-beam scenario using an HV-CMOS sensor. Tests with a Si sensor are planned for the future

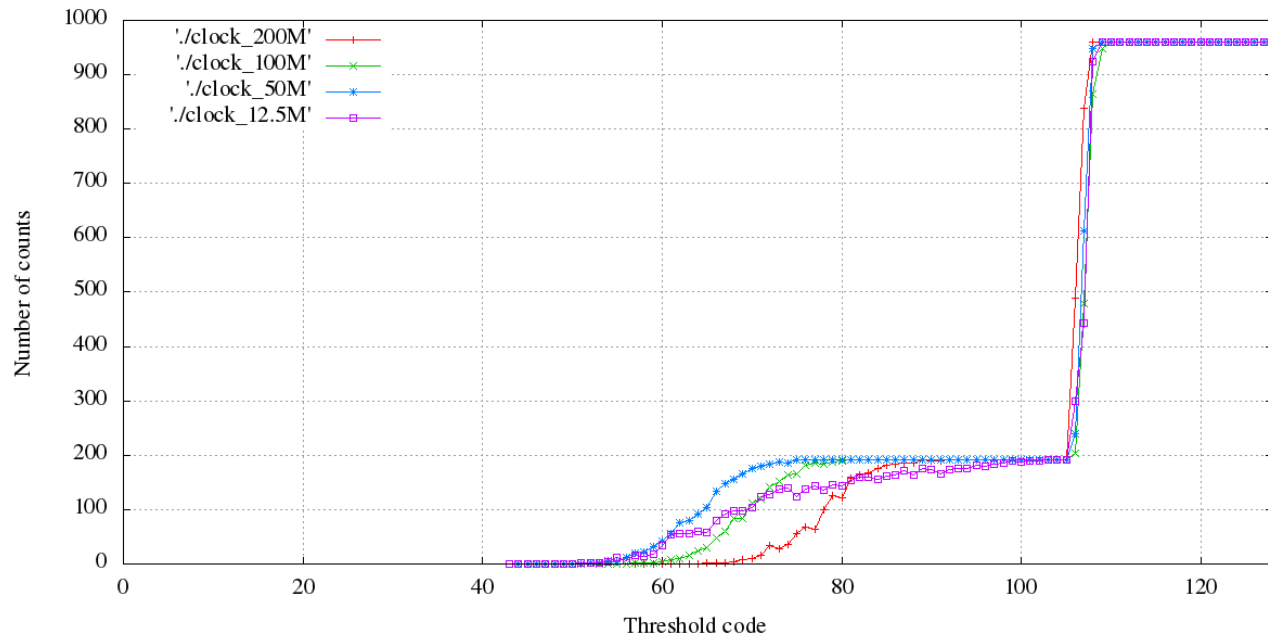


# Issues with the current chip

- However, the current chip has a few issues...
- **Charge injection** from discriminator output to the input pad.
  - This is the most serious issue. It changes the minimum threshold significantly and creates a difference between left/right pixels in a double column and between positive/negative polarity



# Other issues



- Other smaller issues are also present:
- Charge injection from digital side
  - This issue is more limited and it causes increased noise for a certain range of clock frequencies.
- Compression bug
  - Very simple logic bug that slows down the readout when using cluster/column compression

# Design limitations

- Small counters
  - 4 bits TOA is not enough (even for a CLIC application)
    - We require a 10 ns accuracy over a 160 ns period, so we need 5 bits to accommodate for chip-to-chip timing calibration
  - 4 bits TOT is enough, but a longer counter would allow more accurate measurements
  - 4 bits event counter results in really long and tedious testing routines
- Small matrix (64 by 64 pixels)
  - Small area increases the time it takes to get statistics
- “Clunky” readout
  - A few interface design choices resulted in a more complicated test setup than what was foreseen

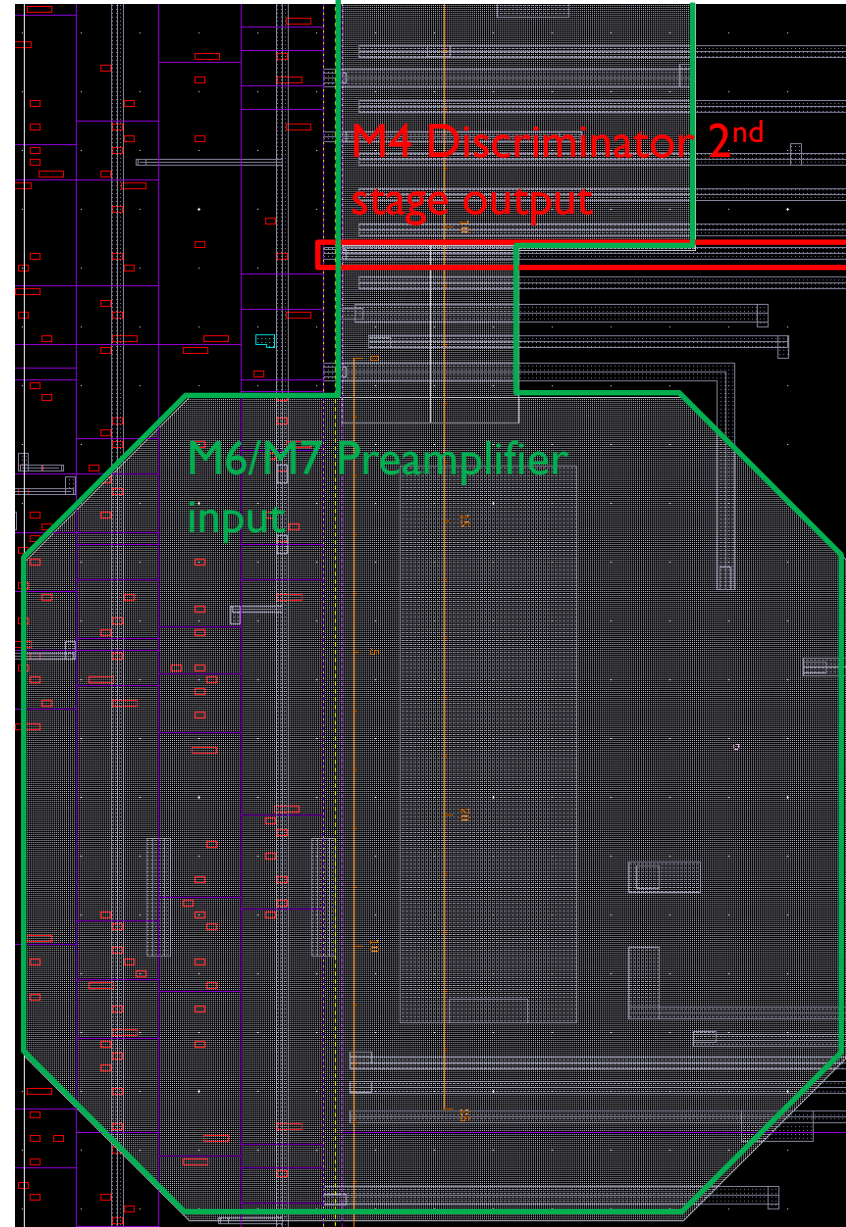


# CLICpix2: Architecture improvements

- Larger Counters
  - 6 bits TOT for more accurate energy measurements
  - 8 bits TOA should be possible – a total of 14 bits is most probably achievable, but it needs to be validated
  - A new mode of operation with a single 14 bits counter for ToA / Event Counting
- Larger matrix (128 by 128)
- More convenient readout
  - 8/10 bit encoding for high speed readout
- A few more IP blocks can be used (and tested), such as a band-gap

# Bug fixing

- Implement a better shielding to avoid noise injection and achieve a lower minimum threshold
- Fix small bug in the readout logic
- Increase comparator gain to be less sensitive to cross-talk from the digital pixels
- Improve the test-pulse mechanism to have easier and more accurate testing routines





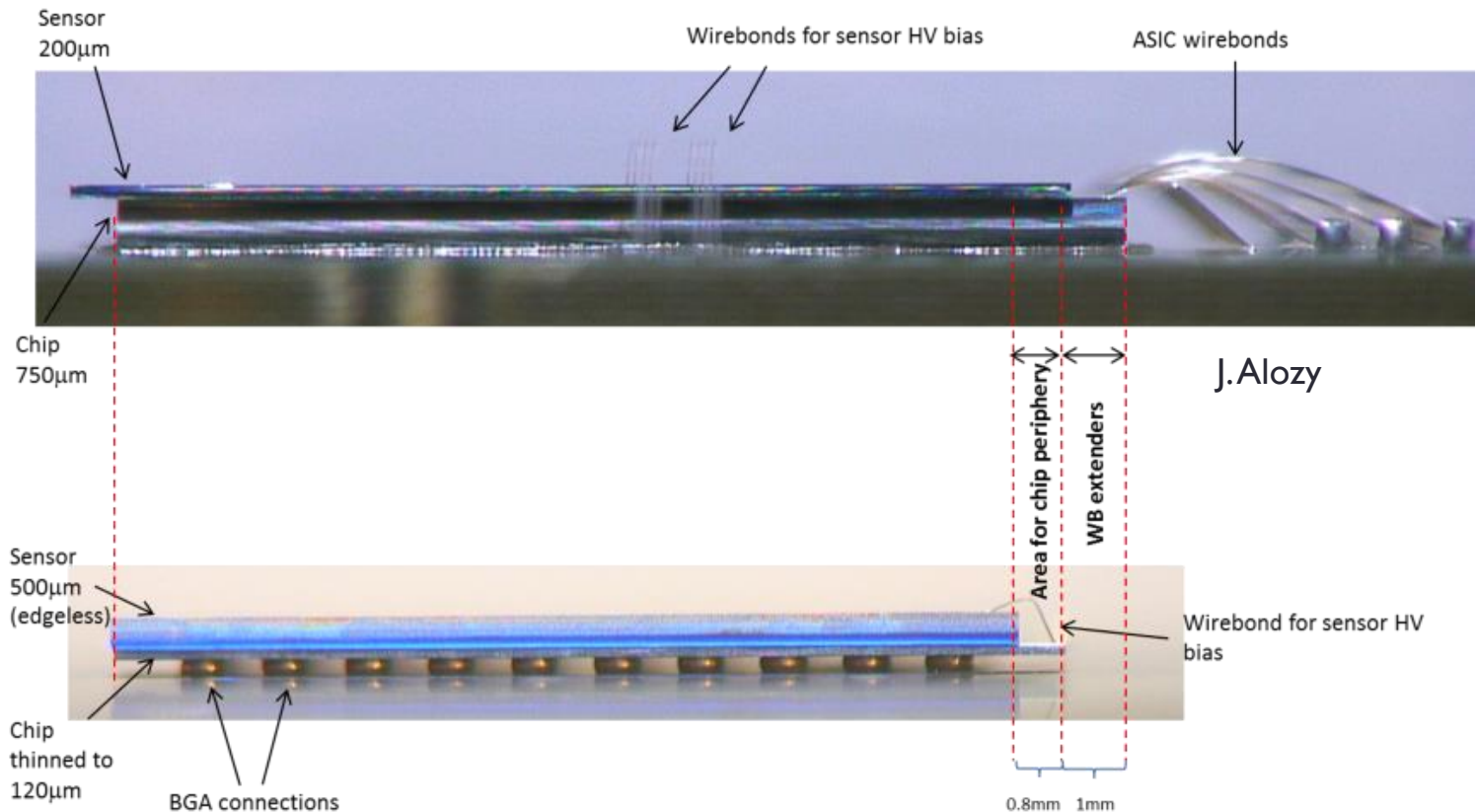
# Project status

- The analog part of the pixel was updated and re-simulated successfully
  - This part needs to be laid out again from scratch to merge structures among adjacent pixels and to reduce cross-talk
- The digital pixel part was modified and fixed. However, a more robust testbench for the digital side is required to avoid bugs
- IP blocks need to be integrated
- Periphery blocks must be updated to correctly manage the larger pixel matrix

# The Medipix TSV project

## Objectives :

- » Fabrication of a read-out chip with Through-Silicon Vias (TSV)
- » Assembly of a particle detector on top of it



# TSV second run

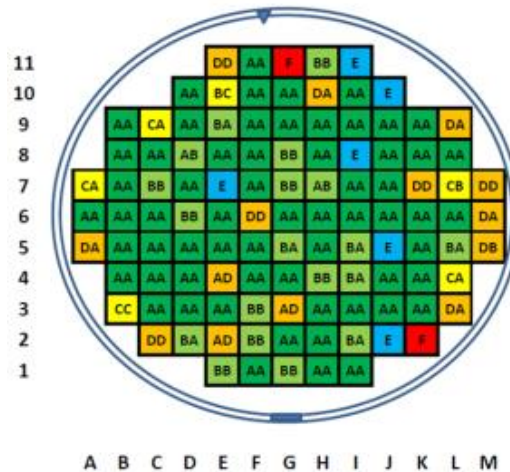
- Launched in CEA LETI (Grenoble) in March 2014 and delivered to CERN in October 2014
  - The main motivation of the second run was to obtain good yields in order to validate the TSV process applied on Medipix chips
- Lot #  $\mu$ SA999P of 3 wafers:
  - P04 (W128-AZPGBPH) : completed, delivered to CERN and tested
  - 14 chips (7 class AA + 7 with other classes) sent to ADVACAM for assembly First assemblies recently received. Test in progress.
  - P05 (W127-AKPGALH) : need rework (during 3D06)
  - P06 (W126-AMPG6LH) : completed, delivered to CERN and tested
- Lot #  $\mu$ SB254P of 3 wafers
  - P01 (W125 A3PGC2H) : completed, delivered to CERN and tested
  - P02 (W124 ACPGAUH) : completed, delivered to CERN and tested
  - P03 (W123 A0PGBNH) : completed, delivered to CERN and tested

# TSV second run

We obtained very encouraging results and we have enough good chips to validate the process

\* Original wafer probing results  
(Foundry yield)

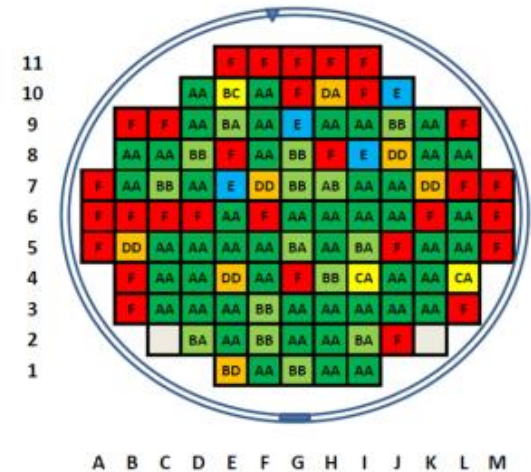
W128\_AZPGBPH\_before\_TSV



AA	62	57%
BB, BA or AB	19	17%
CC, CA, AC, BC or CB	6	6%
D	14	13%
E	6	6%
F	2	2%
Total	109	100%

After foundry production and TSV added process the final yield is 45% of fully functional chips

W128\_AZPGBPH\_after TSV



AA	48	45%
BB, BA or AB	15	14%
CC, CA, AC, BC or CB	3	3%
D	7	7%
E	4	4%
F	30	28%
Total	107	100%

C2 and K2 were not received

	Lot # $\mu$ SA999P			Lot # $\mu$ SB254P		
	P04	P05	P06	P01	P02	P03
Perfect chips before TSV	57%	51%	50%	50%	60%	53%
Perfect chips after TSV	45%	41%	In rework	20%	41%	38%

# TSV third run

- LOT1: **stopped** with TSV-last seed deposition due to presence of residues in via bottom
  - estimated delivery date: moved from mid November 14 to February 2015
- LOT2: at TSV etching, **stopped** until polymer issue is solved
  - LOT2 estimated delivery date: moved from end of December 14 to march 2015



# TSV third run

- Some arcing effects at wafer edge were observed after hard mask etching
  - Arcing issue is a well know problem with silicon on “spin on glass” wafers due to capacitive effect of substrate on electrostatic chuck
  - Problem has been fixed on 120  $\mu\text{m}$  thick wafers (no issue on last run)
- With 50  $\mu\text{m}$  wafers the capacitance increases and makes the process more sensitive
- The issues are more important because of the presence of defects at the edge of the wafer : glue or lithography resin residues. No arcing on Si test wafers
- These defects are limited to the very edges of the wafer an good dies should not be affected
- Polymer residues were observed at TSV bottom after RDL lithography step of LOT#1. It has been decided to stop the process to try to remove the residues and investigate how to avoid this effect on LOT#2



# **THANKS FOR YOUR ATTENTION**

Your input for CLICpix2 is welcome!!