ATLAS/CMS Tracker Upgrade Technologies

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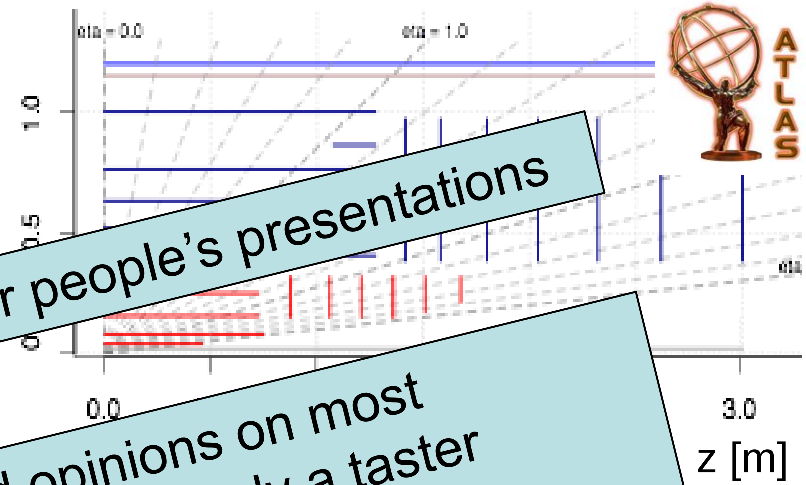
On behalf of the ATLAS and CMS Upgrade Communities
Slides "borrowed" from a cast of thousands

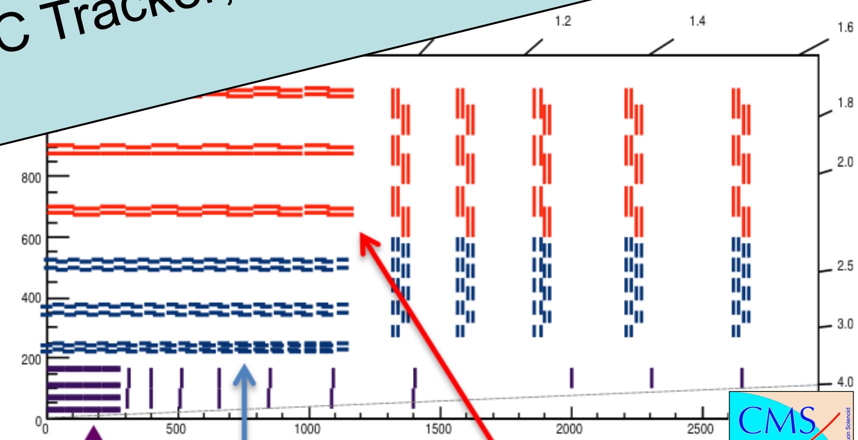
Introduction

- Or how I was roped into this….
  - Led US CMS module testing for current detector, now Deputy Project Leader for ATLAS Strip Upgrade and leading Liverpool ATLAS upg…
- At first glance … upgrades look … in terms of layout and size
  - But the…
  - …gering
  - …TLAS, Self-seeded-CMS
  - Leads to different technologies being used in each layout
    - More for you all to borrow

Disclaimer 1: Most of talk taken from other people's presentations

Disclaimer 2: This talk based on my biased opinions on most applicable technologies/lessons for CLIC Tracker; only a taster possible in 25 minutes

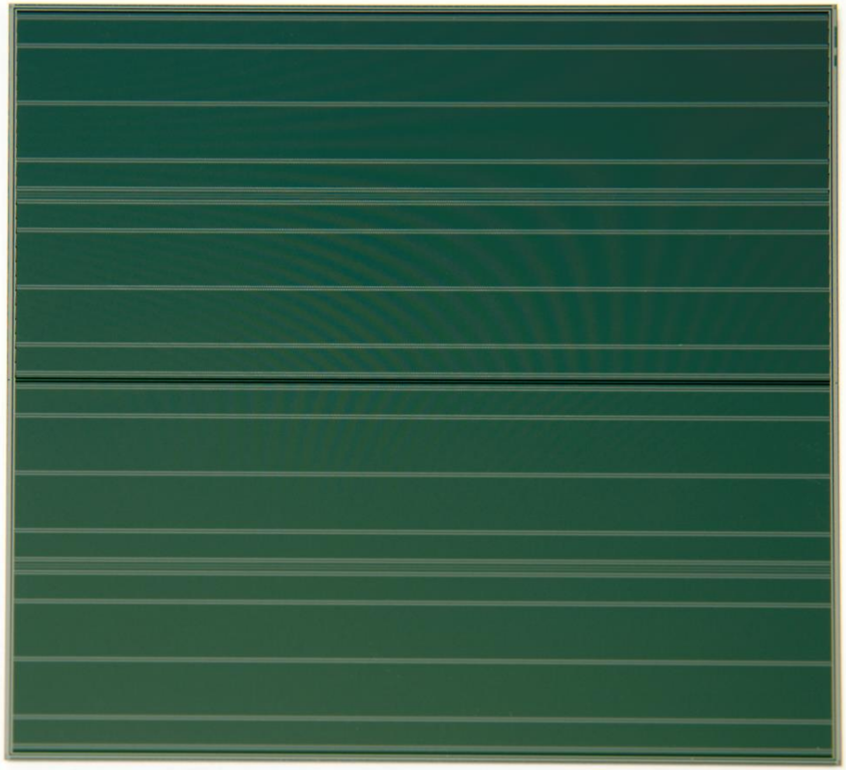


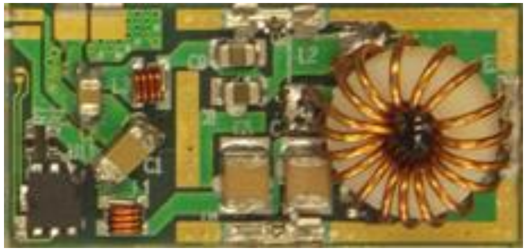


Pixels - Macro-Pixel/Strip & Strip/Strip modules

Common Technical Solutions

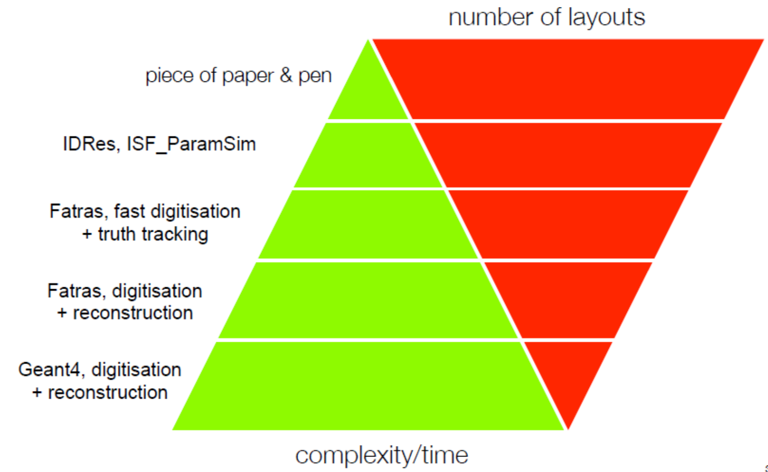
- Planar silicon sensor. Most likely n-in-p FZ 300 μm physical thickness.
- Both experiments are designed without advanced alignment hardware. Both will plan to align using initial metrology and tracks.
- Both trackers are using DC-DC converters as baseline for LV





ATLAS Layout Optimization Process

- Layouts are tested with progressing complex simulations
  - Fast simulation good for hit coverage, efficiency, resolution estimates
  - Fake rates, vertexing, particle-ID and B-tagging all require detailed simulation for needed precision



Tool Matrix

	material maps	inactive/noisy channels	inactive modules	alignment studies	pile-up studies					
piece of paper & pen	-	-	-	-	-					
IDRes	-	-	-	-	-					
Fatras, fast digitisation + truth tracking	<5%	-	+	o	-					
Fatras, digitisation + reconstruction	<5%	+	+	+	+					
Geant4, digitisation + reconstruction	+	+	+	+	+					

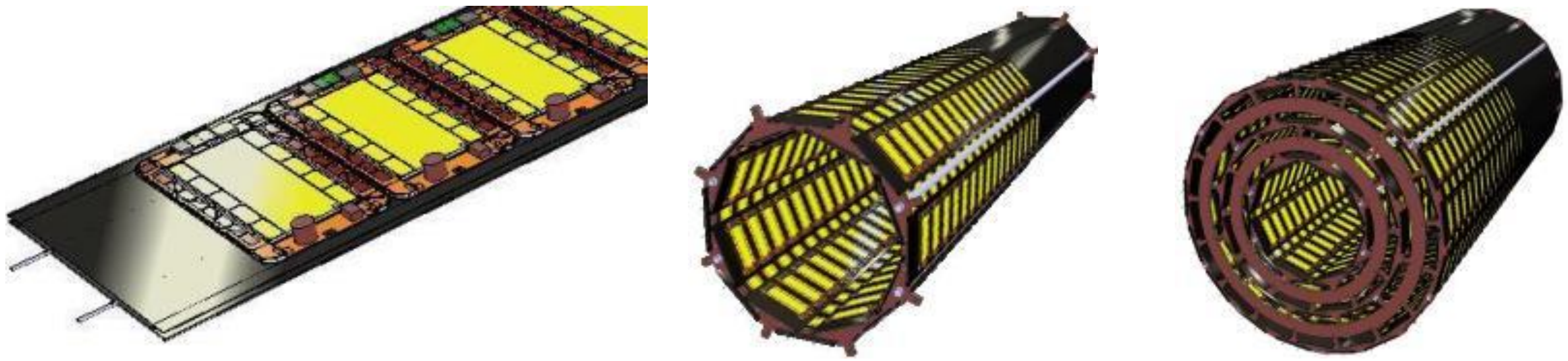
Performance Matrix (guesstimates & achievements)

	hit coverage	resolution (singleP)	efficiency (singleP)	resolution (jets)	efficiency (jets)	fake rate	vertexing res.	vertexing fakes	vertexing eff.	btagging
piece of paper & pen	5%	10%	-	15%	-	-	-	-	-	-
IDRes	2%	10%	-	15%	-	-	-	-	-	-
Fatras, fast digitisation + truth tracking	+	<5%	<5%	5%	5%	<5%	<1%	<1%	<1%	15%
Fatras, digitisation + reconstruction	+	~1%	+	<5%	<5%	+	+	+	+	<10%
Geant4, digitisation + reconstruction	+	+	+	+	+	+	+	+	+	+

Barrel with PS modules (BPS)

baseline version

- Inner layers are mixed pixel-strip modules (PS)
- Support plates with embedded cooling
  - Modules are glued to the plates
    - Plate design and gluing technique to be developed!
  - Plates are joined to form concentric layers
- Radiation length is 3.5-4.0%



PS modules

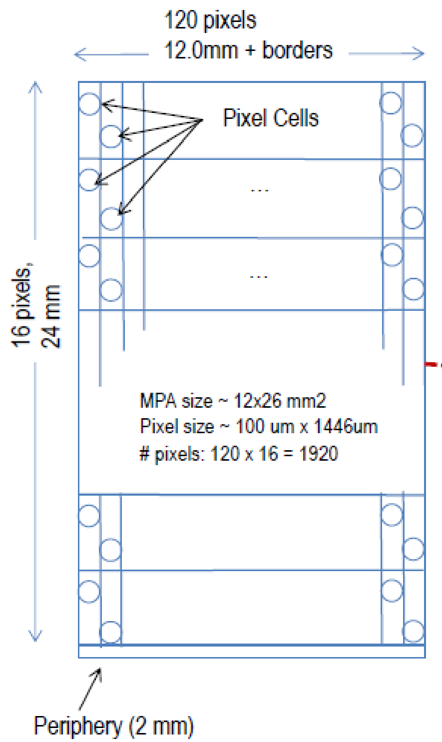
PS module

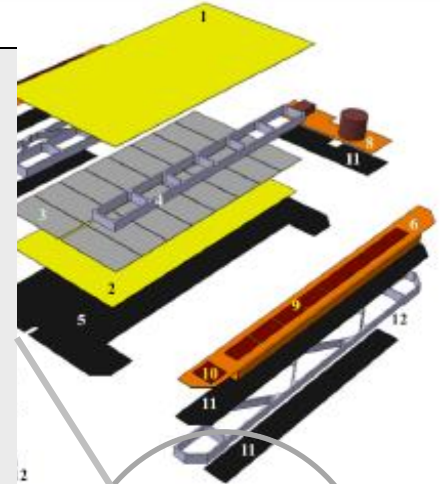
2.4cm×100µm
coupled macro

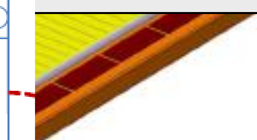
Front-end electr
and
corr

AlCF - carbon fibre reinforced aluminium

property	V2-7	V2-4
in-plane thermal conductivity (W/m/K)	200	230
rmal conductivity (W/m/K)	125	120
pm/K)	7	4
E (ppm/K)	24	24
us (GPa)	90	98







Low-mass mechanical structures optimized for cooling

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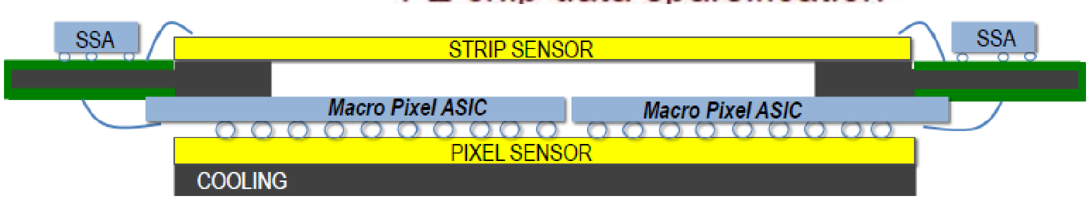
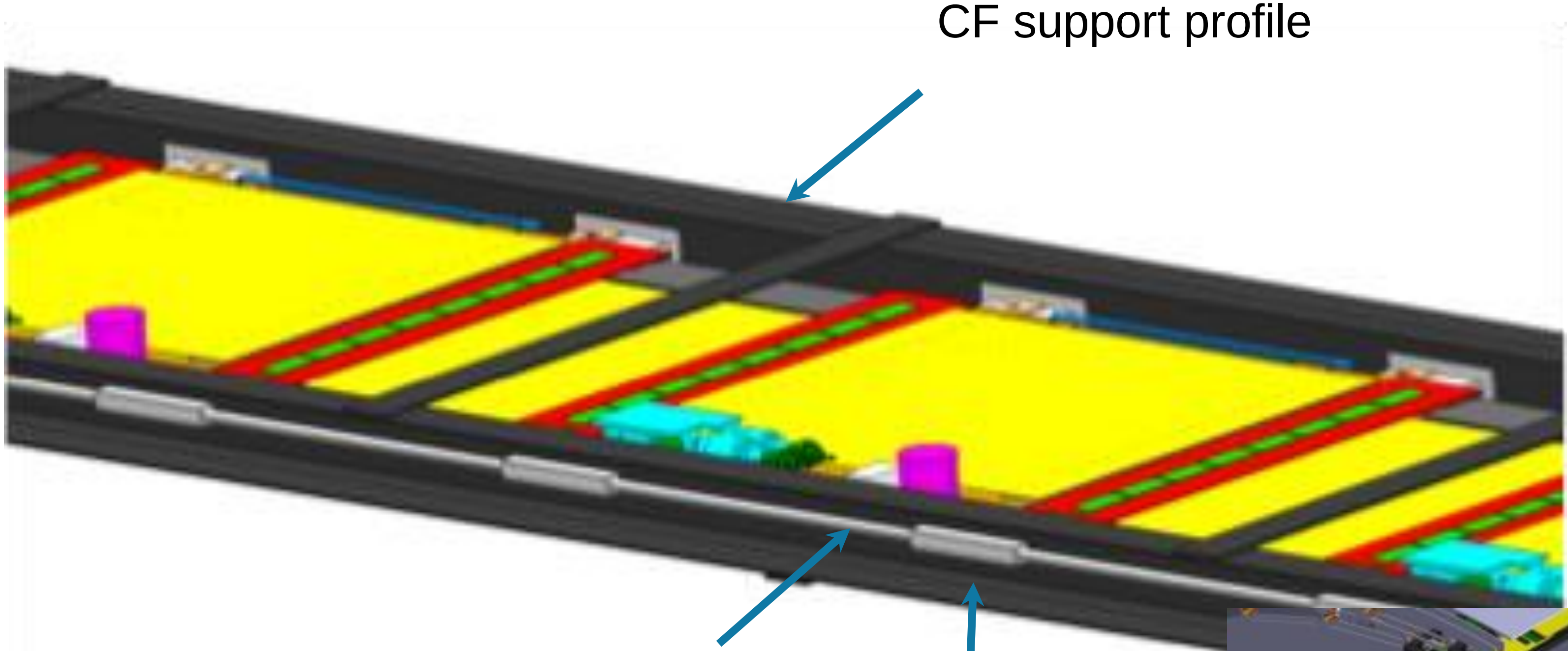
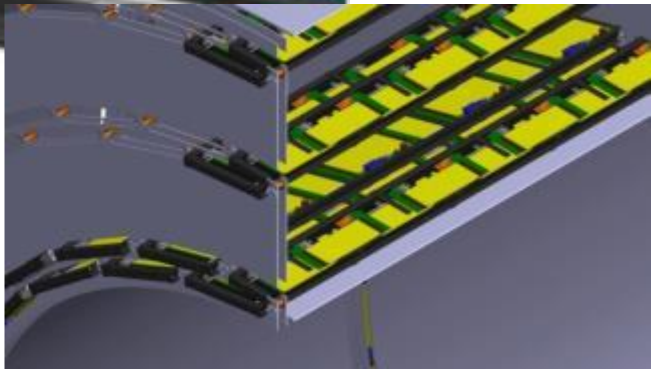
CIC (Concentrator IC):
FE chip data sparsification



Barrel with 2S modules (B2S)





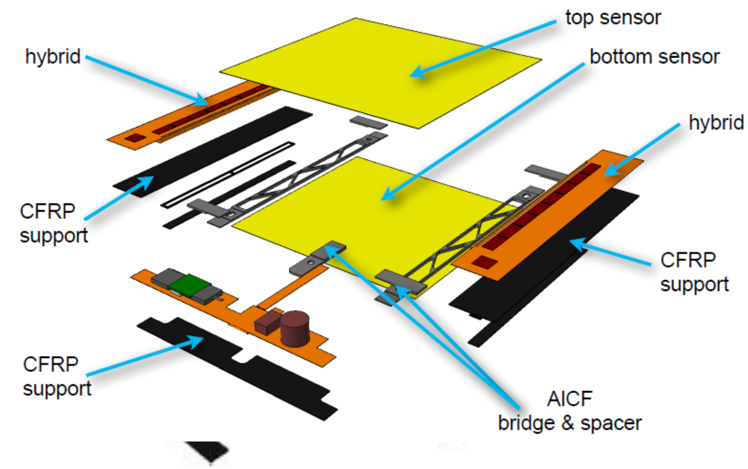
Outer layers are double axial strips
Radiation length of 2-2.5%

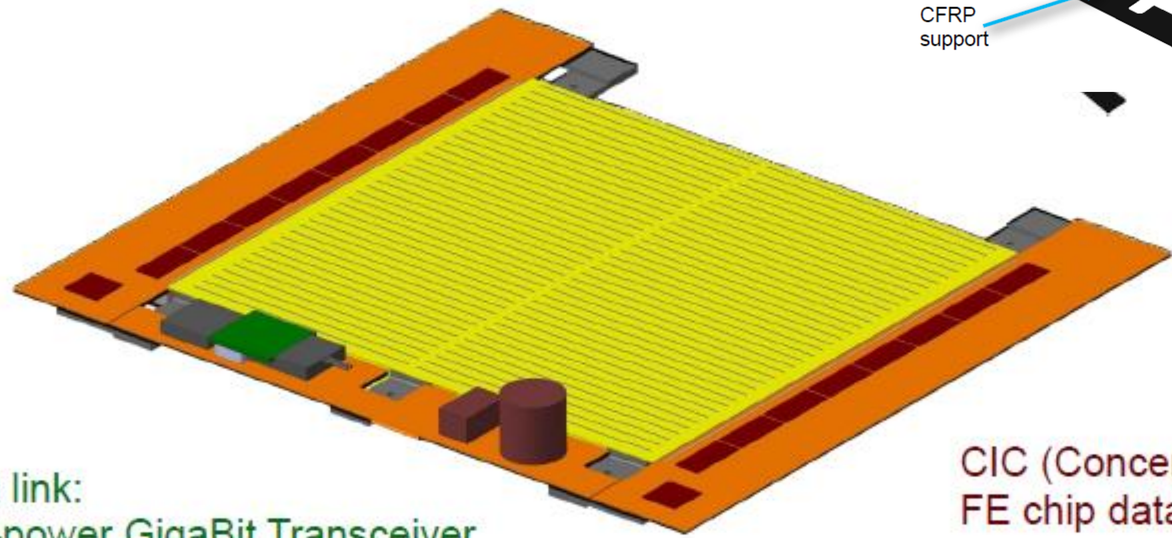
2S Modules

2S module

5cm×90µm AC coupled strips (both sides) pitch, ~10x10cm^2,P~4W

Front-end electronics (CBC chips), specialized for strips features top/bottom sensor correlation





Low-mass mechanical structures optimized for cooling

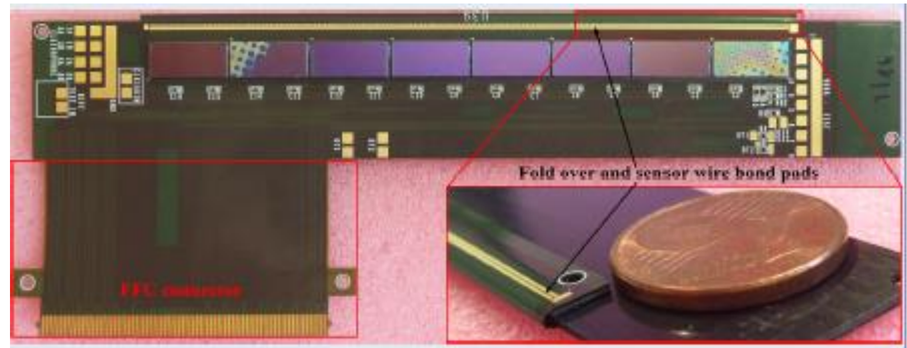
CIC (Concentrator IC): FE chip data sparsification

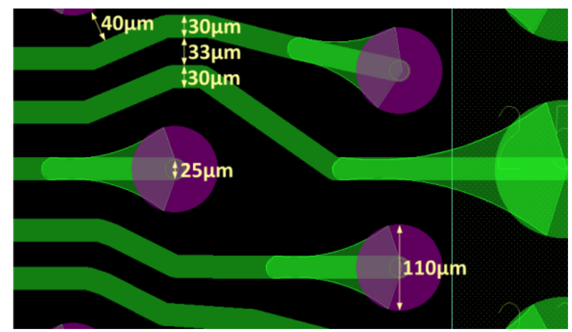
Data link: Low-power GigaBit Transceiver (LpGBT) + laser driver currently under development

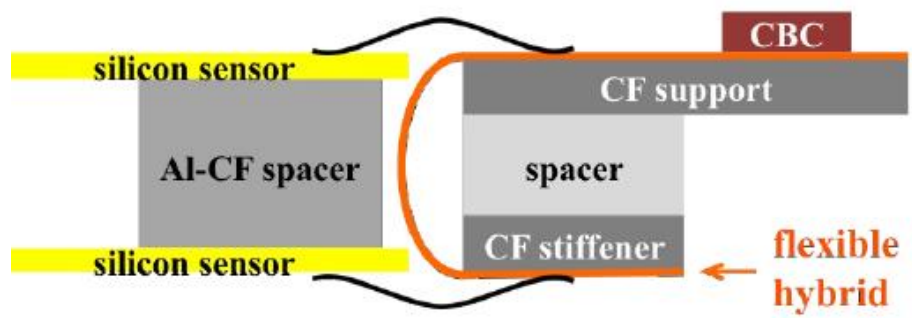
DC/DC converter (already foreseen in Phase-1 pixel project) 10-12V lines: lower current, lower material

Producibility and Hybrid Technology

- CMS is targeting producibility through industrialization
  - Hybrids are laminated on the CF supports by the company
  - CBC is C4 bumped in industry
- Hybrids require fine pitches for tracking into/out of the CBC bump array
  - 30 μm/30 μm track and gap
  - The technology's thin dielectrics minimizes material and bends well over the Al-CF spacer.
  - Total thickness of hybrid of 130 μm





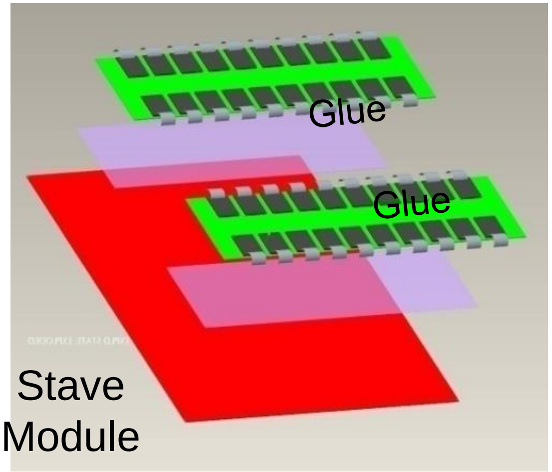


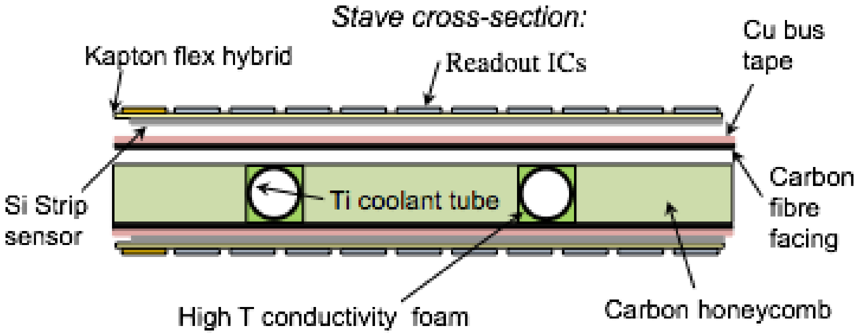
Stave+Petal Programme

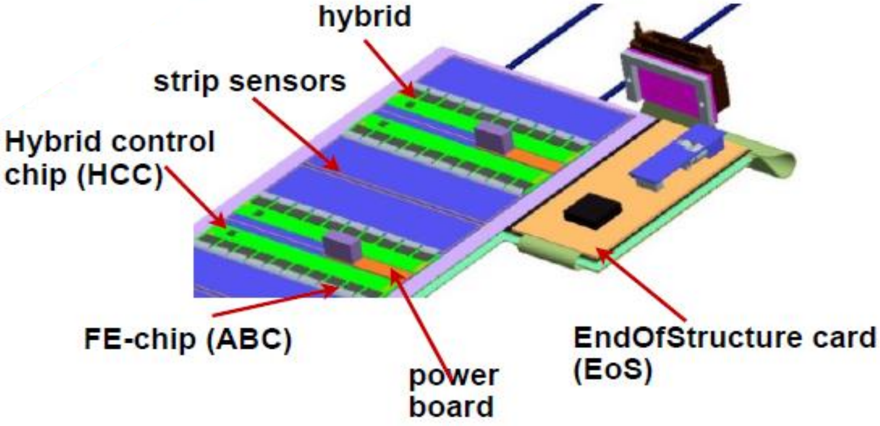
•ATLAS is pursue simplicity for improved producibility
•Silicon modules glued directly onto a cooled carbon fibre plank
•Designed to reduce radiation length

- Minimize material by shortening cooling path
- Kapton service tapes co-cured onto CF skins

- All components independently testable prior to construction
- Design aims to be low cost-
  - *Minimize specialist components*

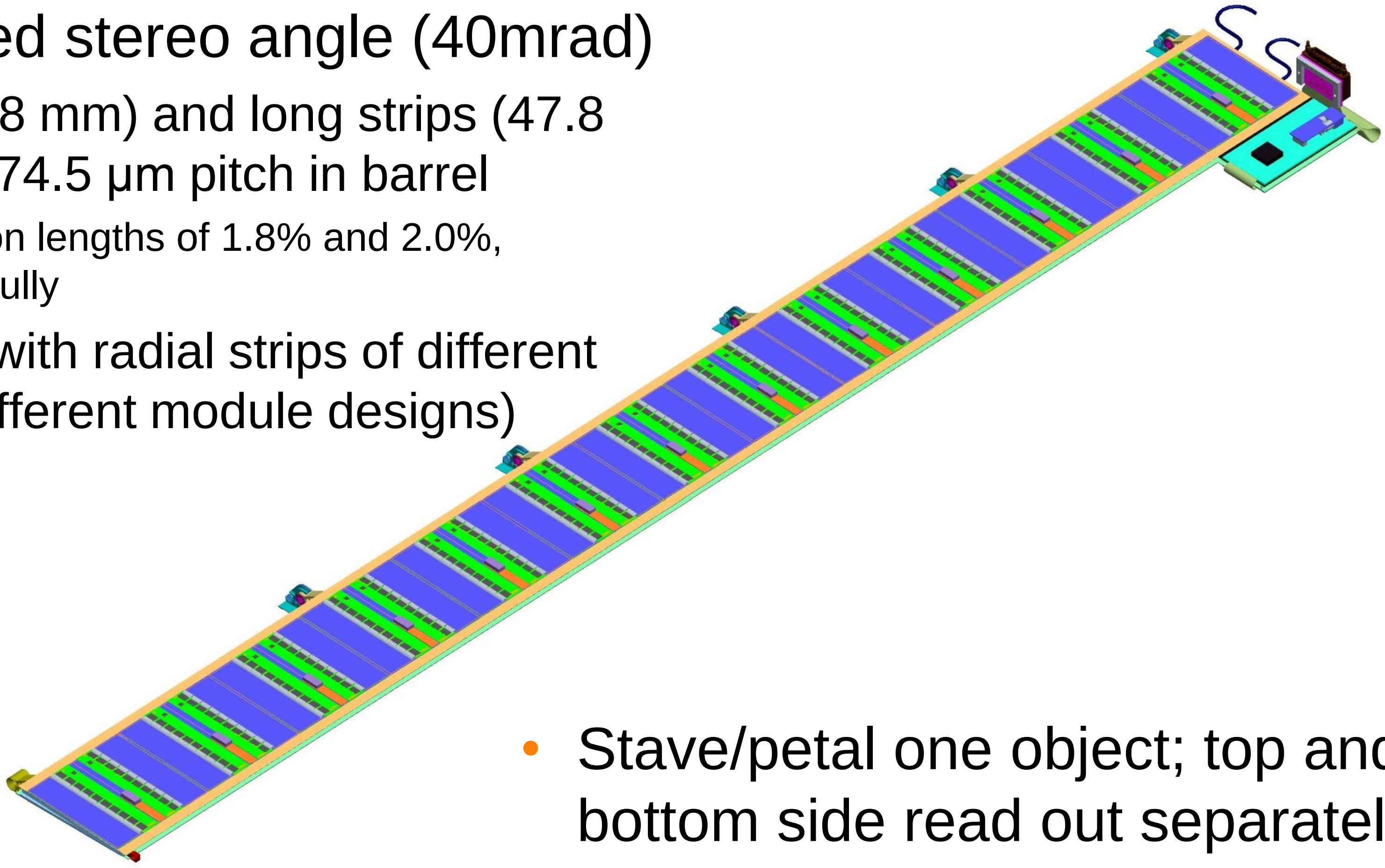






Staves

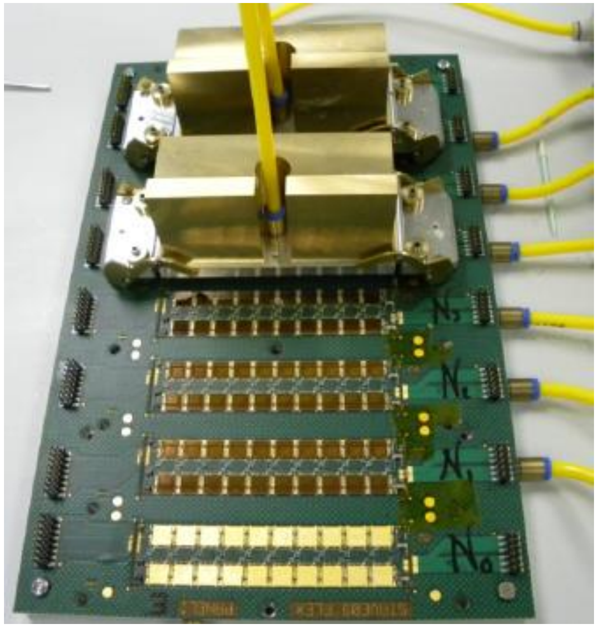
- Double-sided layers with implemented stereo angle (40mrad)
  - Short (23.8 mm) and long strips (47.8 mm) with 74.5 µm pitch in barrel
    - Radiation lengths of 1.8% and 2.0%, respectfully
  - End-Cap with radial strips of different pitch (6 different module designs)



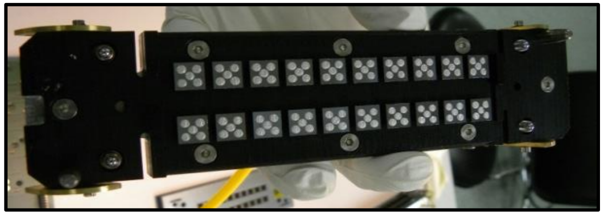
- Stave/petal one object; top and bottom side read out separately
  - not suited for self-seeded trigger

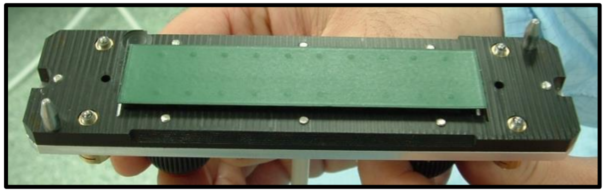
Hybrid Mass Production

- Hybrids built in panels (8 in each):
  - Flex selectively laminated to FR4
    - FR4 acts as temporary substrate during assembly, wire bonding and testing
  - Designed for machine placement and solder re-flow of passive components
  - Mass attachment/wire bonding of custom ASICs
  - Mil-spec test tokens for monitor metalization and via quality throughout production
- Flex uses conservative design rules (~20000 hybrids to be installed):
  - ↳ High yield, large volume, low price
    - 100µm track and gap, blind vias (375µm lands with 150µm drill) and 50µm dielectrics
- Hybrids+ASICs tested in panel
  - With final ASIC set (ABCn-130nm, HCC, power), all hybrids in the panel tested with one data I/O and one power connection



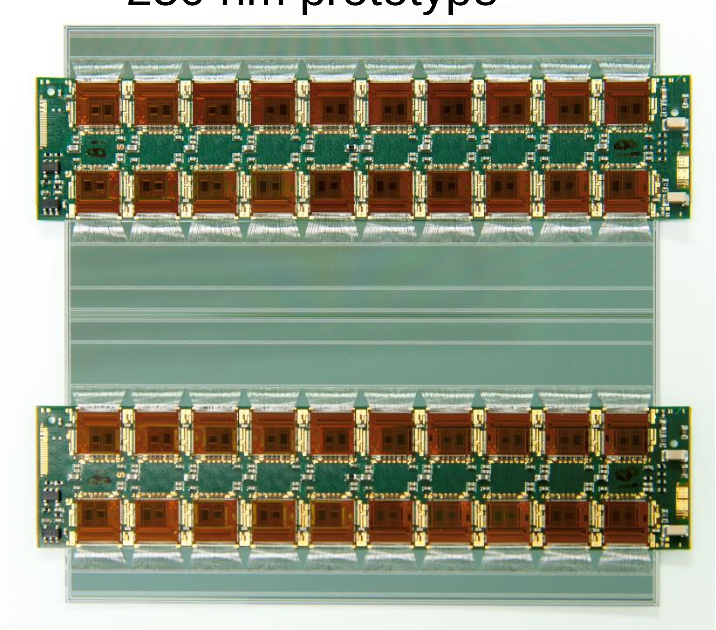
Panel dimensions: 300mm x 200mm
Hybrid dimensions: 24mm x 107.6mm



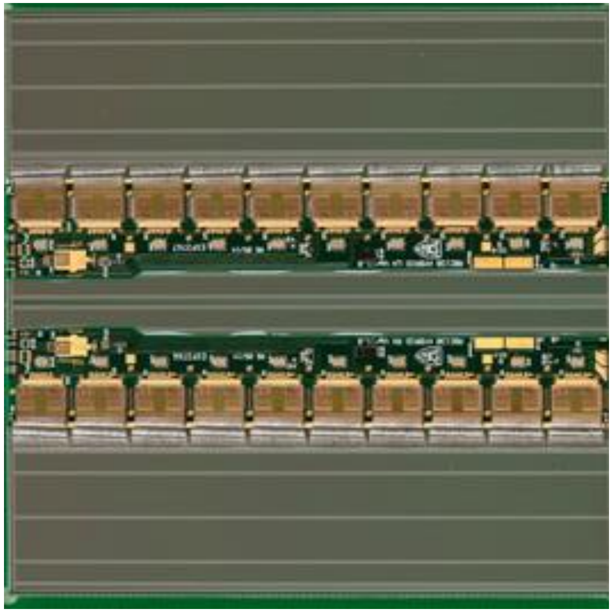


Module Design

250 nm prototype



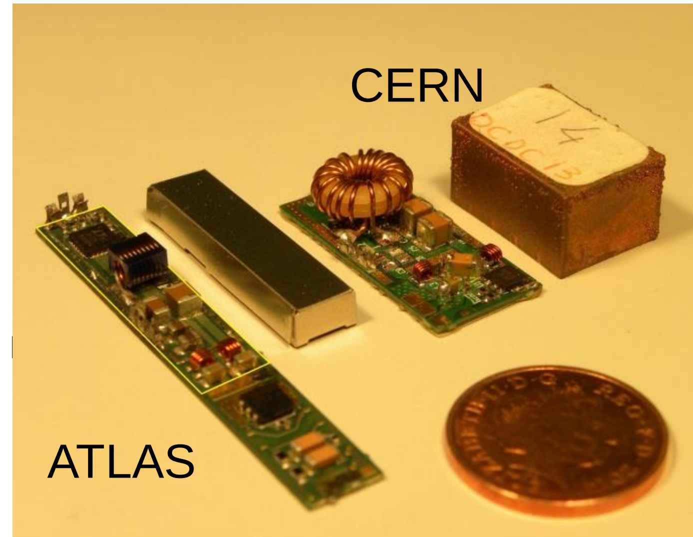
130 nm prototype

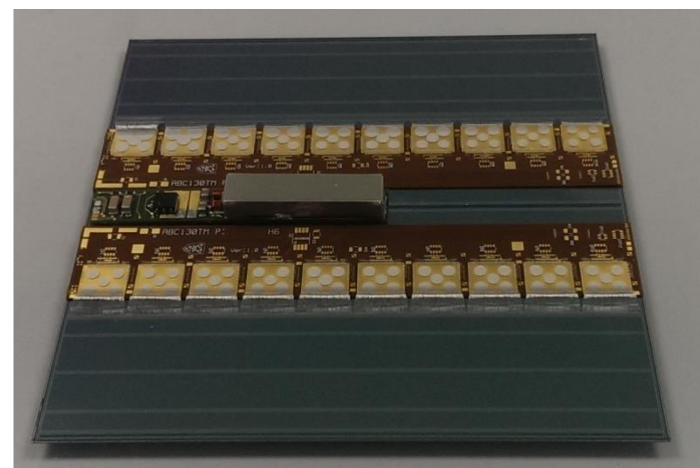


- Collaborative effort between sensor, ASIC, and hybrid designers important
  - Reduced material by 40%, hybrid bonding times by ~60%, module bonding times by ~30%
- Reduced estimated production time by ~1 year

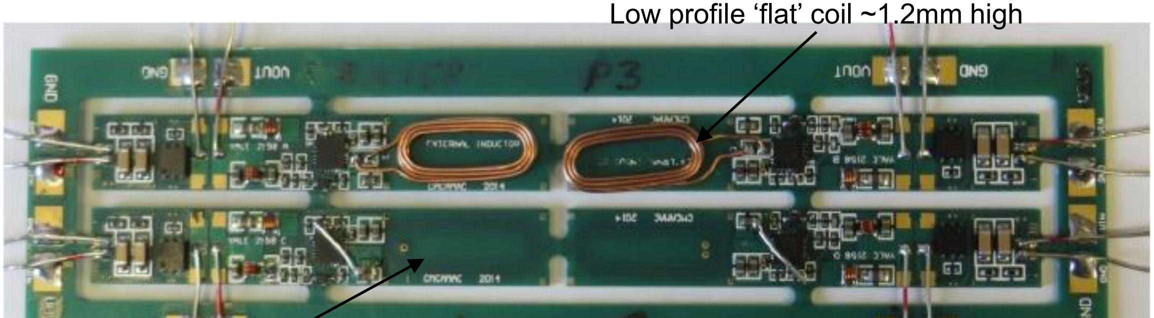
Module Powering

- Baseline powering choices are serial powering for pixels (ATLAS) and DC-DC for the strips.
  - DC-DC base layout and FEAST ASICs provided by CERN PH-ESE
- We have since optimized material use by shrinking packaging (from 0.1% to ~0.05% X_0 per module)
  - Custom flat coils are important to reduce height which drives clearances within a layer
- Also have shown that they can operate on sensor with no noise effect.
  - Single testable object with no additional material





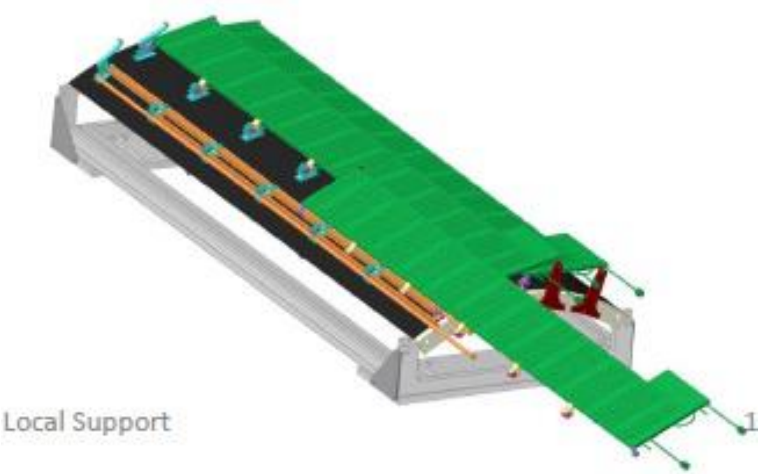
Low profile ‘flat’ coil ~1.2mm high

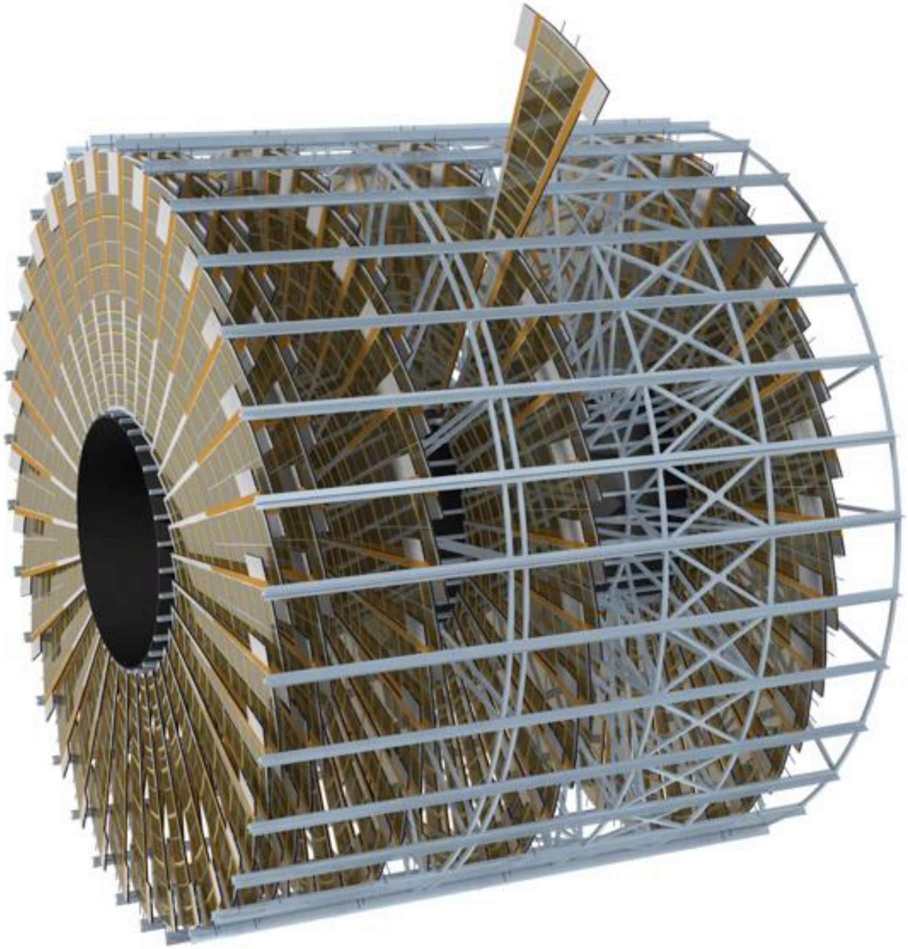


Embedded coil

Assembly Sequence

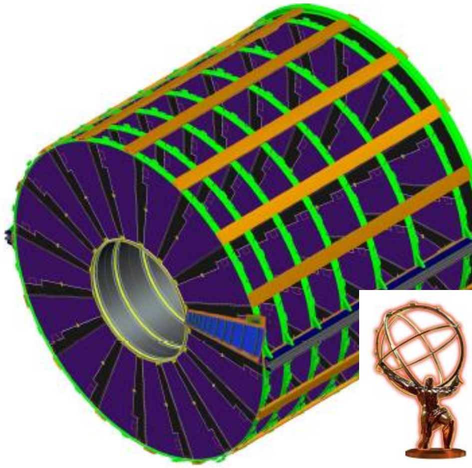
- Stave and petals designed to end insert
  - Larger global structures/testing earlier in the build
- Stave/petals also require systems-like test for burn-in early in cycle
  - Larger scale info early in build process

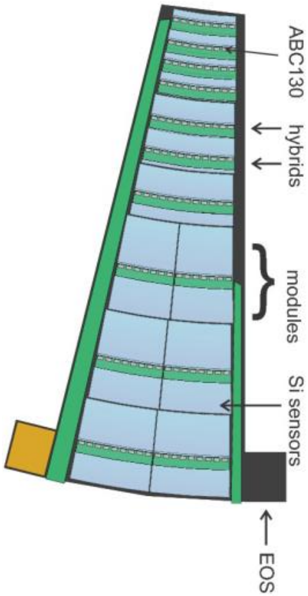


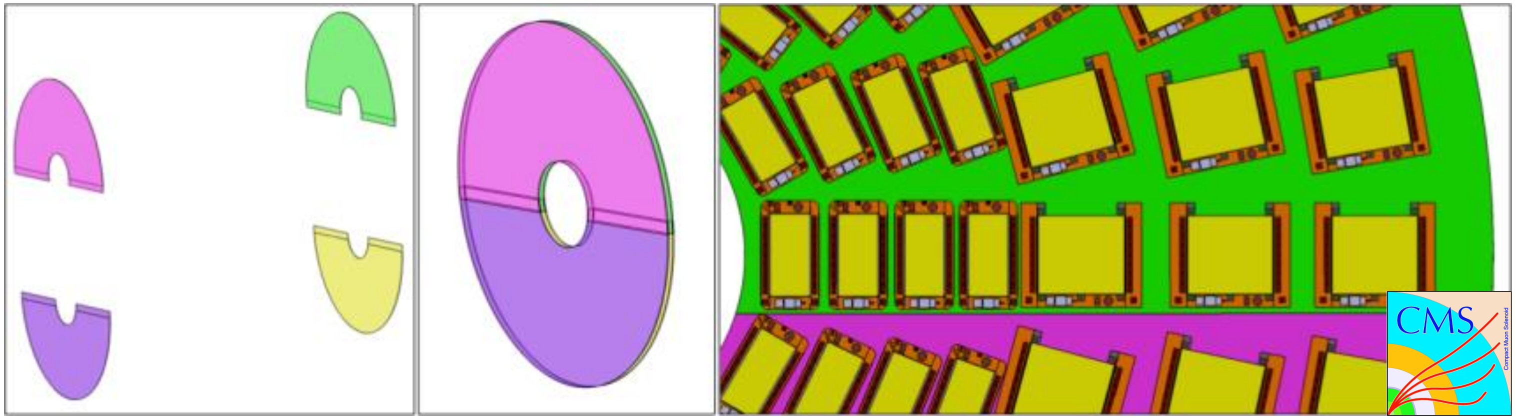


End Cap Concepts

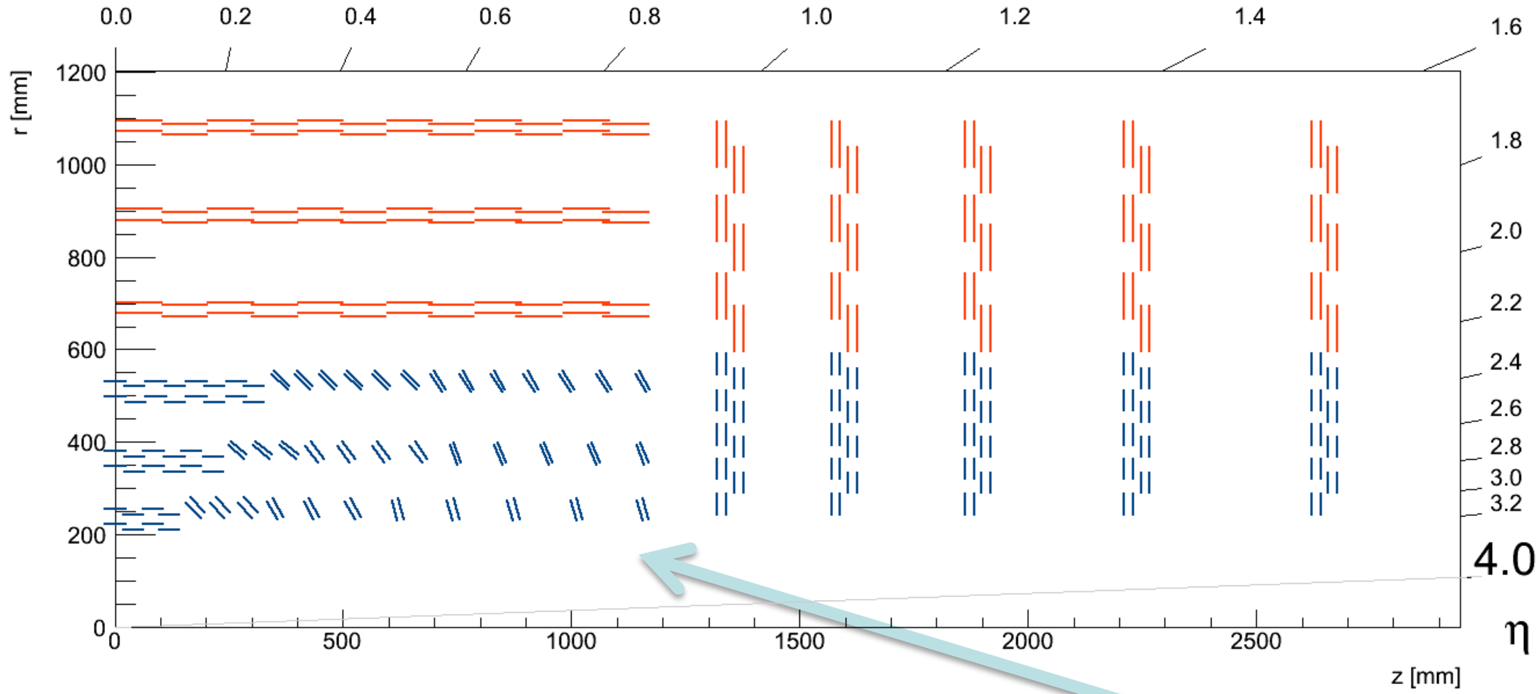
- Very different concepts
  - CMS: Rectangular modules (same as barrel) tiled on 4 surfaces on two large disks, each made of 2 dees.
  - ATLAS: Trapezoidal modules glued onto petals (32 petals in a disk). Inserted into larger global structure
- Two experiments effectively switched basic concepts
  - Suggests end caps are hard
  - Can either minimize module types or material overlaps
  - Can either minimize material in big supports or have easier (smaller) items to build/install/repair

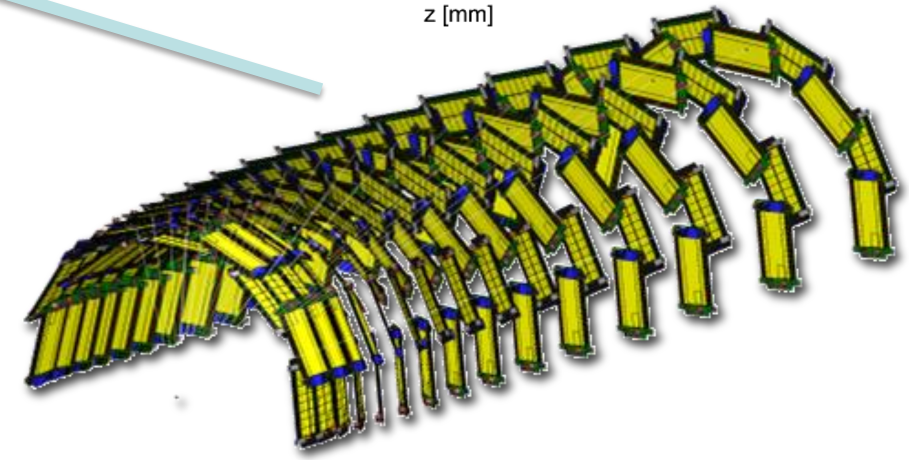






Beyond baseline?

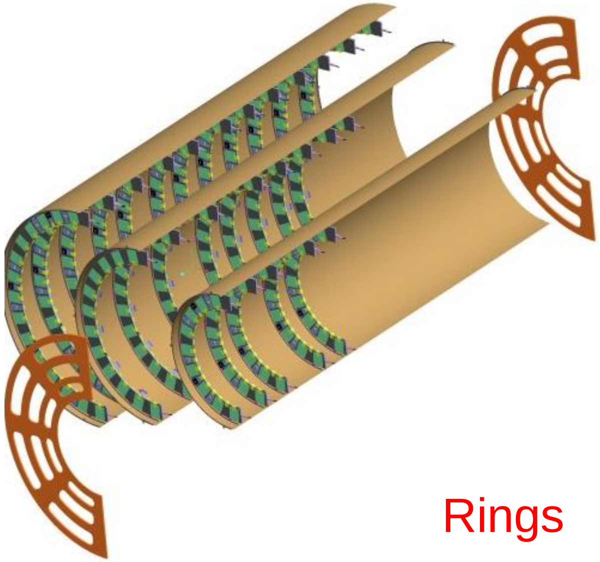


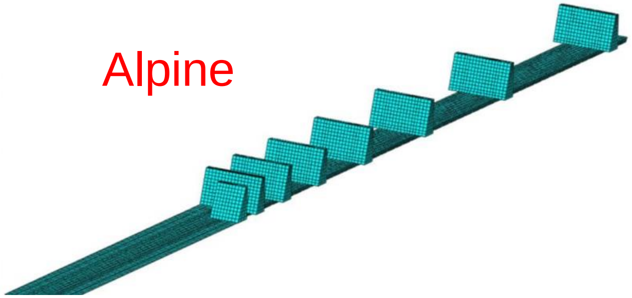


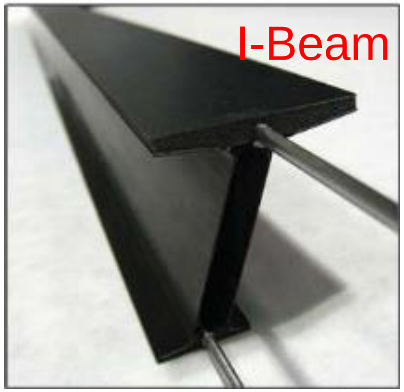
- Variant of BPS with progressively tilted modules
- Short central section followed by groups of rings with same tilt
- Same coverage and ~same tracking performance with a smaller number of modules

Pixel mechanical Structures

- Many different carbon fibre structures under consideration
  - Less silicon for same coverage
  - Move flexibility in layout optimization
  - More stiffness for same material

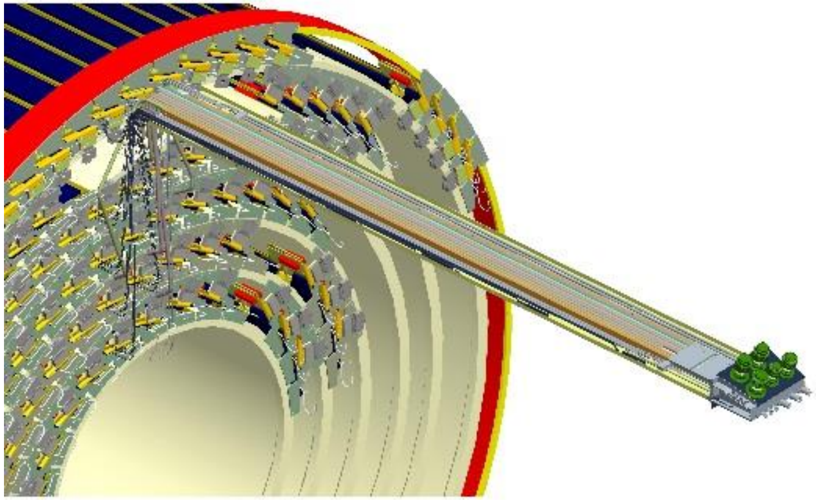






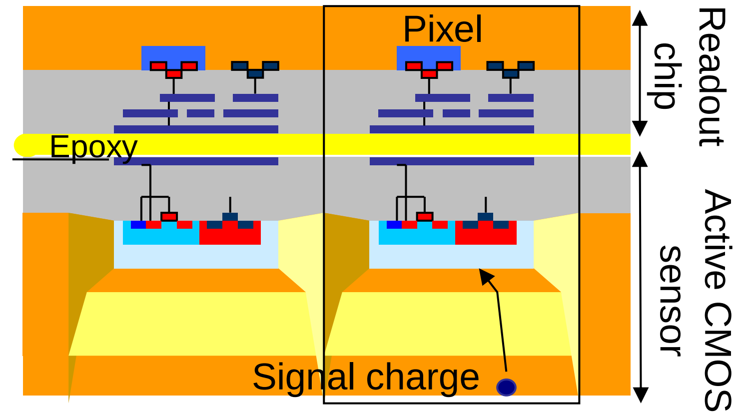
Services

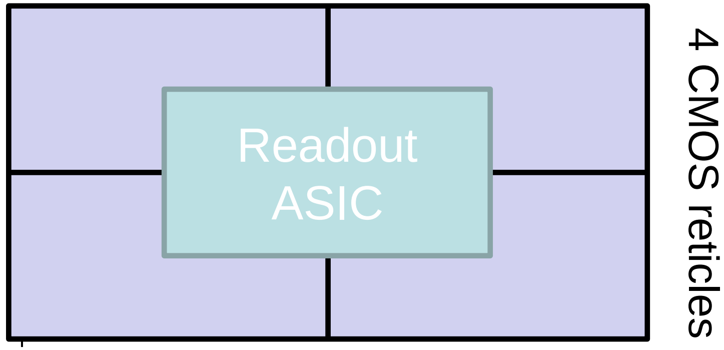
- Services was a major source of material in current trackers
  - Dominate source of faulty modules
- Manifolding and multiplexing service key for material reductions
- ATLAS using service modules which can pre-assembled and tested extensively
  - Reliability is extreme important due to manifolding/multiplexing
  - LV voltage and cooling choices drive the material budget.

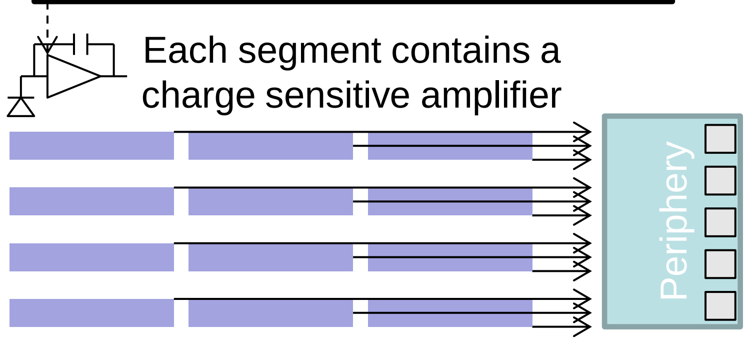


Active CMOS Sensors

- Three variants of active CMOS sensor R&D underway due to potential cost savings and performance gains. All have separate readout ASICs.
  - Pixels: one-to-one matching between ASICs and sensor. Capacitive coupling possible.
  - Macro-pixels: metal layers are used to route larger pixels into standard pixel ASIC
  - Strips: segments are bought to periphery circuit. Periphery designed to have less than ½ wire bonds than standard modules

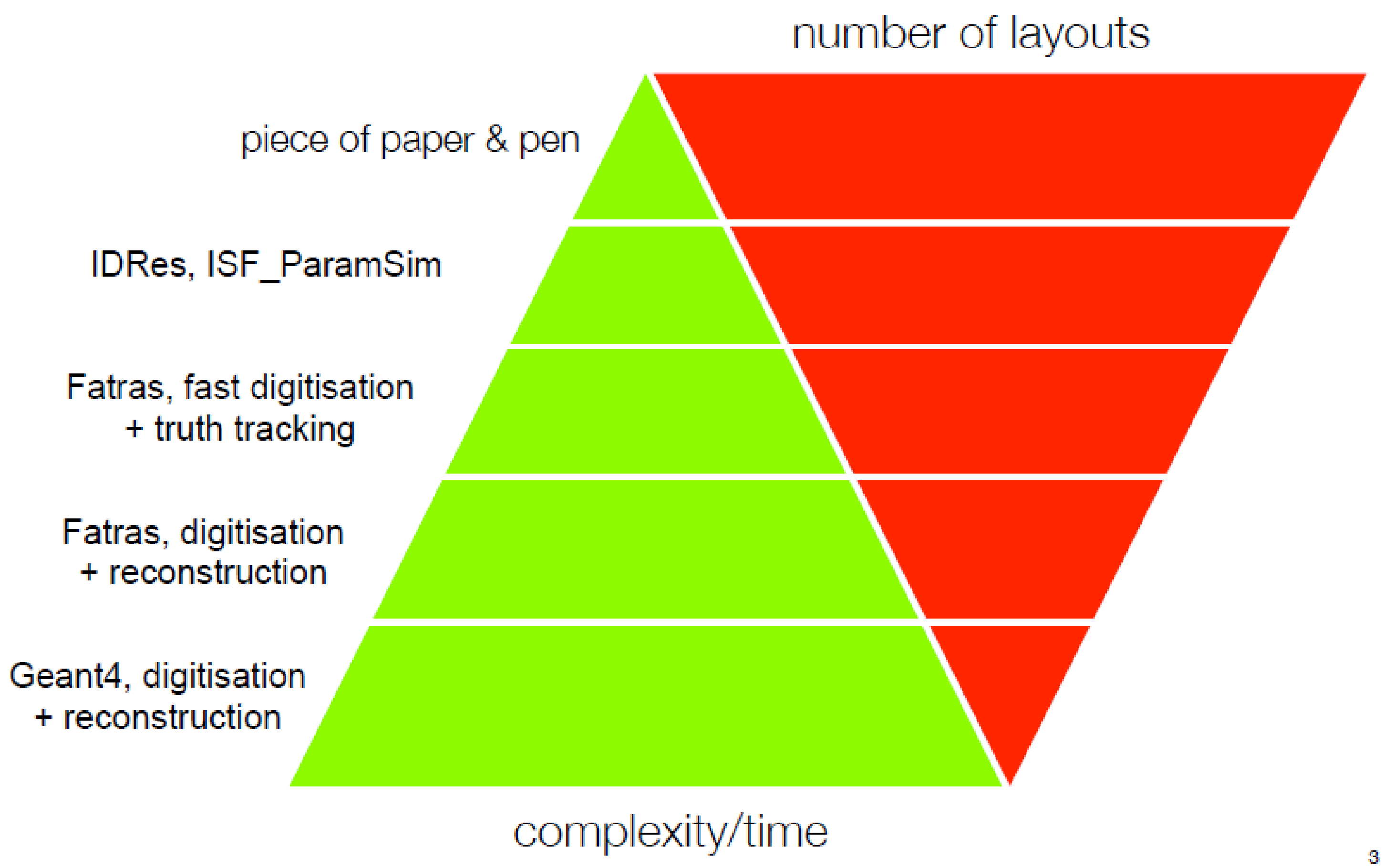






Conclusion

- A great deal of R&D pursued for the HL-LHC tracker upgrade
  - Development is still needed in many areas
- The basic “rules” for building a larger tracker (~100s m^2) are applicable anywhere
  - Need to think of industrialization, scaling, producibility and rates
  - Services and powering are often overlooked
- A few baseline technologies are direct relevant
  - C4 bumping, thin kaptons, DC-DC converters, co-curing, ALCF, CF
- Many concepts not fully realized could easily find a home at CLIC
  - CMOS active sensors, various mechanical concepts


number of layouts
piece of paper & pen
IDRes, ISF_ParamSim
Fatras, fast digitisation
+ truth tracking
Fatras, digitisation
+ reconstruction
Geant4, digitisation
+ reconstruction
complexity/time
3

Tool Matrix

Tool	material maps	inactive/noisy channels	inactive modules	alignment studies	pile-up studies					
piece of paper & pen	-	-	-	-	-					
IDRes	-	-	-	-	-					
Fatras, fast digitisation + truth tracking	<5%	-	+	o	-					
Fatras, digitisation + reconstruction	<5%	+	+	+	+					
Geant4, digitisation + reconstruction	+	+	+	+	+					

Performance Matrix
(guesstimates & achievements)

	hit coverage	resolution (singleP)	efficiency (singleP)	resolution (jets)	efficiency (jets)	fake rate	vertexing res.	vertexing fakes	vertexing eff.	btagging
piece of paper & pen	5%	10%	-	15%	-	-	-	-	-	-
IDRes	2%	10%	-	15%	-	-	-	-	-	-
Fatras, fast digitisation + truth tracking	+	<5%	<5%	5%	5%	<5%	<1%	<1%	<1%	15%
Fatras, digitisation + reconstruction	+	~1%	+	<5%	<5%	+	+	+	+	<10%
Geant4, digitisation + reconstruction	+	+	+	+	+	+	+	+	+	+