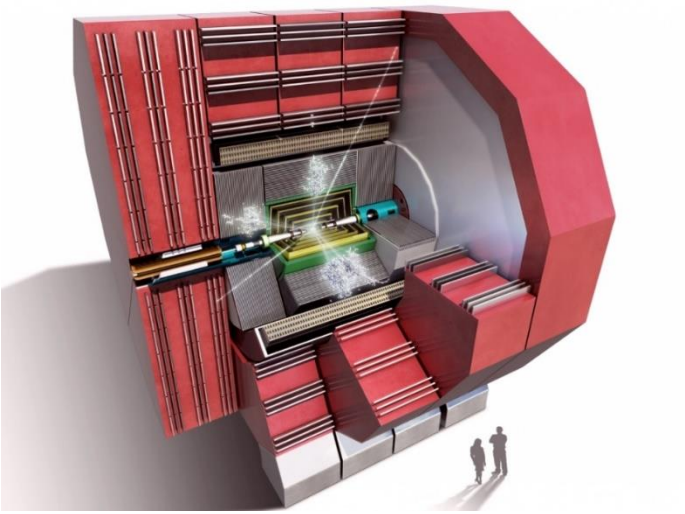
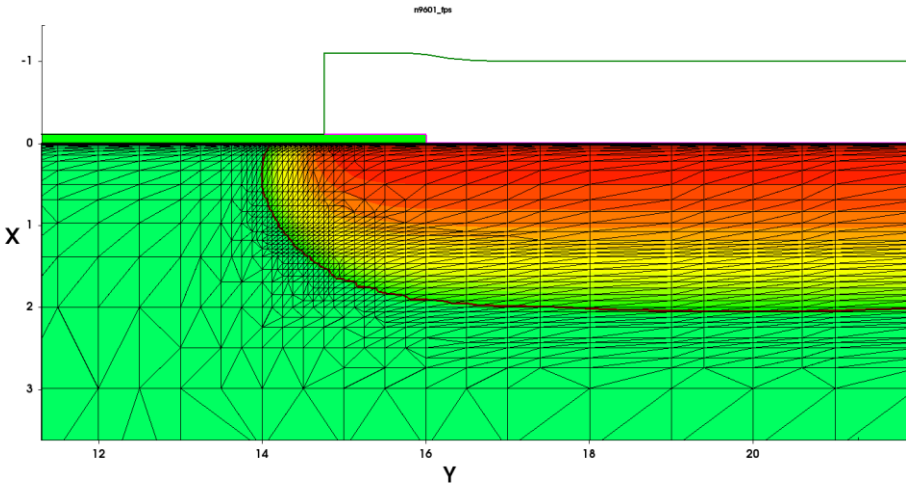
HV-CMOS Simulation

Matthew Buckland
University of Liverpool
CERN

Outline

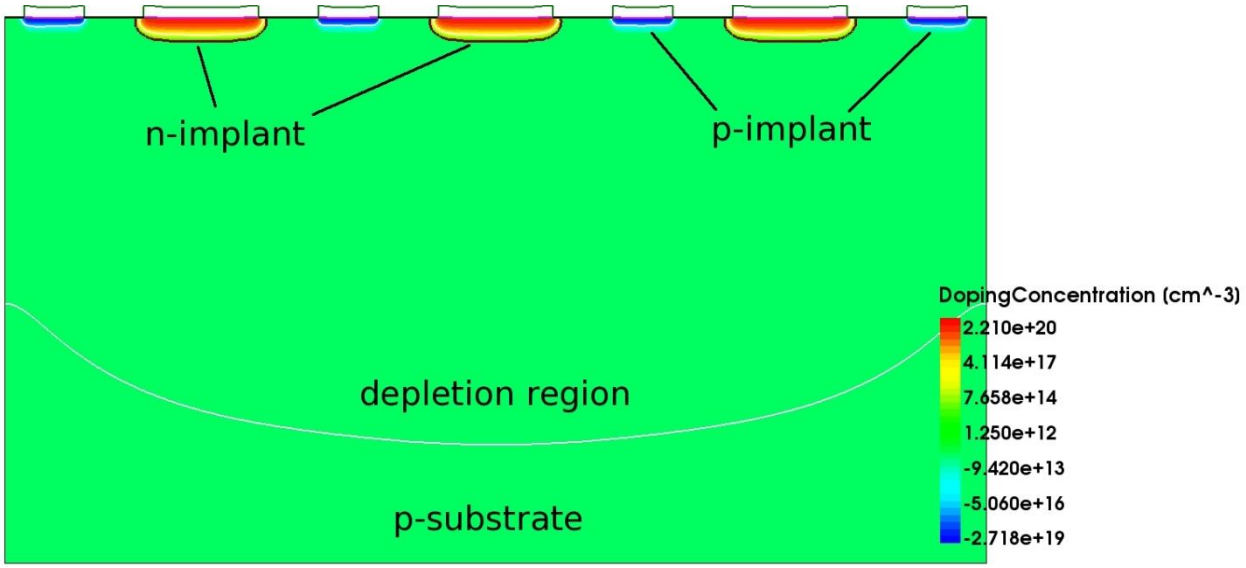
- TCAD
- The study of two biasing schemes
- HV-CMOS submission/reticle edge study
- Summary





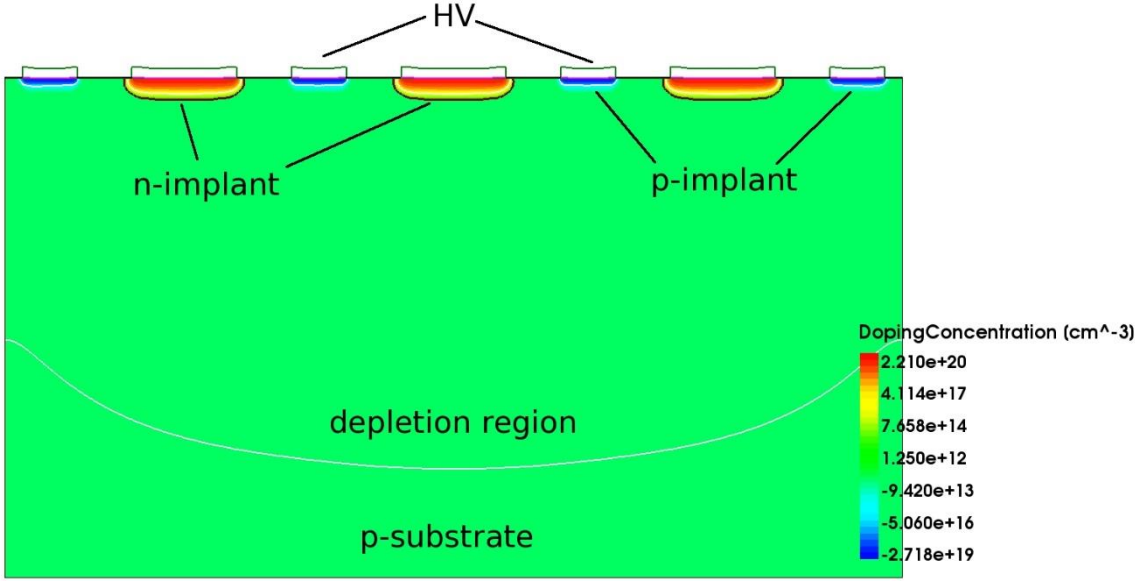
TCAD

- Computer simulations for semiconductor devices
- Simple diode, n-in-p device
- 3 diode array, (90x50)μm
- Resistivity = 1000Ωcm
- Implant doping $1x10^{20}cm^{-3}$
- Full RD50 radiation model
- Bias = -60V

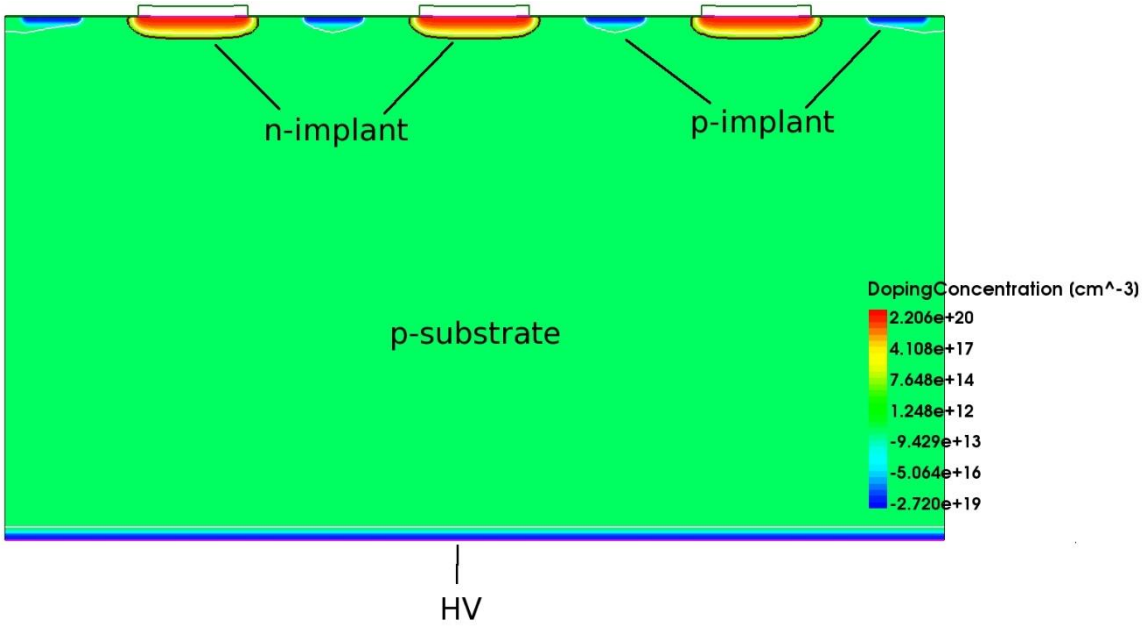


The Two Bias Schemes compared

- HV top

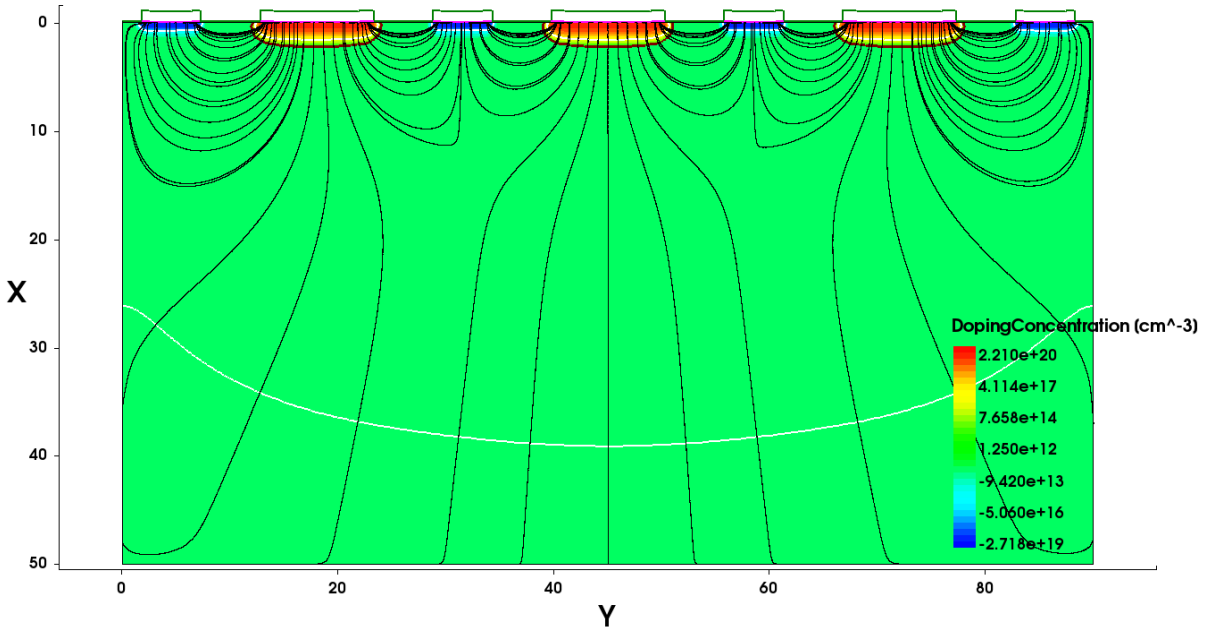


- HV back (p-implants floating)
- Full depletion at -60V (50µm thickness)

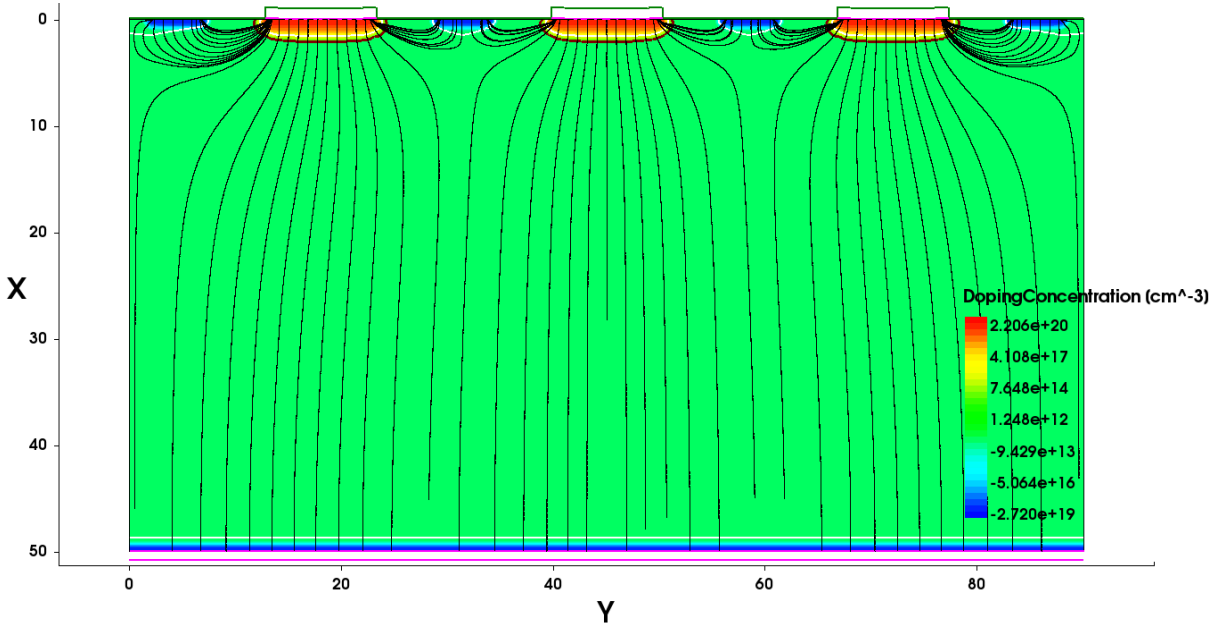


E-field Lines Comparison

- HV top

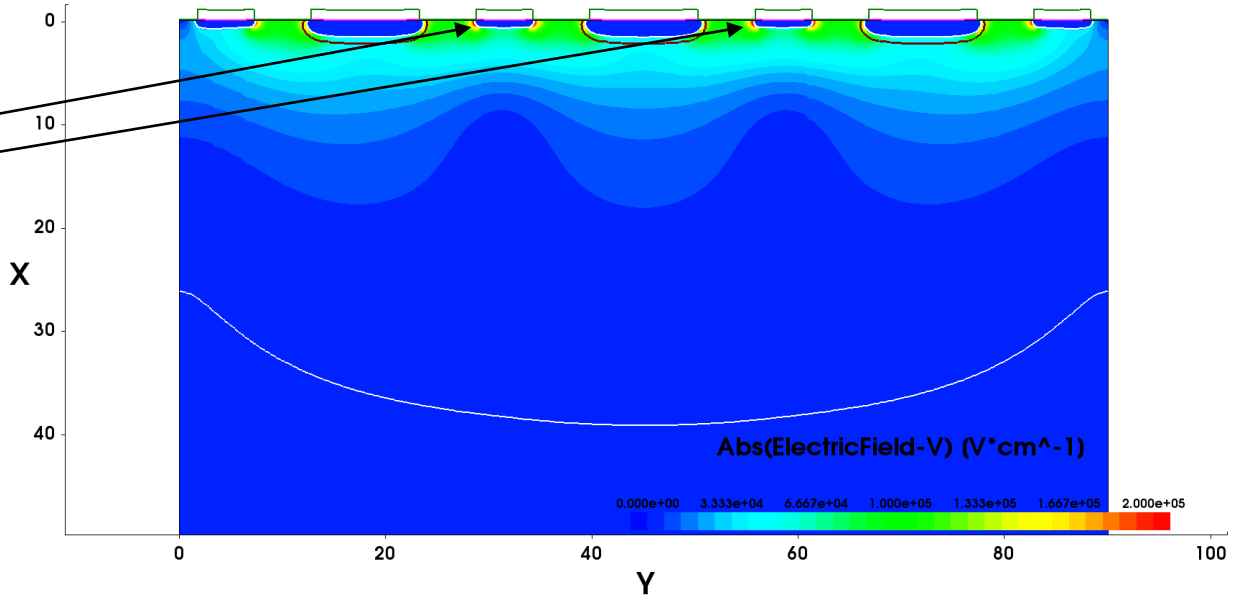


- HV back
- More uniform field

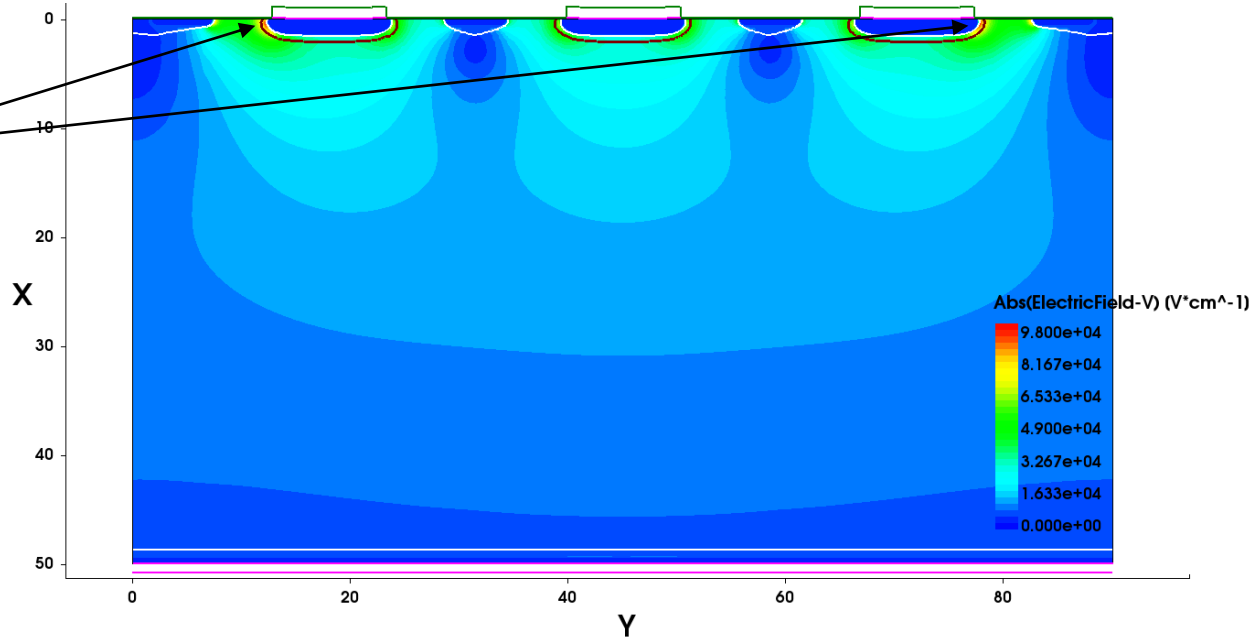


E-field Value Comparison

- HV top
- High field regions
- Value 2×10^5 V/cm

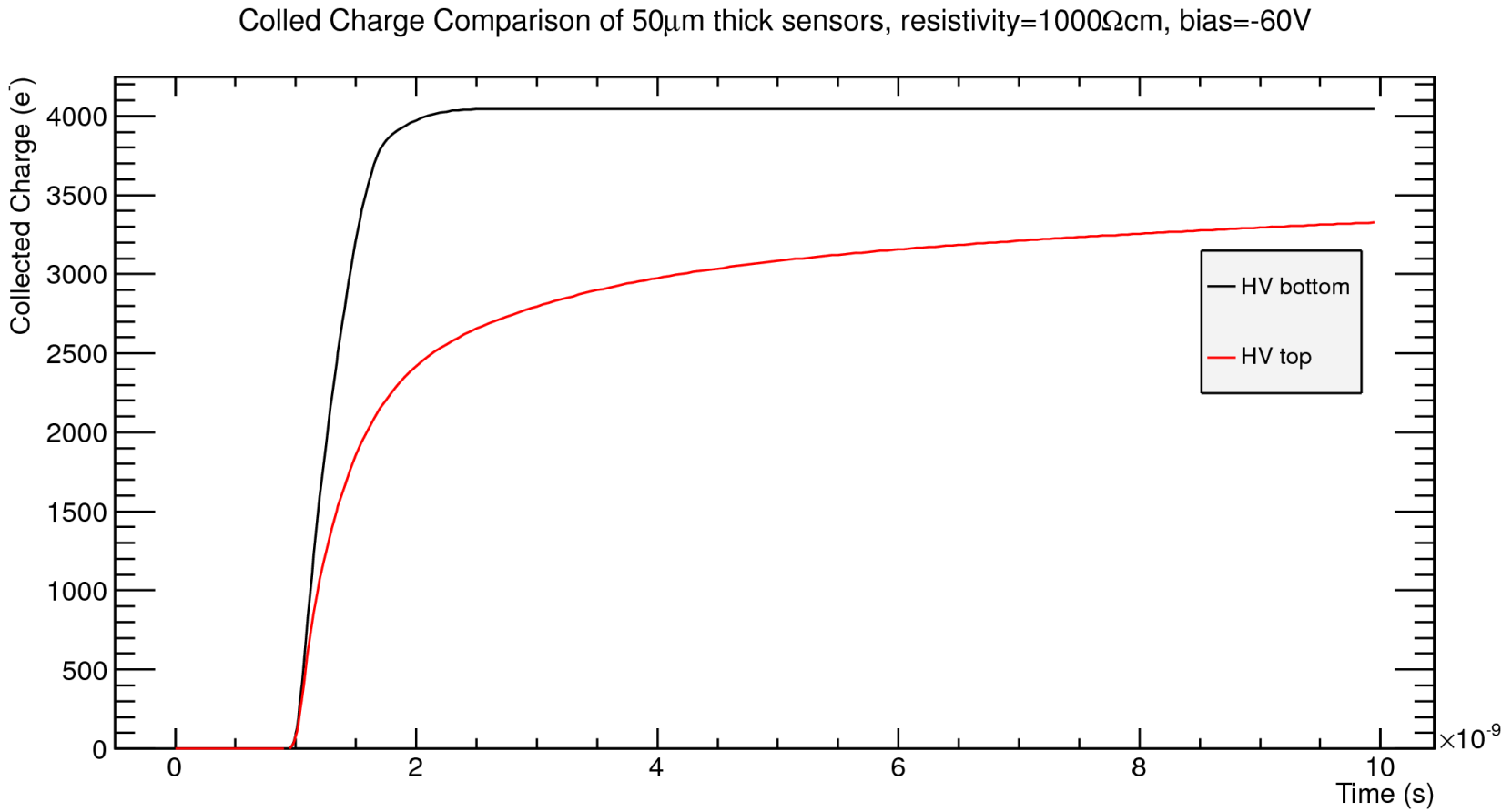


- HV back
- High field regions
- Value 9.8×10^4 V/cm
- Lower field value
- Deeper field

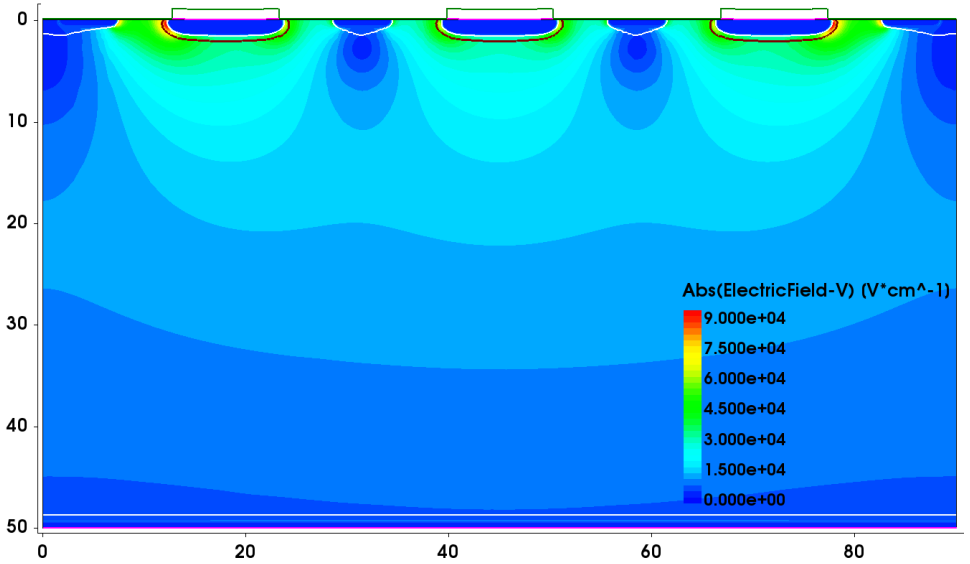


Charge Collection Comparison

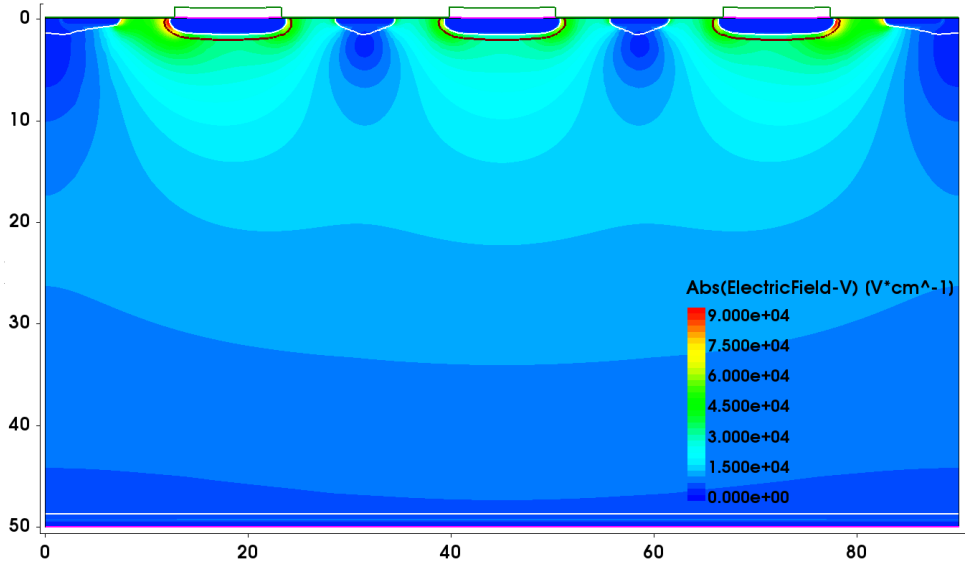
- Mip enters at 1ns at width of 45µm, 80eh pairs per µm
- Deposits total charge of 4000e^-
- Back bias full charge collection at 2ns compared to ≈60% for HV top



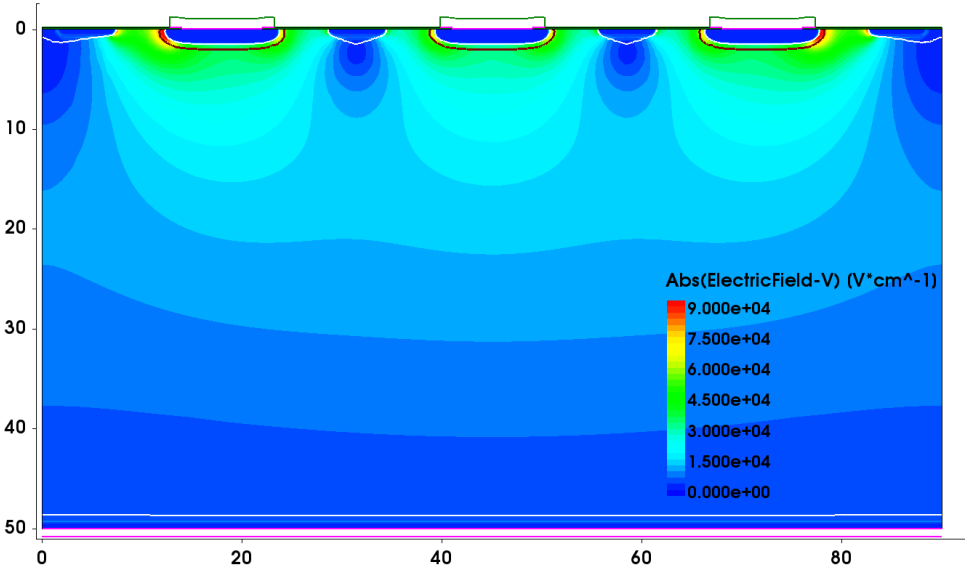
E-field with Radiation



- $\Phi_{eq}=1x10^{13}cm^{-2}$ (CLIC)



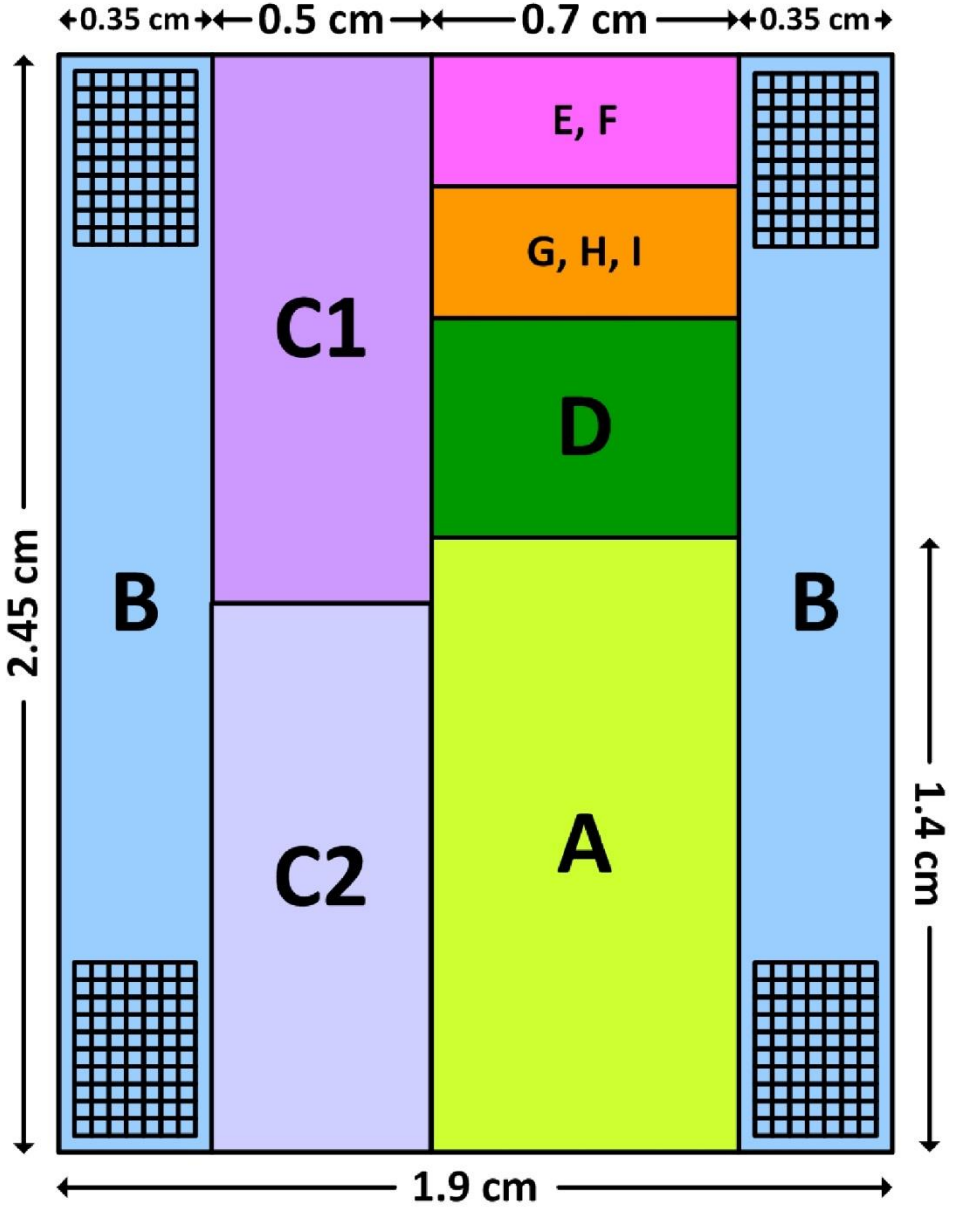
- $\Phi_{eq}=1x10^{14}cm^{-2}$



- $\Phi_{eq}=1x10^{15}cm^{-2}$

Floorplan

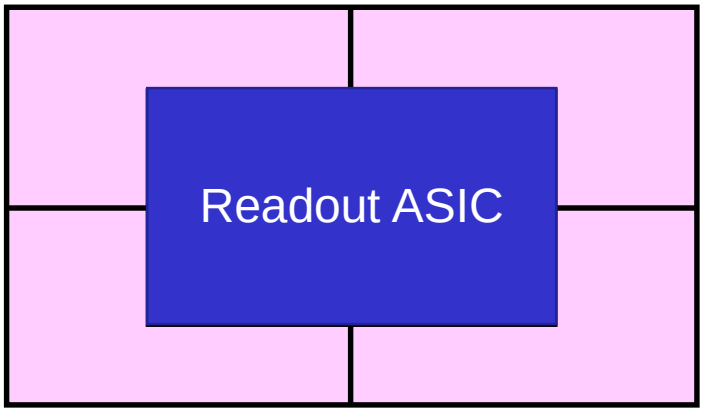
- Planned AMS350 submission (Liverpool, Geneva, KIT, Bern)
- Section B
  - Dedicated part to test fan out structure in metal layers
  - Macro pixels with pixel readout
- Read larger area sensor with single pixel ASIC



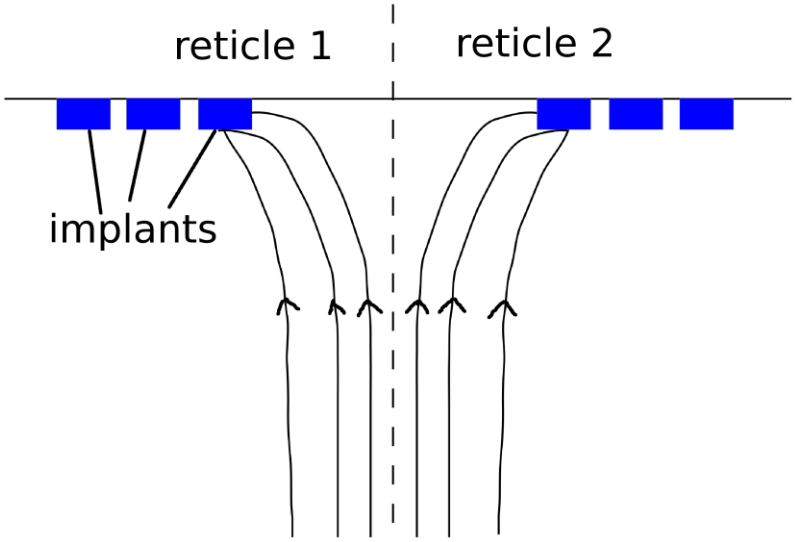
*E.Figueras. Engineering run with 0.35*µm CMOS HV from AMS. Floorplan.

E-field at Edges of Reticles

- Test possibility of using undiced sensor
  - If one to one ASIC sensor still easier tilling
  - Or use macro pixel sensors (multi-reticle) with one ASIC
- Need TCAD study for charge collection at the reticle edges
  - Look at design rules in this region
  - Optimise design for best charge collection



4 CMOS reticles, 1 ASIC



Summary and Future Work

- Study of top vs. back bias
  - Full depletion at lower bias for HV back
  - More uniform fields
  - Lower value high field region
- Want to study the possibility of undiced sensors (either easier tiling or macro pixel assemblies)
  - TCAD study of signal collection at the edge