

# HVCMOS for the ATLAS Experiment

Mathieu Benoit

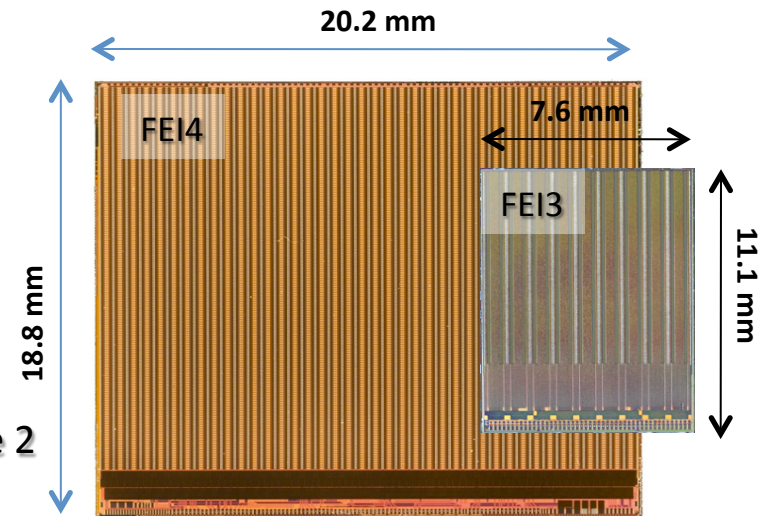
# Outline

- Presentation of CCPD sensor family
  - CCPDv2
  - CCPDv3
  - CCPDv4
  - AMS H350 CAPSENS
- Test beam and characterization of the CCPDv2 coupled to the FEI4
- Toy TCAD Simulation of the observed effects

# Front-end Electronics – FEI4

## FEI4 main features:

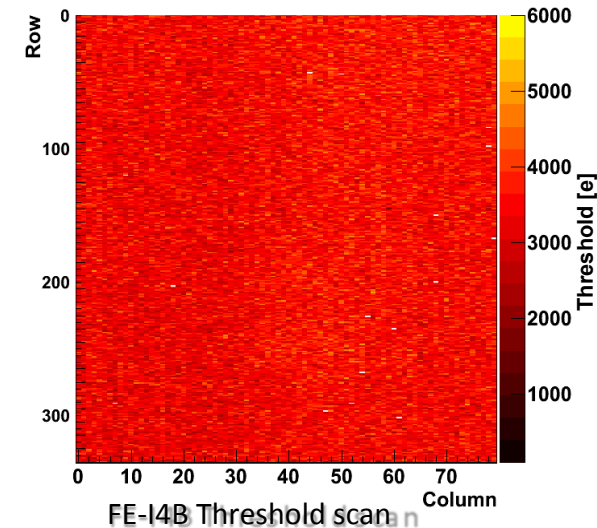
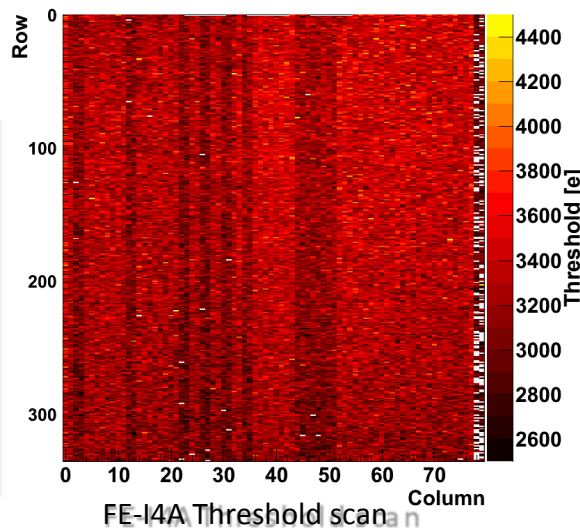
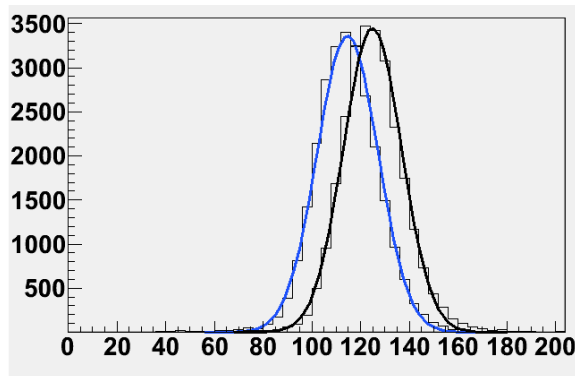
- IBM (130 nm)
- 70 Million transistors
- 26880 pixels ( $50 \times 250 \mu\text{m}^2$ )
- Lower noise than FE-I3 ( $\sim 150\text{e}^-$  with sensor)
- Lower threshold operation
- Higher rate compatibility
- Radiation hard to  $>250\text{Mrad}$
- In use for pixel R&D and towards Upgrade phase 2



## Through the FEI4 progresses:

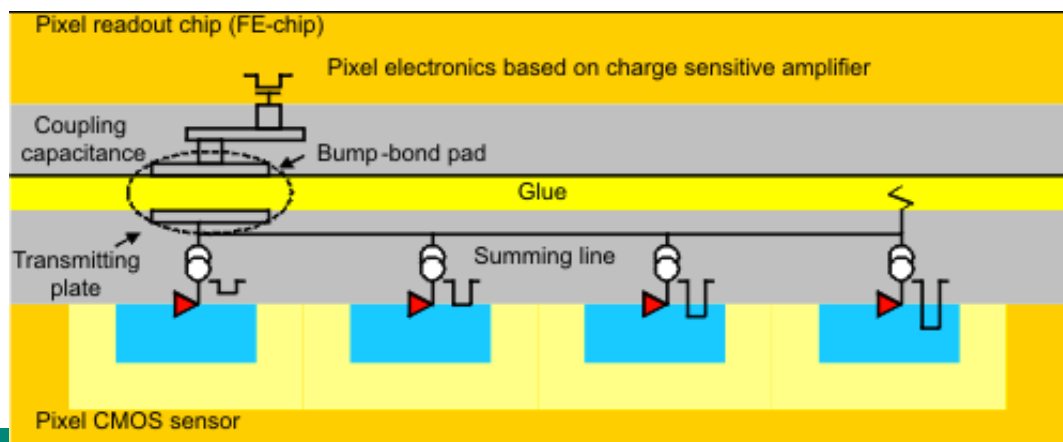
- First version FEI4a for validation and IBL prototypes (32 FE-I4A wafers received in 2010/11)
- FEI4b features: minor fixes + r/o functionalities + uniform pixel matrix + Power functionality
- First FEI4b delivery in Dec. 2011
- FEI4b now in production (30 wafers) and wafer probing is almost completed (yield  $\sim 60\%$ )

**FEI4b noise before and after irradiation:  
114e  $\rightarrow$  124e (both tuned)**



# Capacitively-Coupled Sensors for ATLAS

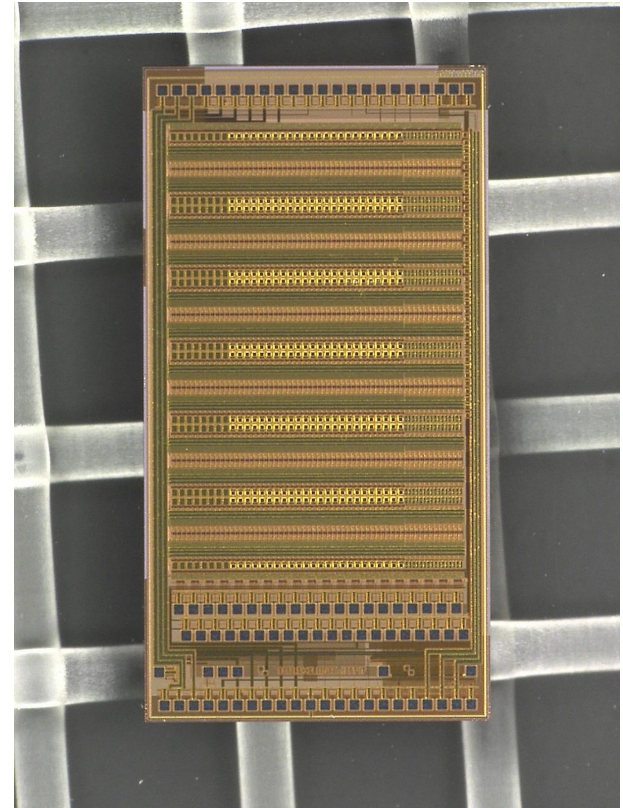
- The ATLAS experiment is planning for an upgrade of its inner detector for operation at High-Luminosity
  - Large area of pixel detectors are needed to cope with the increased occupancy
  - Low-cost detectors are needed to keep the price of the new Inner Tracker low
- HVCMOS processes allow for the reverse biasing of sensor diode up to  $\sim 100\text{V}$  and allow to implement CMOS circuitry inside the collecting diode (Deep N-Well)
  - Preamplifier very close to the collection node allow for large signal output  $\rightarrow$  Capacitive-coupling !
  - Replacing DC coupling using bump-bonding with AC-coupling could allow for a large cost reduction
  - Large scale production capability of HVCMOS foundries allow us to take advantage of cost scaling associated with medium to large-scale production in the industry



# The CCPD sensor family

## CCPDv2

- Chip size: 2.2mm x 4.4mm
- Pixel matrix: 60x24 (sub-)pixels of 33  $\mu\text{m}$  x 125  $\mu\text{m}$
- 21 IO pads at the lower side for CCPD operation
- 40 strip-readout pads (100  $\mu\text{m}$  pitch) at the lower side and 22 IO pads at the upper side for (virtual) strip operation
- On chip bias DACs
- Pixels contain charge sensitive amplifier, comparator and tune DAC
- Configuration via FPGA or  $\mu\text{C}$ : 4 CMOS lines (1.8V)
- 3 possible operation modes
  - standalone on test PCB
  - strip-like operation
  - pixel (FE-I4) readout

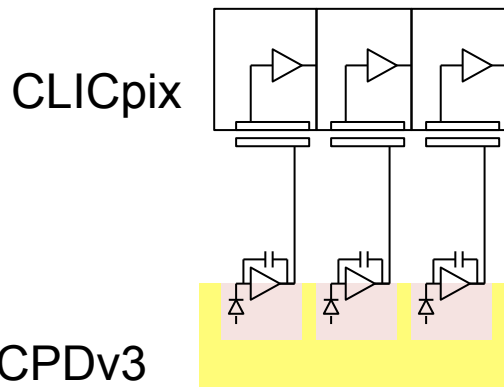
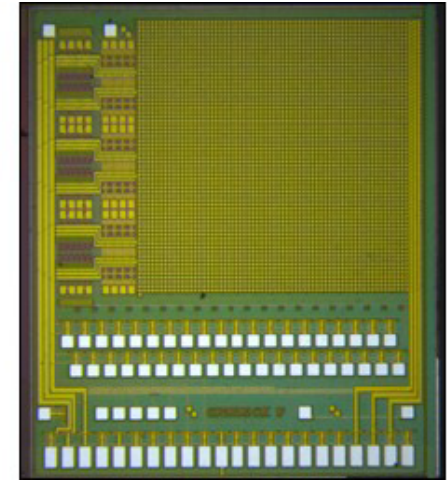


# The CCPD sensor family



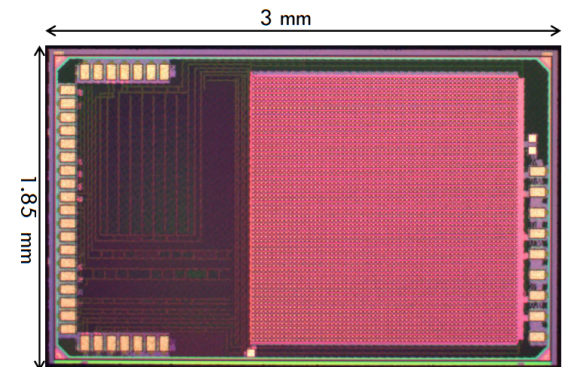
## CCPDv3

- shared with CLIC, contains amplifier-only  $25 \times 25 \mu\text{m}$  pixels and some ATLAS test pixels
- CLIC pixels matrix matching the CLICPix 65nm ASIC developed for CLIC
- Dedicated readout system developed for control and data acquisition for both ASIC



Size:  $25 \mu\text{m} \times 25 \mu\text{m}$

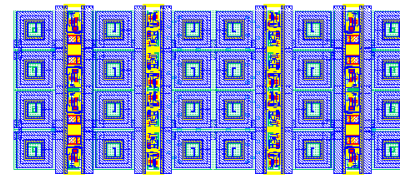
Size:  $25 \mu\text{m} \times 25 \mu\text{m}$



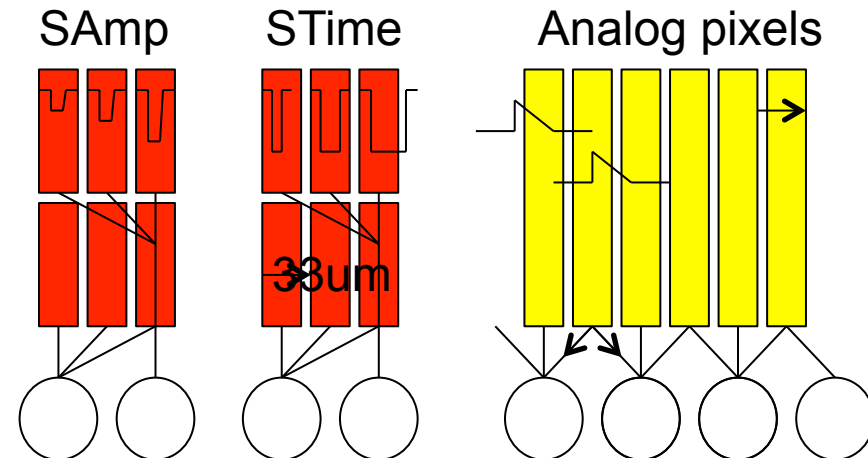
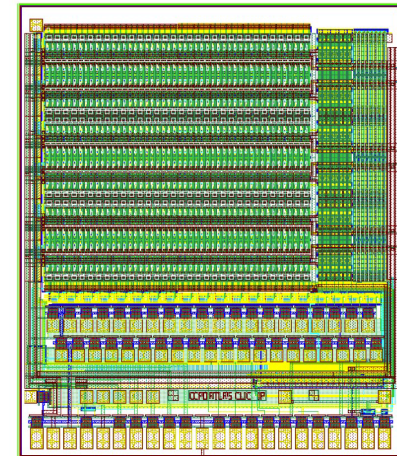
# The CCPD sensor family

## CCPDv4

- focused on ATLAS-pixel readout, several noise improvements, segmented pixels, analogue pixels
- 4 types of pixels :
  - **Samp** : Standard pixels (as in CCPDv3-1, contain comparator and tune DAC) with the current-mode amplitude coding – several improvements
  - **Stime** : Standard pixels with (new) voltage-mode amplitude coding or the pulse length coding
  - **N**: “NewPixels” – the pixels with separated electronic and electrode, sub pixel size 25um x 125um (as in CCPDv3 contain comparator and tune DAC)
  - **A**: New: Analog pixels - size 25um x 350um – contain only amplifier - electronics similar as in CLIC pixels (CCPDv3). New analog summing scheme.



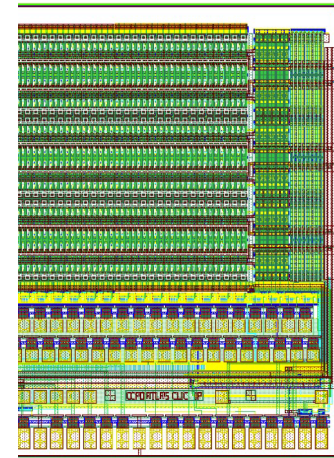
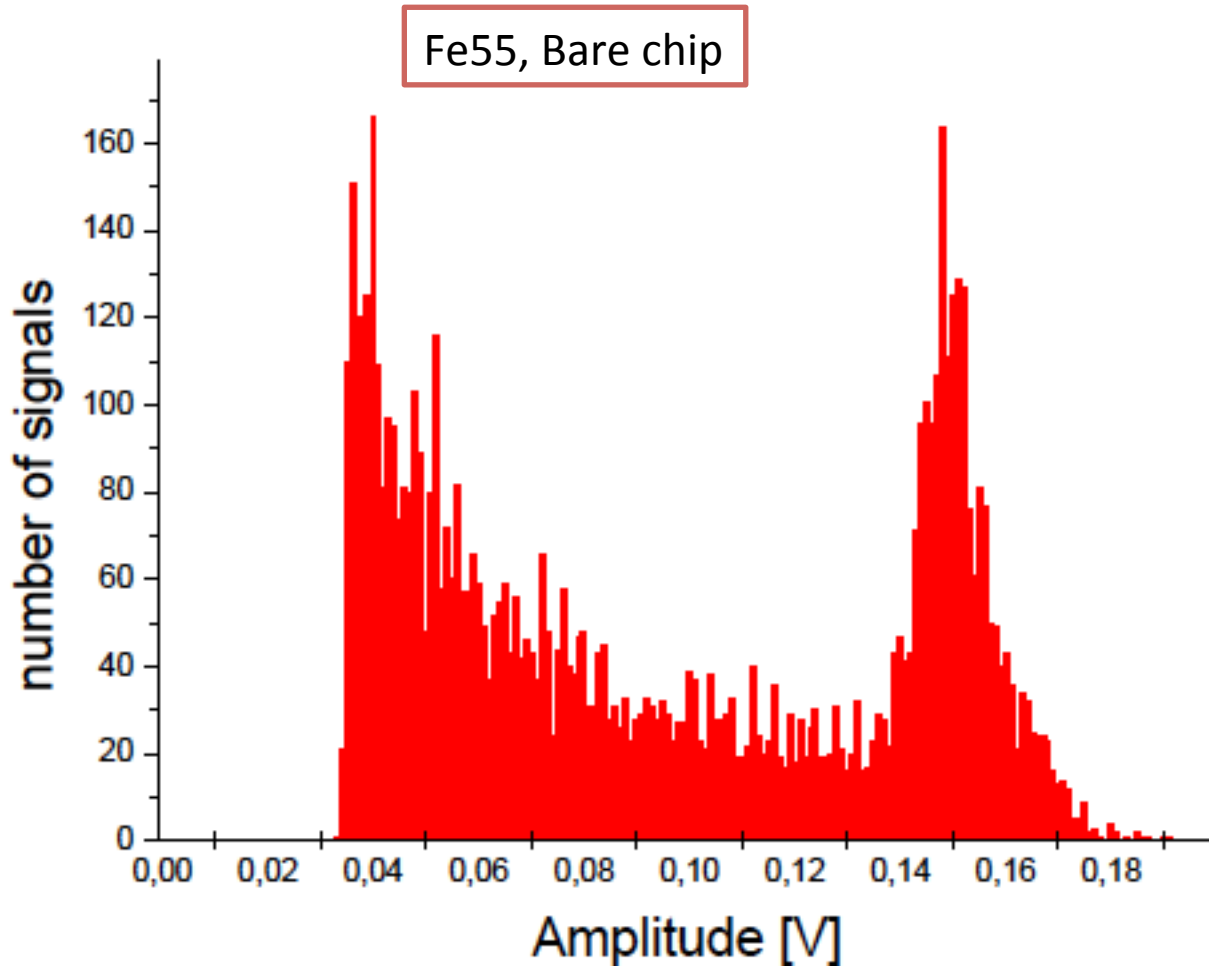
NewPixels



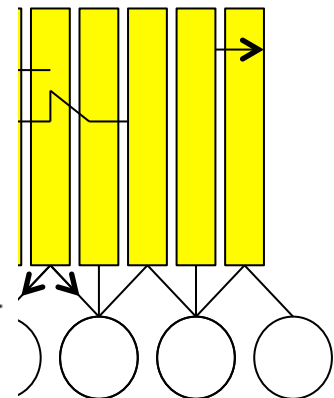
# The CCPD sensor family

## CCPDv4

- focused on A  
improvement  
pixels
- 4 types of pixels
  - Samp : S  
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  - A: New:  
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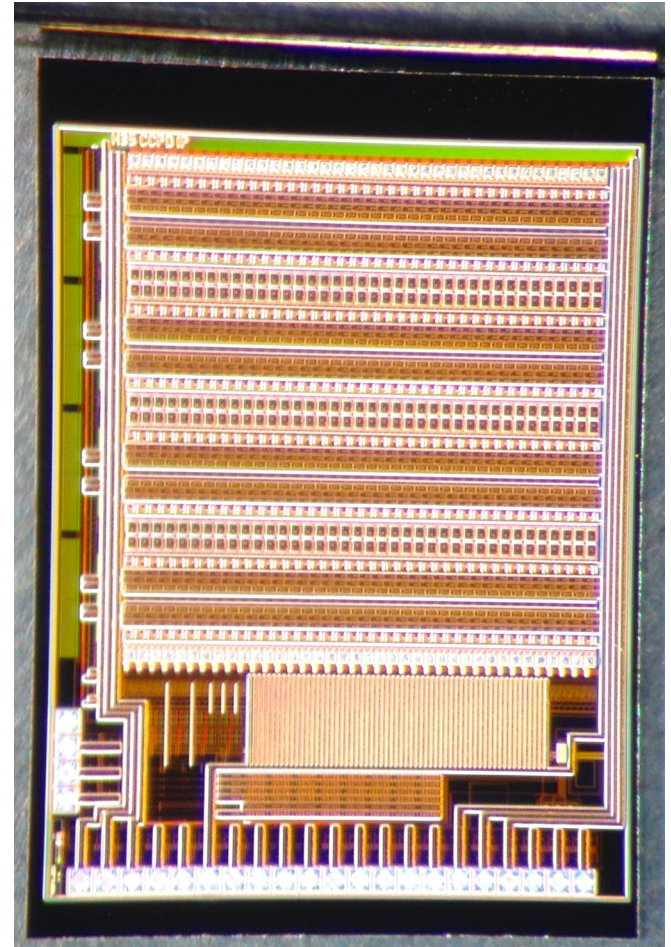
analog pixels



# The CCPD sensor family

## AMS350 new CAPSENS

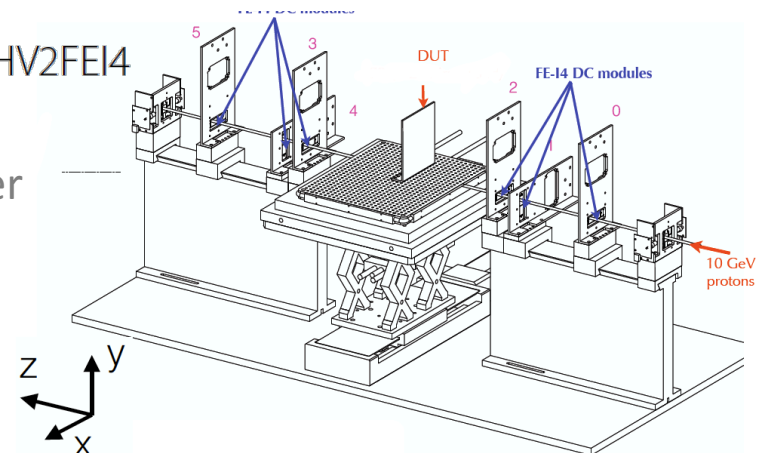
- New design in 350nm
- Compatible with v5.1 PCB (CCPDv4)
- Contains only analog pixels , no discriminator
- Software and lab setup under development



# TEST BEAM AND CHARACTERIZATION OF THE CCPDV2 COUPLED TO THE FEI4

# The FEI4 Telescope

- Telescope built primarily for characterization of HVCMOS prototypes
  - Can of course be also used for other sensors
- 6 position sensitive planes + 2 trigger planes (scintillators)
- Use existing components
  - IBL Double Chip modules + Module adapter cards
  - RCE+HSIO+Cosmics adapter card
- Pixels not square shaped
  - Alternating horizontal/vertical planes for increased resolution in long pixel direction
- Mechanics support movement of planes in z and rotations in two directions perpendicular to beam
- Synchronous read out of all FE-I4s (Telescope+DUTs)
  - No reference plane/time matching necessary
- Homebrew DCS based on Lab View
- Region of interest trigger for small devices like the current HV2FEI4
- Data reconstruction based on Judith (+ tbmon2)
- Possibility to cool DUT using our cold box and chiller
  - Monitoring of temperature and humidity in the box using DCS
  - Leakage current in HV monitored using DCS
- Calculated resolution is 8 and 12  $\mu\text{m}$  (x and Y)

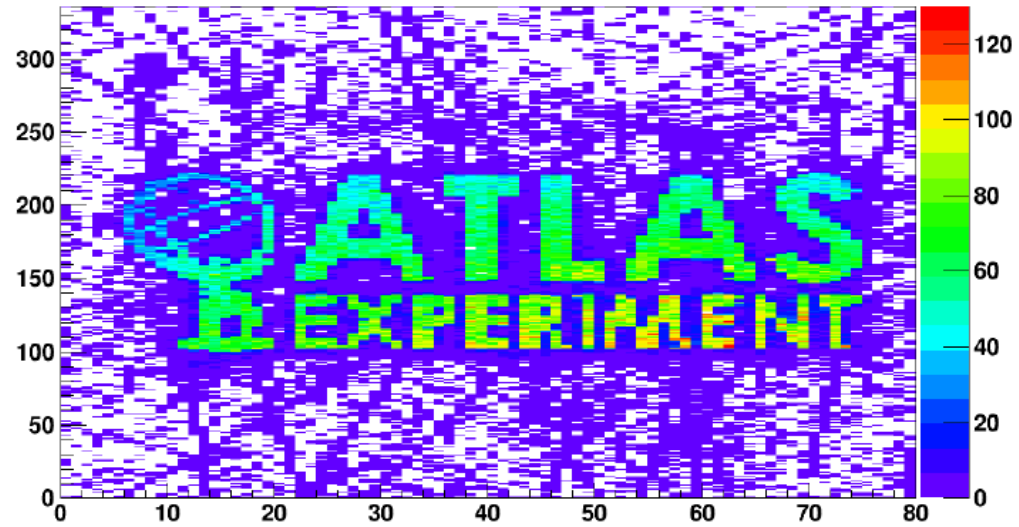
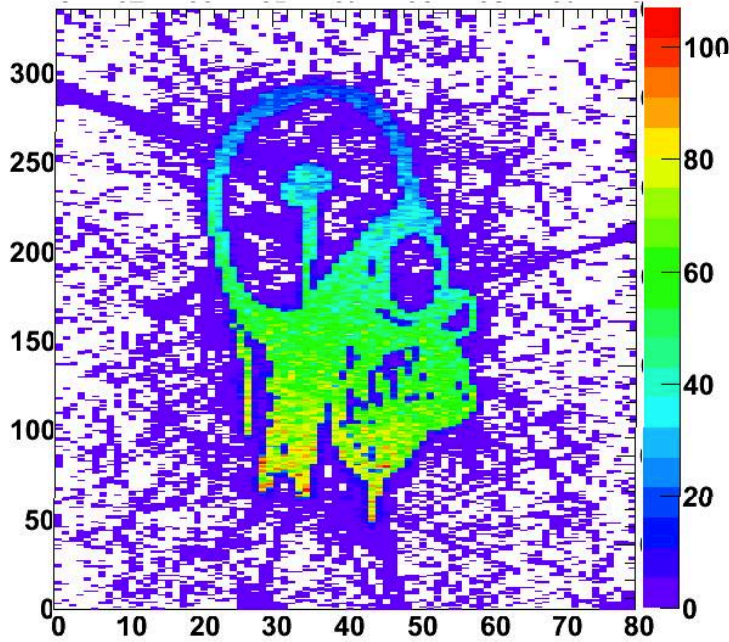


# 4 Telescope

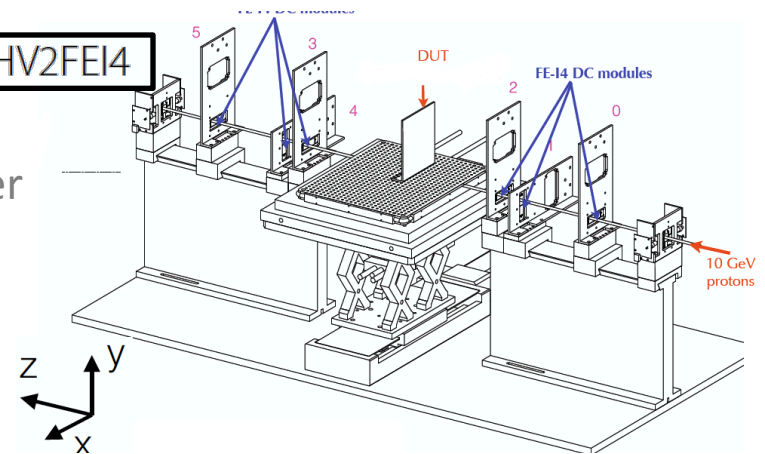
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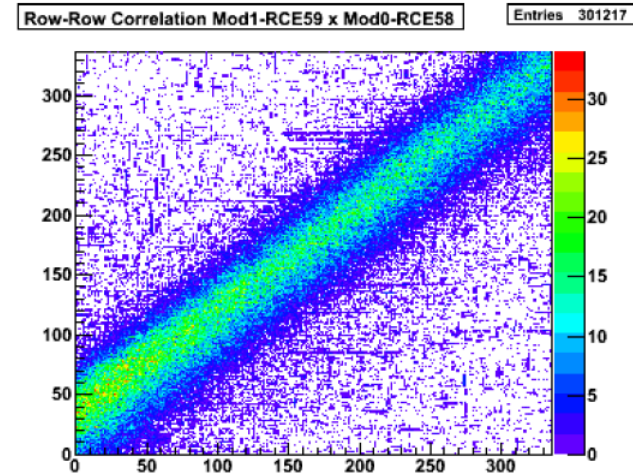
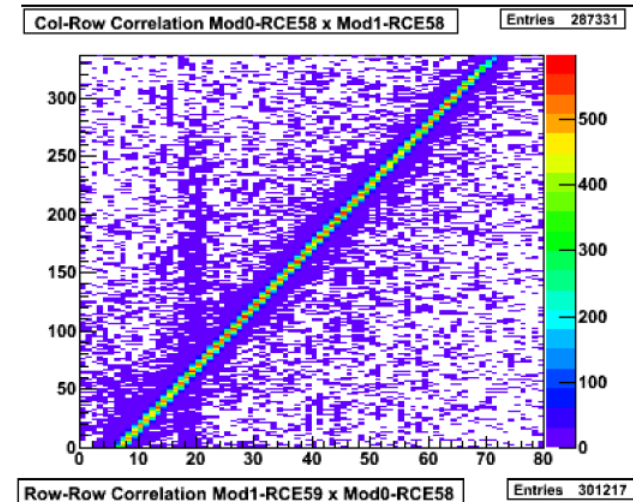
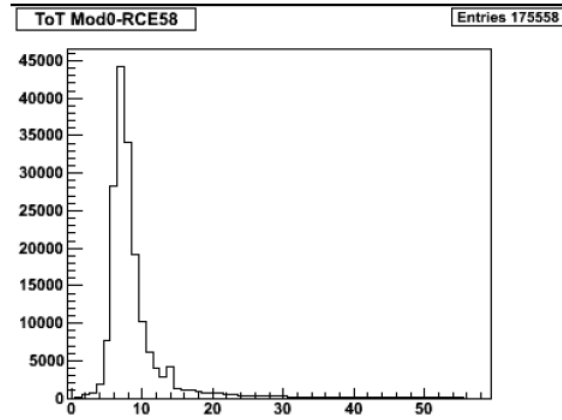
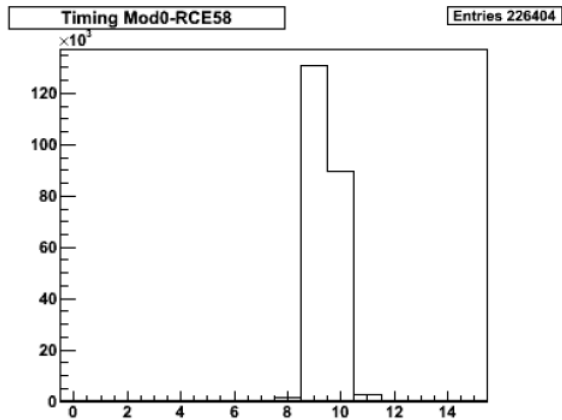


2014 SPS Data



# Online Monitoring/Reconstruction

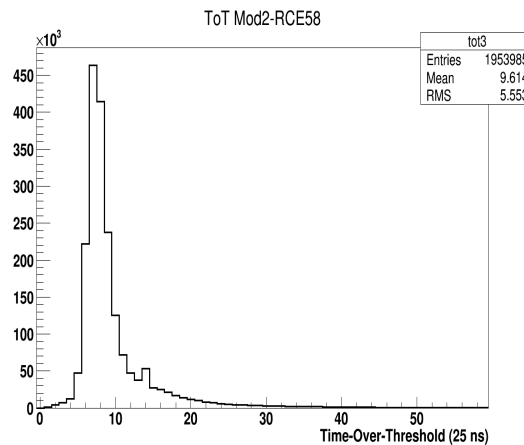
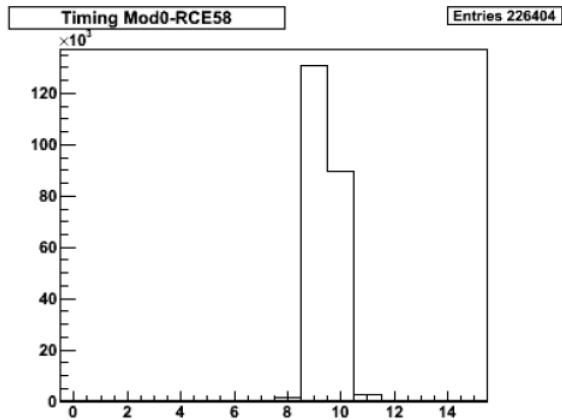
- Telescope copes quite nicely with the beam at PS T9
  - Mixed particle beam, 1-10GeV
- DAQ runs very stable → No problems in days
- Triggered on Hitbus of telescope planes
  - Up to 7000 trig/spill (spill length: ~400ms)
  - ROI trigger comes for free
- Timing as expected for unirradiated IBL sensors
- Quite clear correlations, however multiple scattering visible
  - High material budget for 10GeV



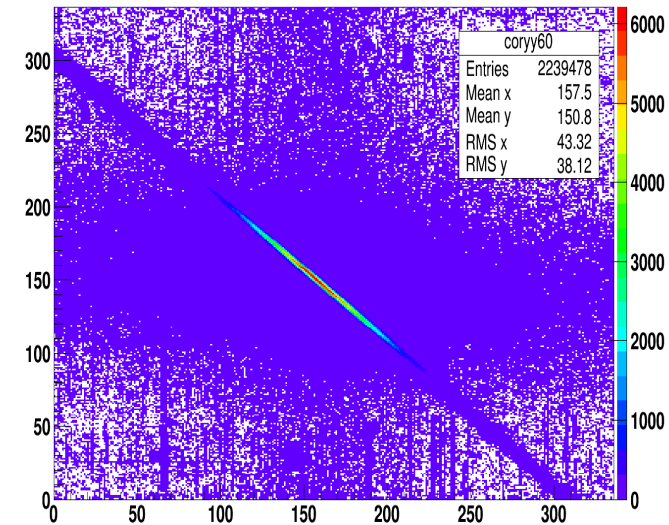
PS Data

# Online Monitoring/Reconstruction

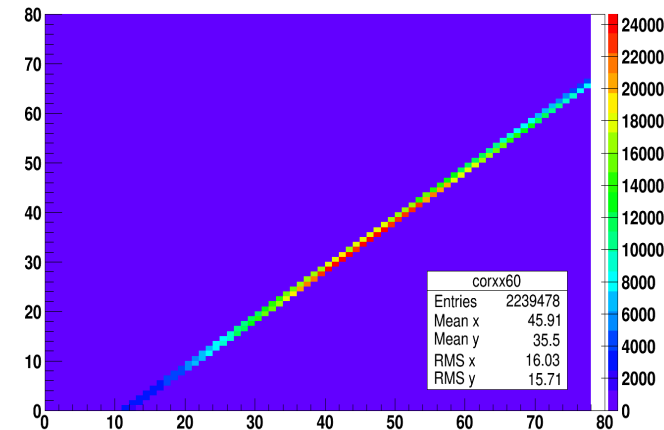
- Telescope copes quite nicely with the beam at SPS
  - 180 GeV pion beam
- DAQ runs very stable → No problems in days
- Triggered on Hitbus of telescope planes
  - Up to 7000 trig/spill (spill length: ~400ms)
  - ~20000 trigger/ spill
- Timing as expected for unirradiated IBL sensors
- Quite clear correlations,



Row-Row Correlation Mod1-RCE59 x Mod2-RCE59



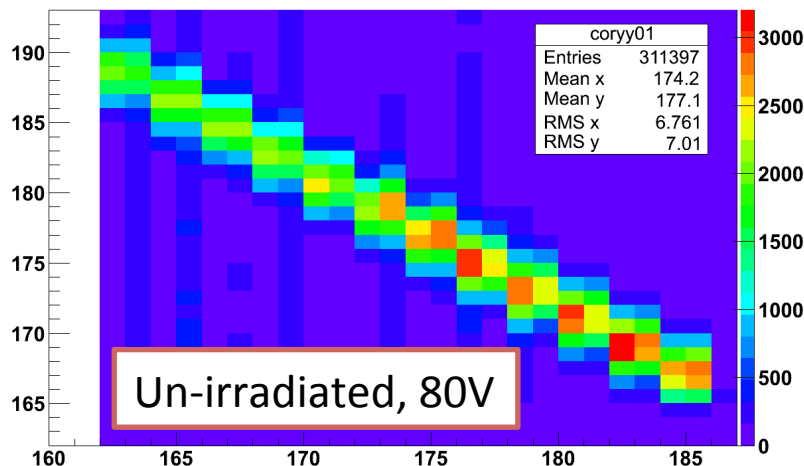
Col-Col Correlation Mod1-RCE59 x Mod2-RCE59



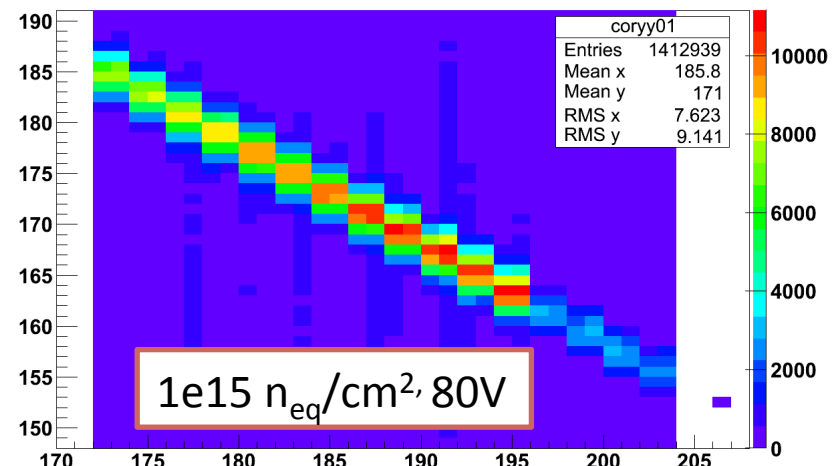
# Test beam characterization of CCPDv2

- CCPDv2 un-irradiated and  $1e15 \text{ n}_{\text{eq}}/\text{cm}^2$  were tested in the beam in October 2014 using the FEI4 telescope
  - C19 (unirradiated) , was operated at room temperature, high noise observed, higher threshold applied to obtain good picture of inefficiency
  - C22 ( $1e15 \text{ n}_{\text{eq}}/\text{cm}^2$ ), was operated a -20C on the DUT box baseplate, 80V bias, much better performance than for C19 ?

Row-Row Correlation Mod2-RCE59 x Mod0-RCE58

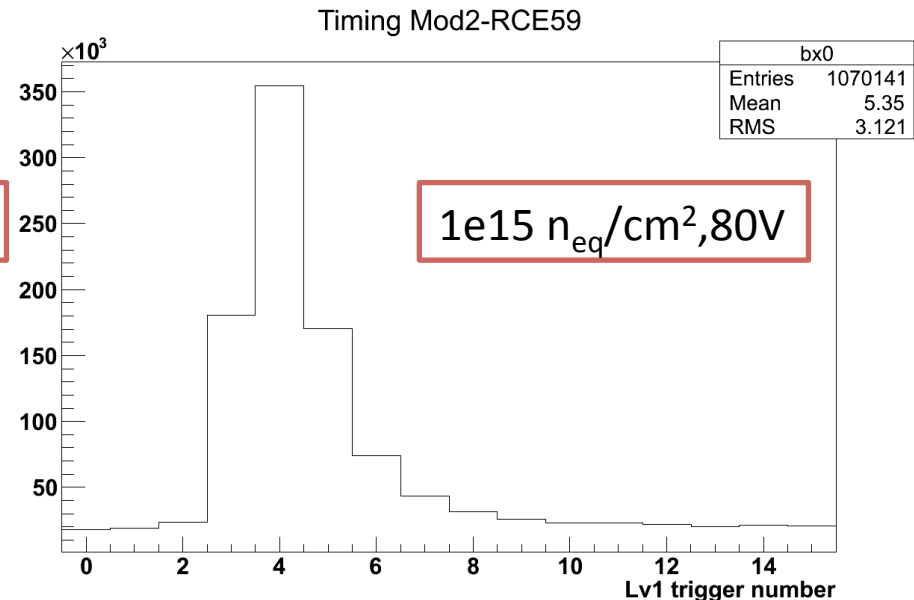
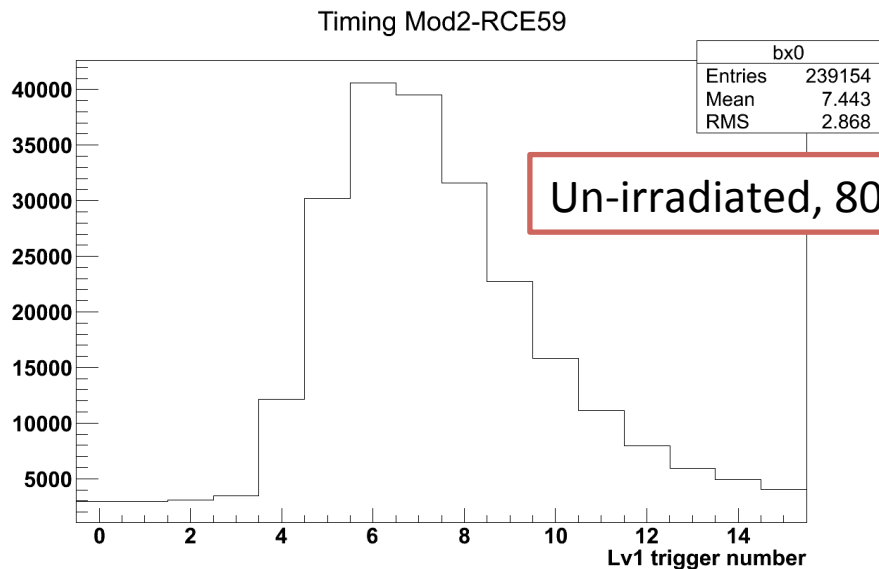


Row-Row Correlation Mod2-RCE59 x Mod0-RCE58



# Test beam characterization of CCPDv2

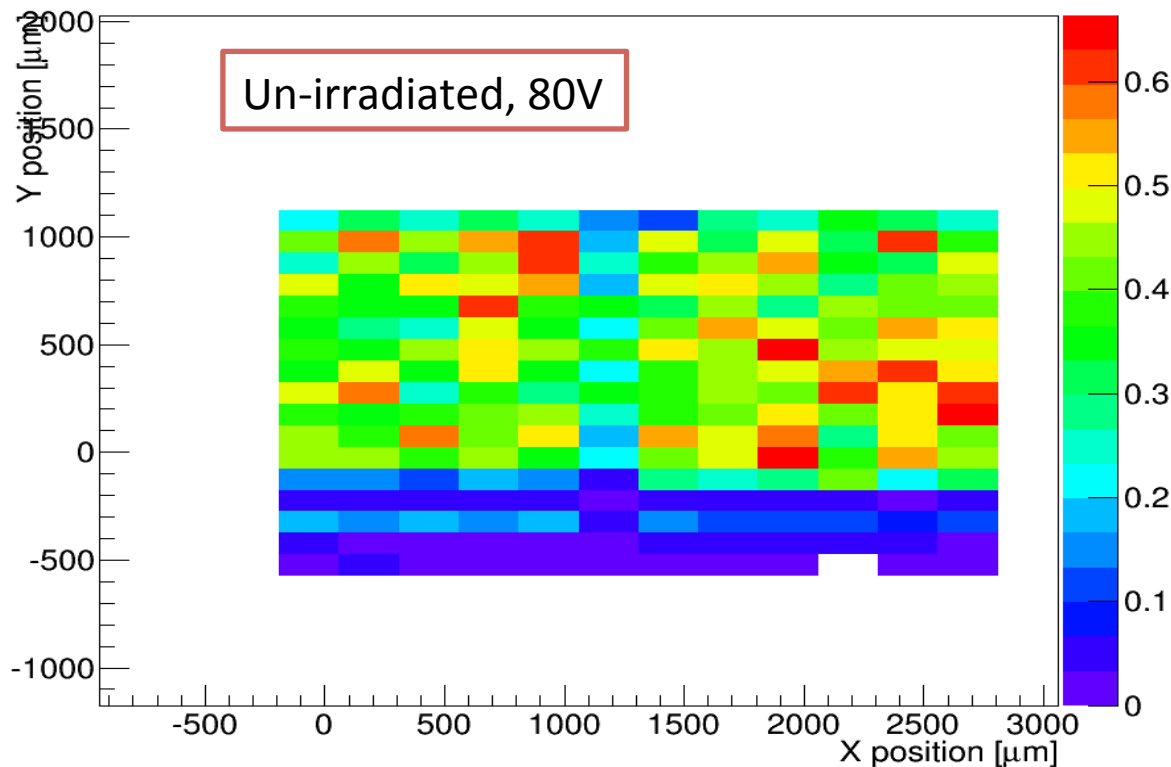
- Timing is improved after irradiation due to the suppression of the diffusion components of the pulse



# Test beam characterization of CCPDv2

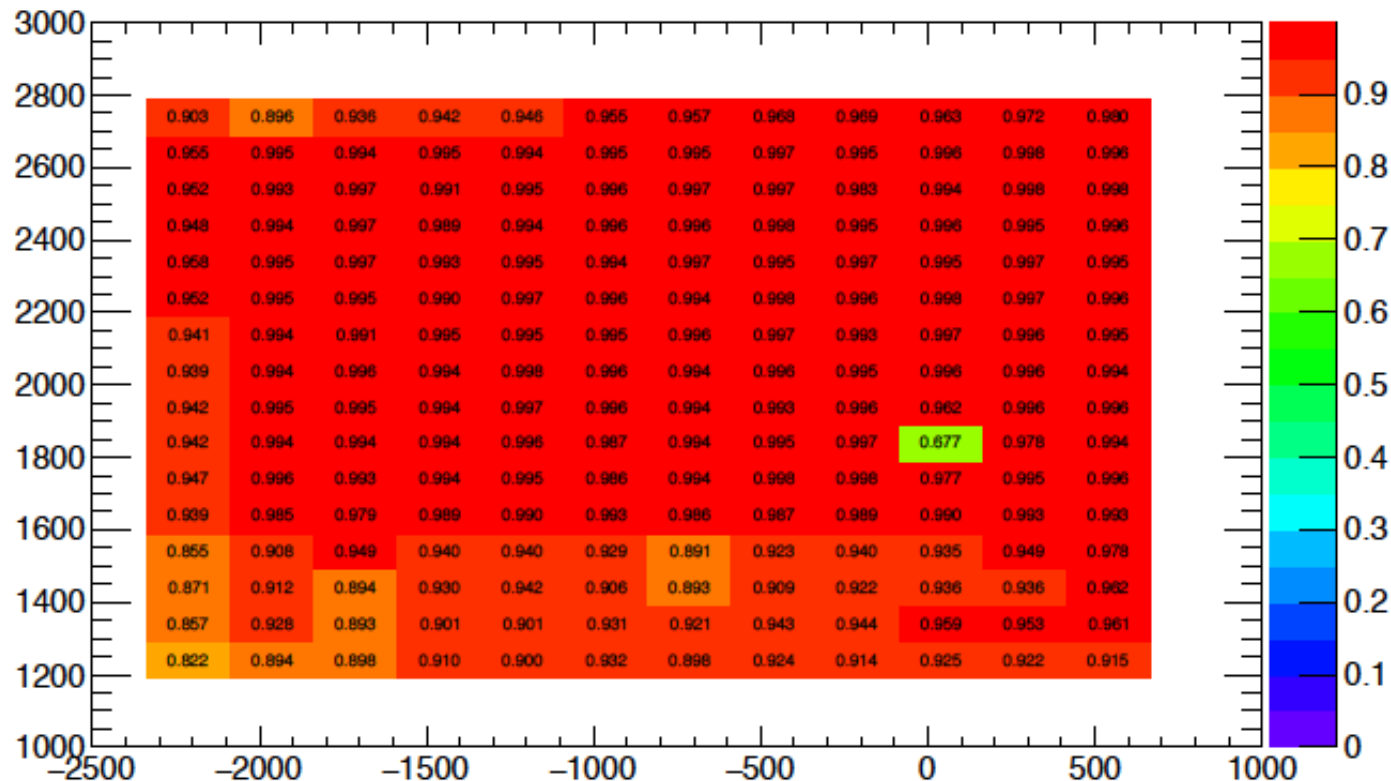
- Efficiency for the unirradiated sample not very good due to High Threshold (96% at PS, to be understood)

DUT Plane0 Efficiency Map



# Test beam characterization of CCPDv2

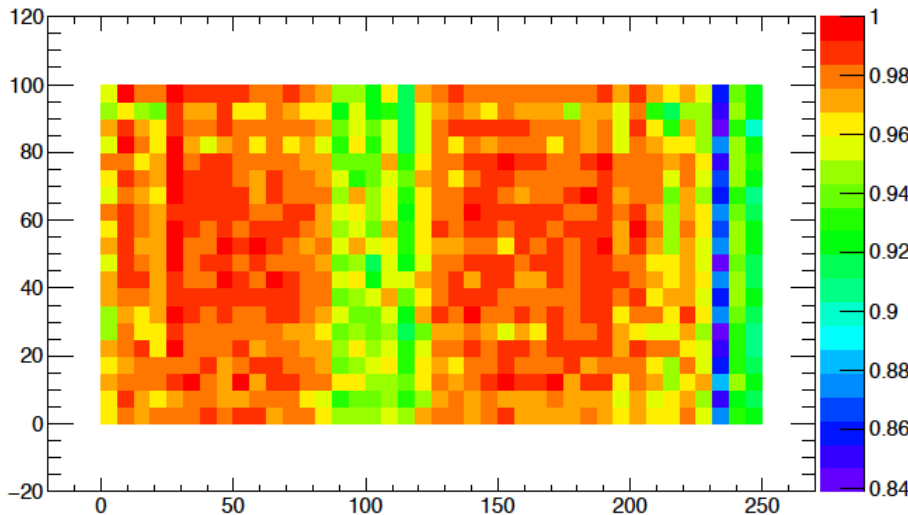
- After fixing electromagnetic compatibility issues and improving the tuning procedure



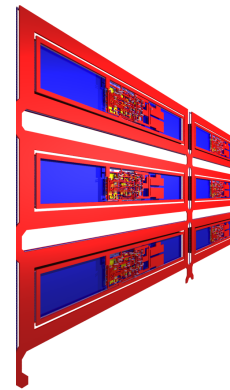
# Test beam characterization of CCPDv2

- In pixel efficiency show clear sign of drop in detection efficiency between the sub-pixels

Un-irradiated, 80V



Very Preliminary !



CCPD Pixels

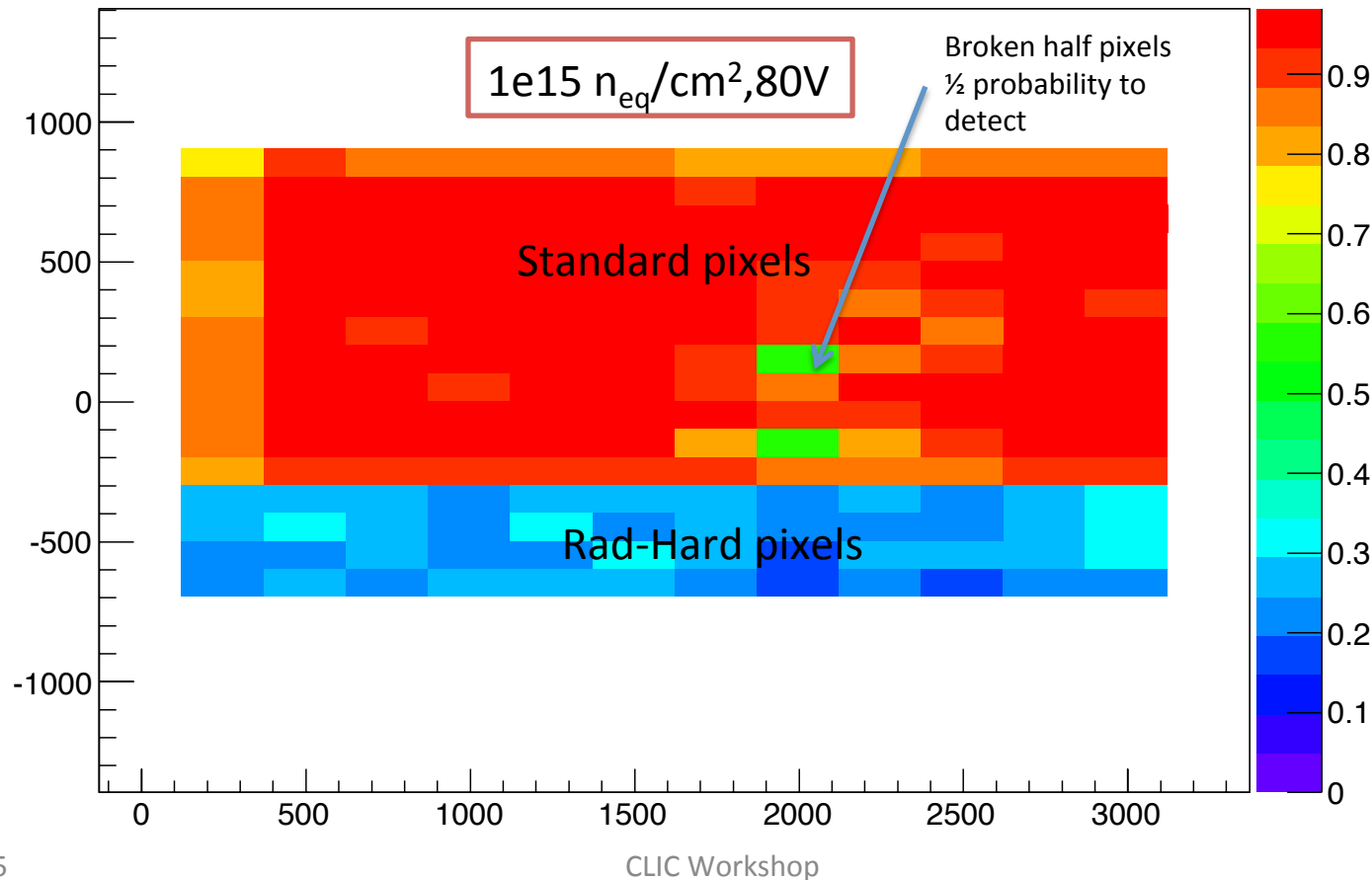
|   |   |  |
|---|---|--|
| 2 | 2 |  |
| 3 | 3 |  |
| 1 | 1 |  |

# Test beam characterization of CCPDv2

- Efficiency for irradiated sample  $> 95\%$

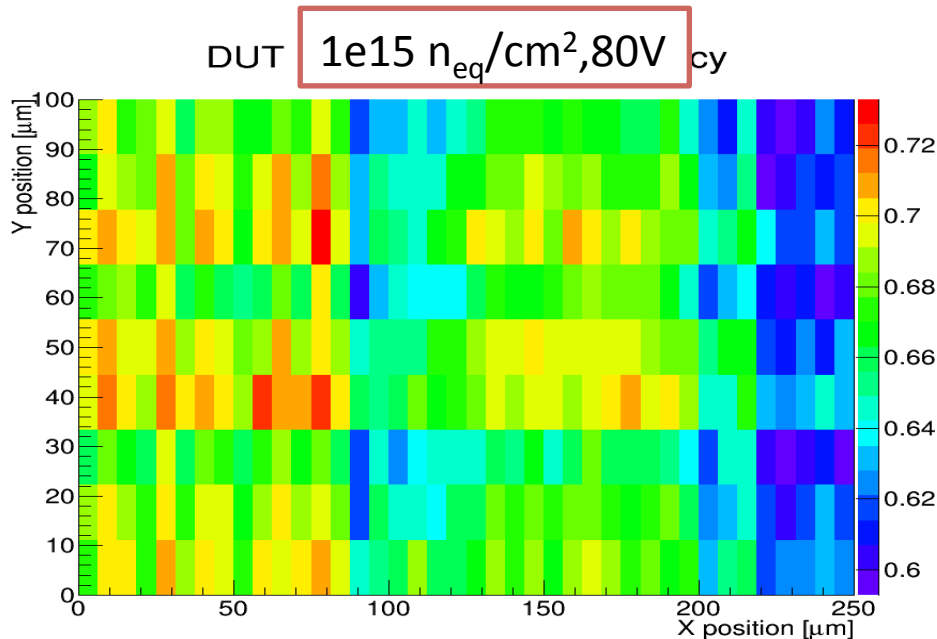
DUT Plane0 Efficiency Map

Very Preliminary !

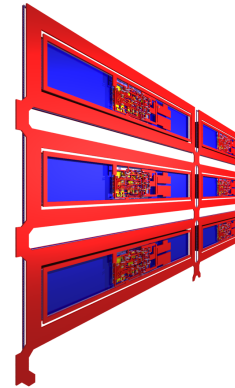


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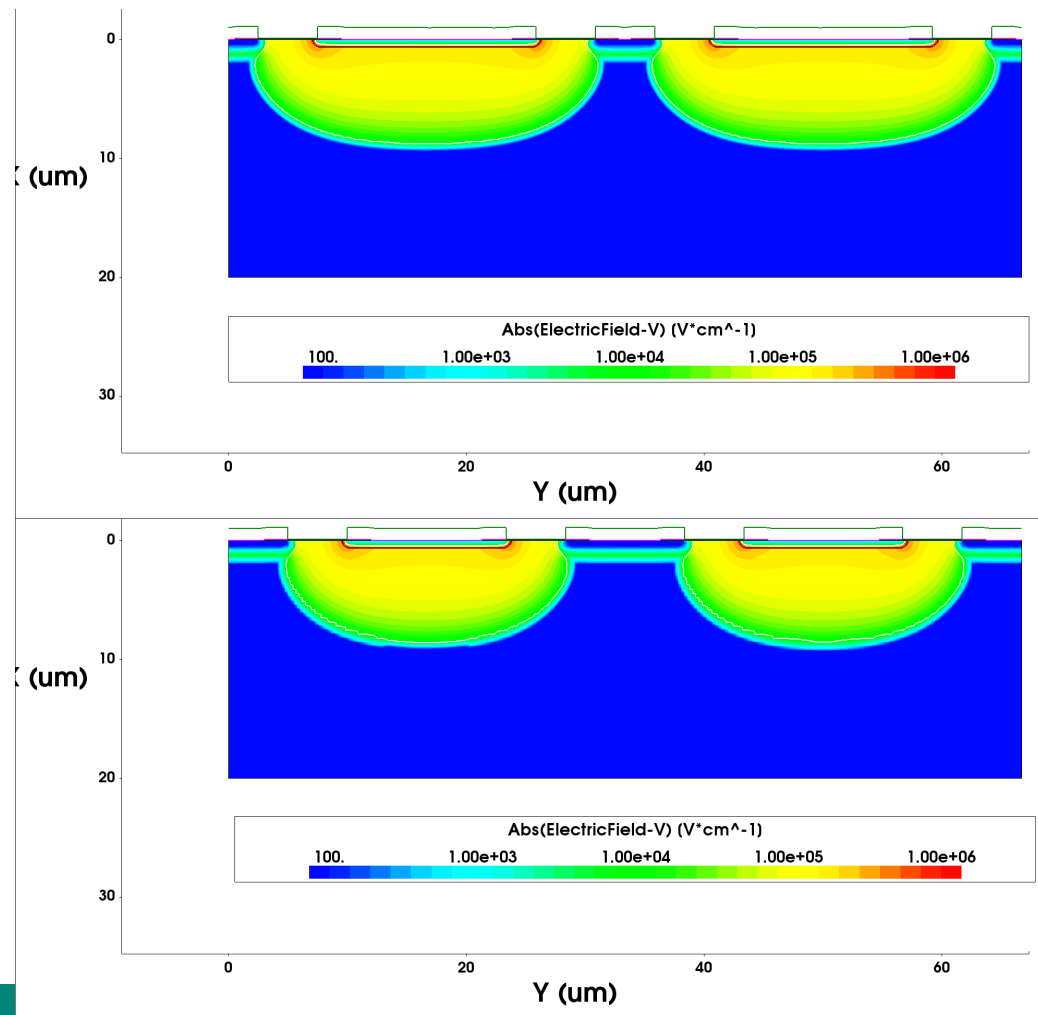


CCPD Pixels

|   |   |  |
|---|---|--|
| 2 | 2 |  |
| 3 | 3 |  |
| 1 | 1 |  |

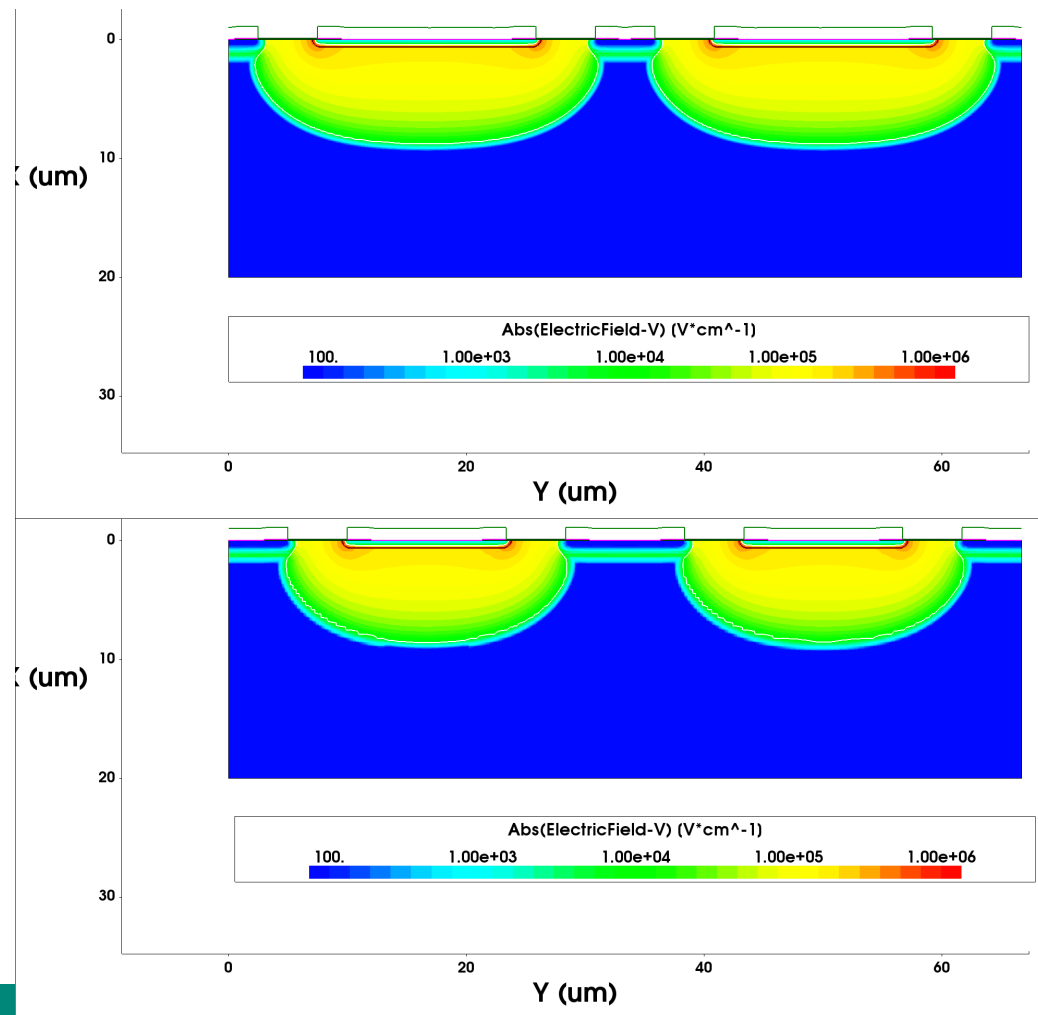
# TCAD Simulation of CCPDv2

Low depletion due to low substrate resistivity and application of the bias voltage by the lateral ring create an undepleted region even at high bias voltage , 10  $\Omega\text{cm}$ , 80V represented here



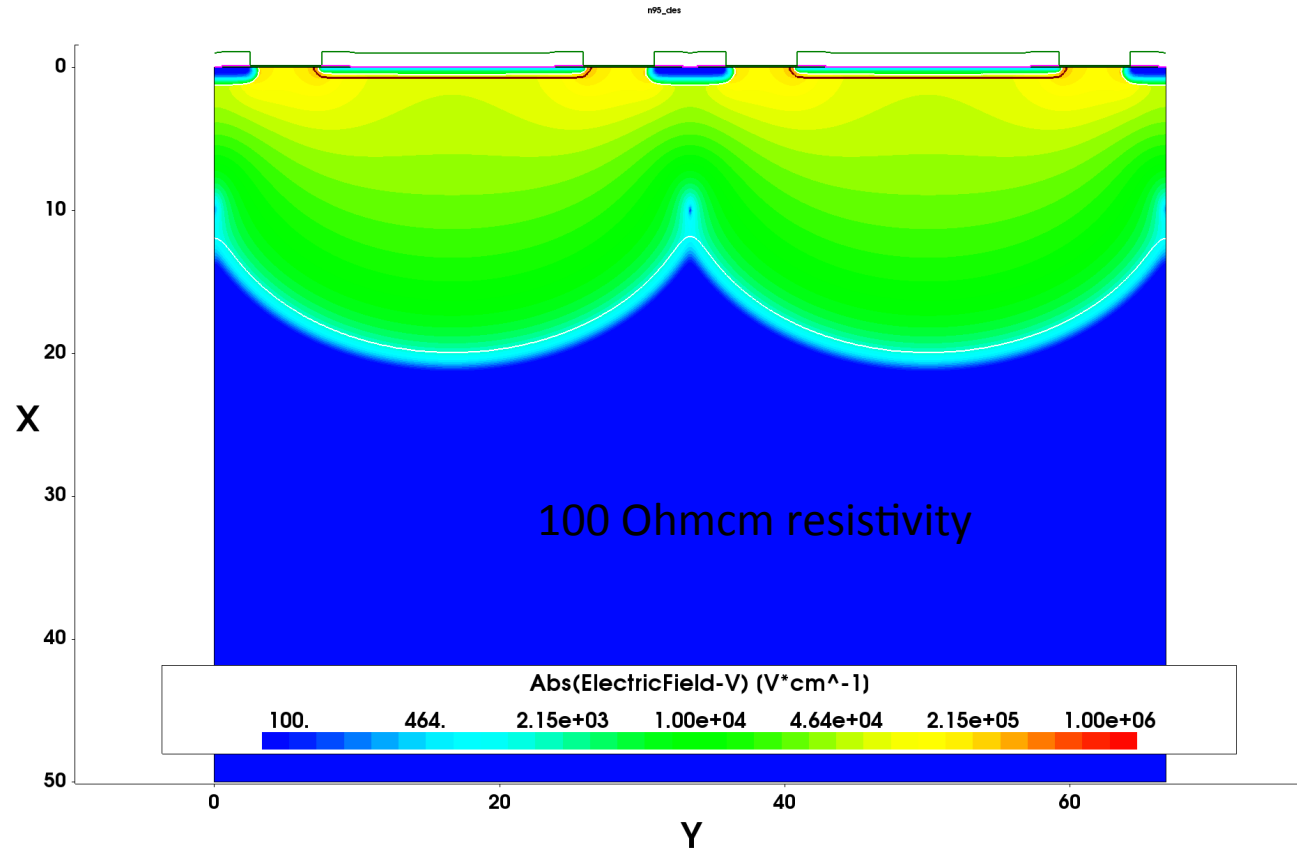
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# TCAD Simulation of CCPDv2

Increasing resistivity and minimizing P implant width would allow to increase field factor, therefore efficiency and timing



# Conclusion

- Test beam with unirradiated and irradiated CCPDv2 samples using the FEI4 telescope yield interesting results. Noise immunity of the test setup need to be improved to get lab performance in the test beam setup
  - 95% efficiency for irradiated sample cooled down to -20C and operated at -80V
  - Zone of inefficiency can be observed in the in pixel detection efficiency data
- Over 6 billion triggers with CCPDV2,v4, irradiated and unirradiated collected during last testbeam, analysis ongoing
- A new  $\sim\text{cm}^2$  HVCMOS demonstrator is being design, incorporating the lesson learned from the current prototypes

## Thanks to the HV-CMOS Collaboration

- University of Bonn  
L. Gonella, T. Hemperek, F. Hügging, H. Krüger, T. Obermann, N. Wermes
- LBNL  
M. Garcia-Sciveres
- CERN  
M. Backhaus, M. Capeans, S. Feigl, S. Fernandez Perez, M. Nessi, H. Pernegger, B. Ristic, M. Tavassoli
- University of Geneva  
S. Gonzalez-Sevilla, D. Ferrere, G. Iacobucci, A. Miucci, D. Muenstermann, A. La Rosa
- University of Goettingen  
M. George, J. Große-Knetter, A. Quadt, J. Rieger, J. Weingarten
- University of Glasgow  
R. Bates, A. Blue, C. Buttar, D. Hynds
- University of Heidelberg  
C. Kreidl, I. Peric
- CPPM  
P. Breugnon, P. Pangaud, D. Fougeron, F. Bompard, J.C. Clemens, J. Liu, M. Barbero, A. Rozanov

“Original” collaboration largely based on institutes with expertise in pixel readout chips, recently also much interest from strip upgrade community...