MARTINO FERRARI
on behalf of
BE-BI-SW

CHALLENGES AND CONSTRAINTS FOR BI/SW

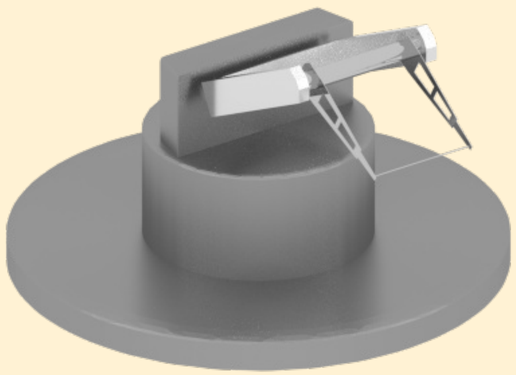
16.10.2014

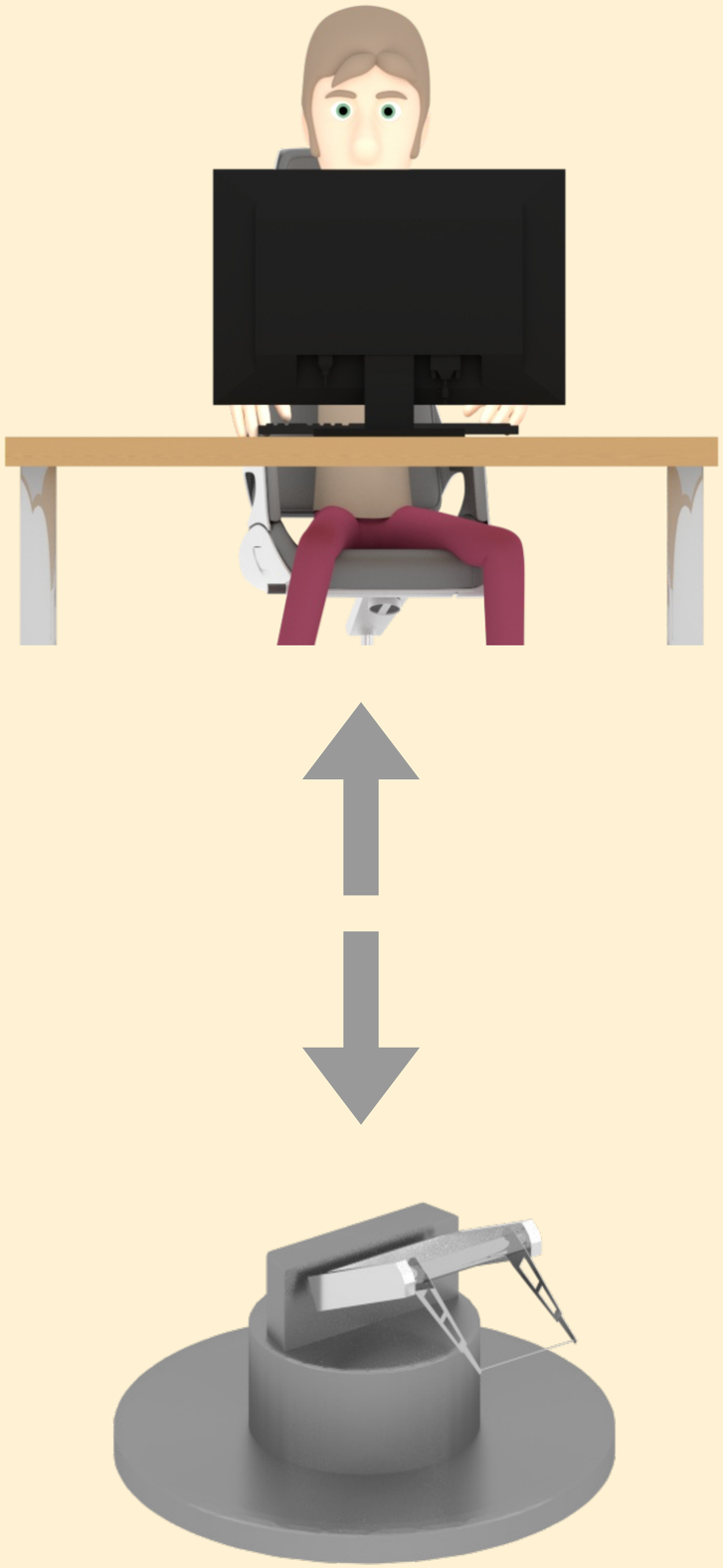
BI DAY

OUTLINE

1. Who we are
2. Accelerator Control System overview
3. What we do
    - 3.1. Custom board and driver
    - 3.2. Front End Computer
    - 3.3. FESA overview
    - 3.4. FESA development
    - 3.5. Expert applications and other tools
4. Constraints
5. Conclusions

WHO WE ARE



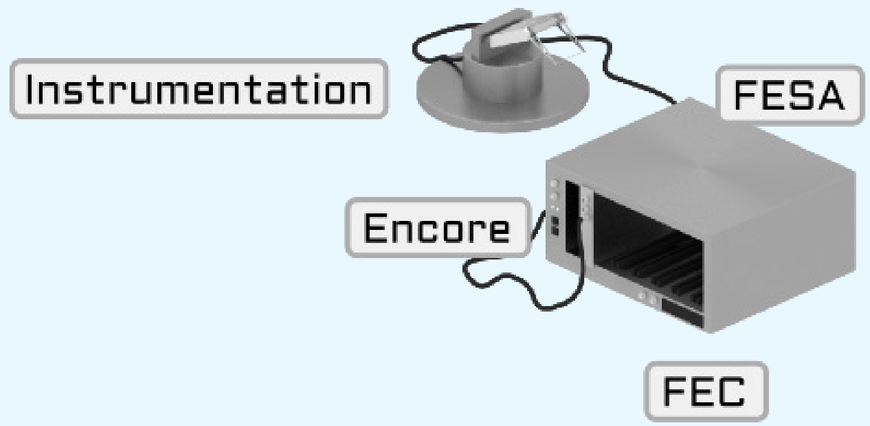


WHO WE ARE

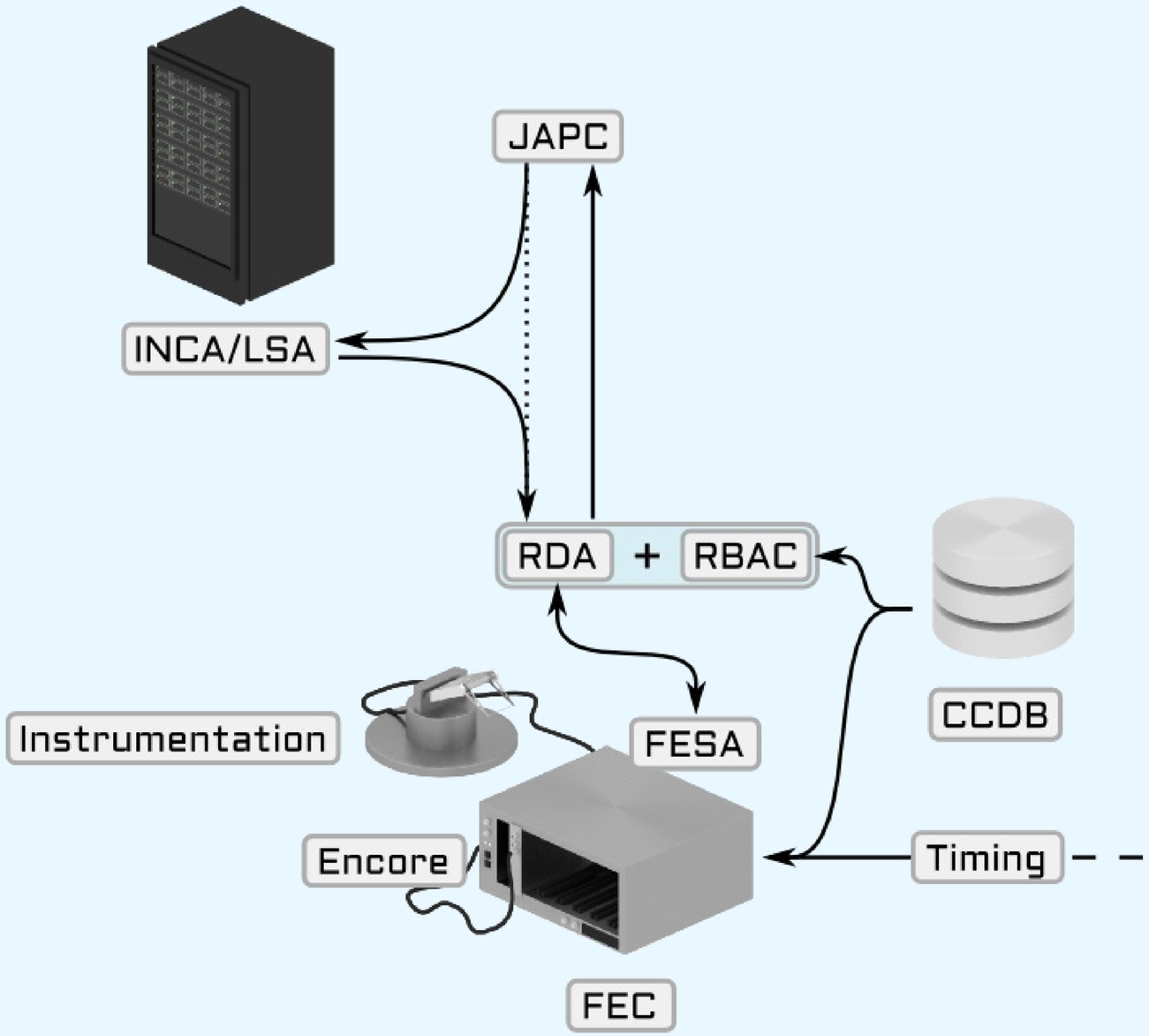
The **BE-BI Software Section** provides all the software necessary to develop, test, diagnose and maintain the different instruments produced by the Group.

We provide tools to allow other people to work (operators/hardware experts)

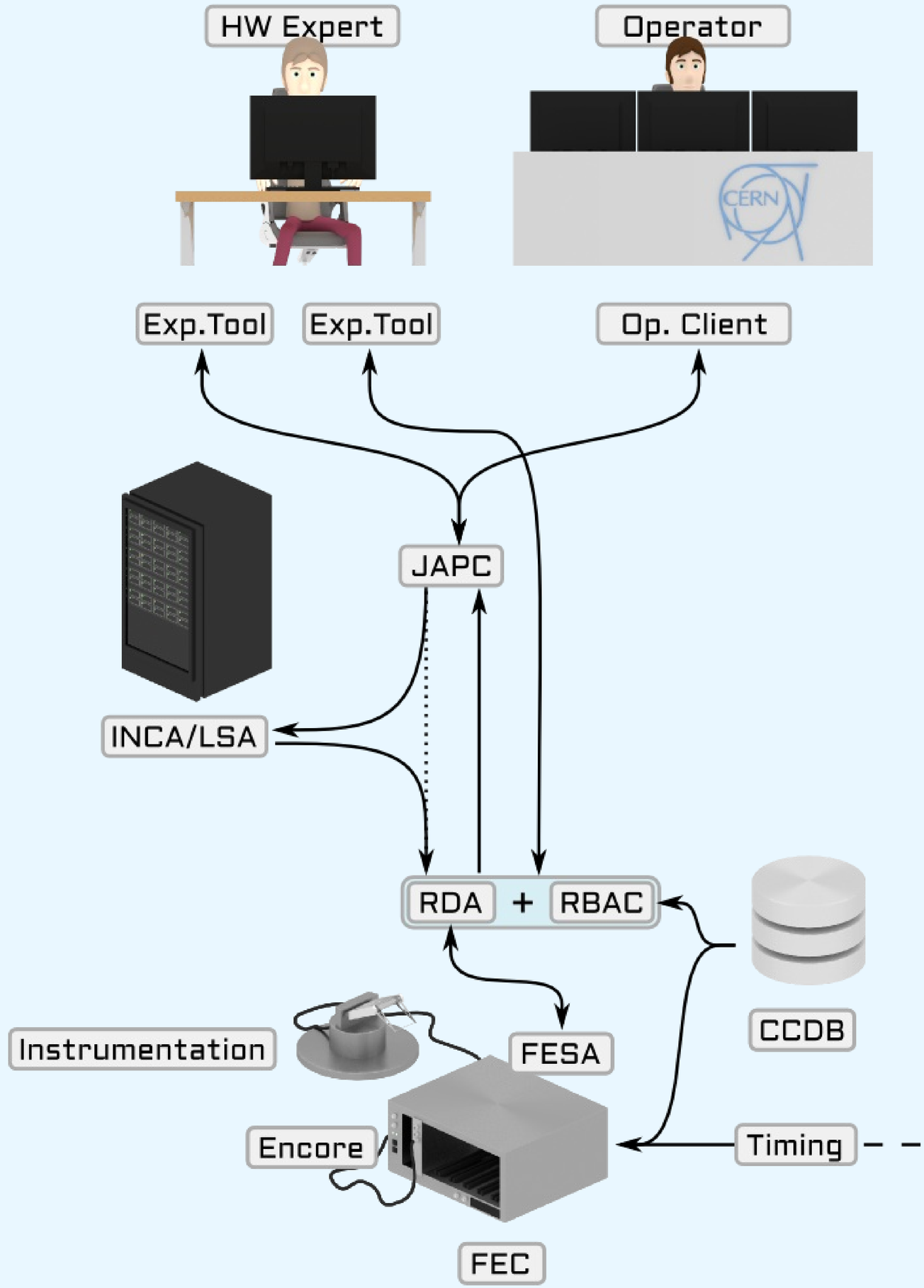
ACCELERATOR CONTROL SYSTEM



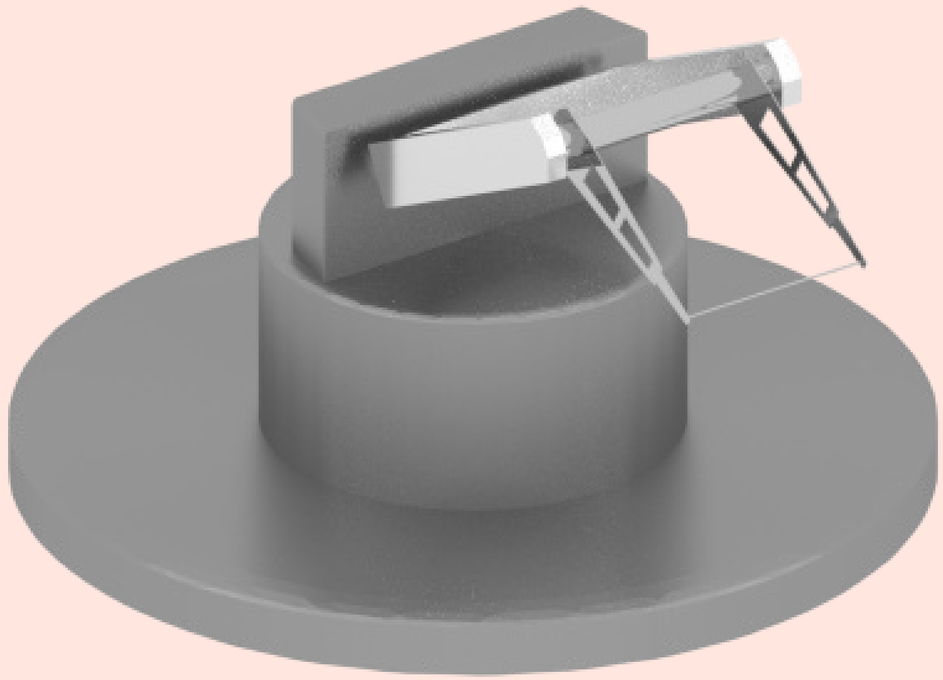
ACCELERATOR CONTROL SYSTEM



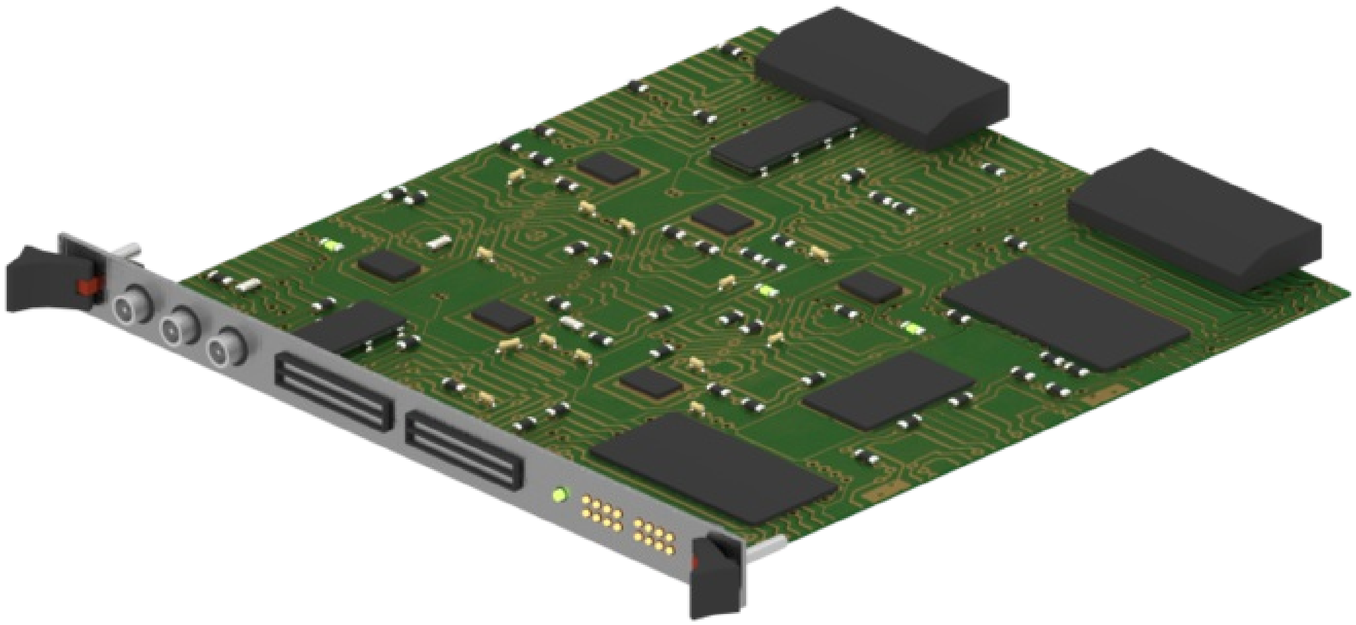
ACCELERATOR CONTROL SYSTEM



WHAT WE DO



A CUSTOM BOARD AND ITS DRIVER



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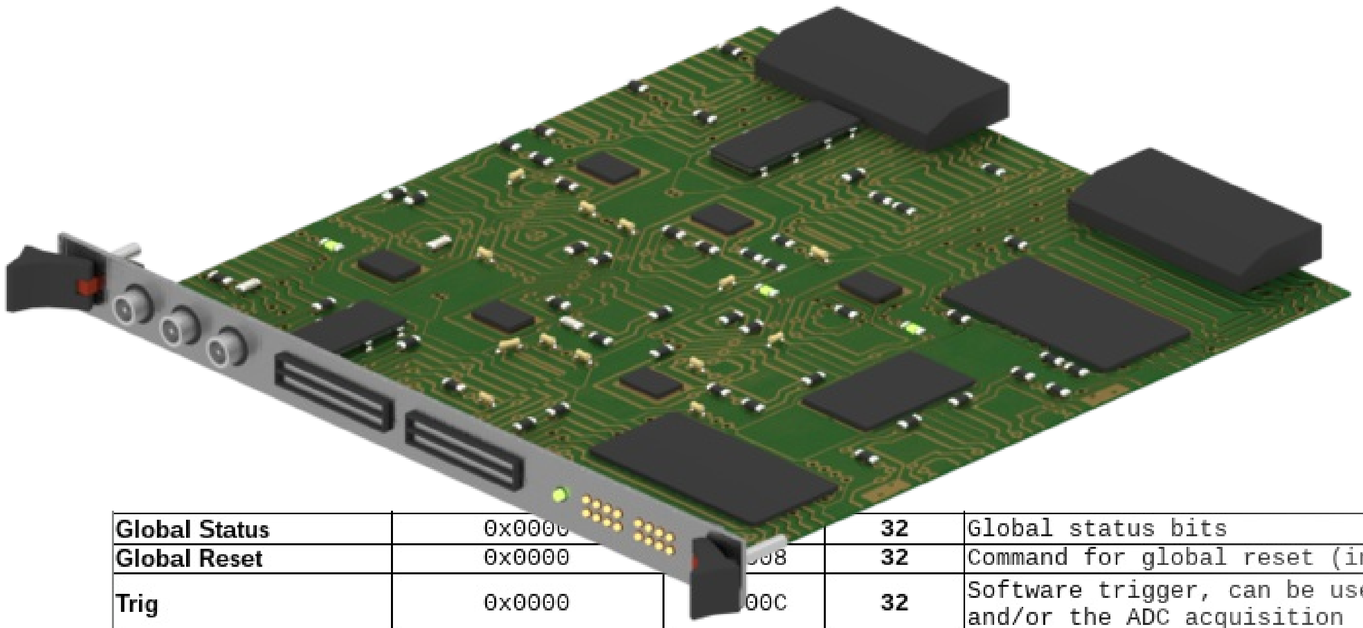
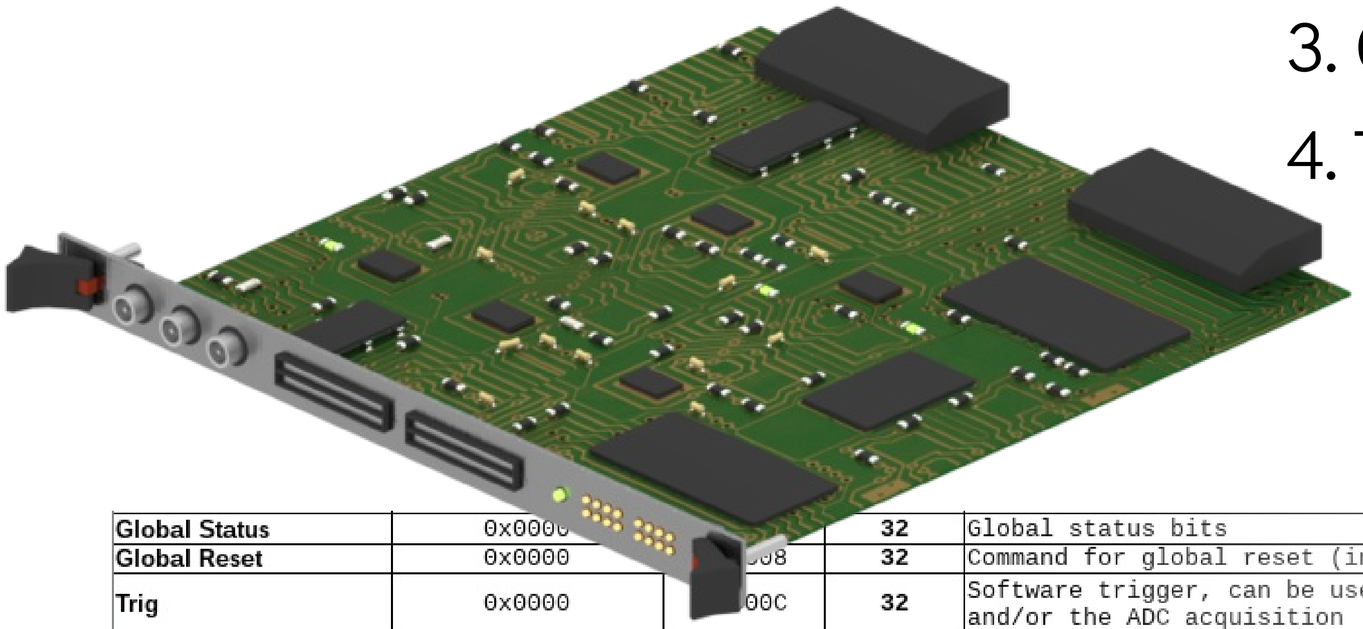


Global Status	0x0000	[illegible]	**32**	Global status bits	R	32	T.B.D.
Global Reset	0x0000	[illegible]08	**32**	Command for global reset (in parallel with VME SYSRESET)	W	0	
Trig	0x0000	[illegible]00C	**32**	Software trigger, can be used to start the motor movement and/or the ADC acquisition	W	0	
Clock Selection	0x0000	0x0010	**32**	Select the global clock source	R/W	1	0 == External 1 == Internal
Internal Clock Divider	0x0000	0x0014	**32**	The internal clock frequency is equal to 1 MHz divided by the content of this register (plus 1). The clock (internal or external) is used to clock the ADC sampling and to generate the control gate pulses for the preamplifier.	R/W	20	0 - 0x1FFFFF (1 MHz - 0.48 Hz)
External clock delay	0x0000	0x0018	**32**	The external clock pulse can be delayed by putting a non zero value in this register. Delay [ns]= reg*40	R/W	32	0 - 0xFFFFFFFF

A CUSTOM BOARD AND ITS DRIVER

1. Getting your specifications
2. Defining the memory registers in the Control DB
3. Generating the driver with ENCORE
4. Testing it!



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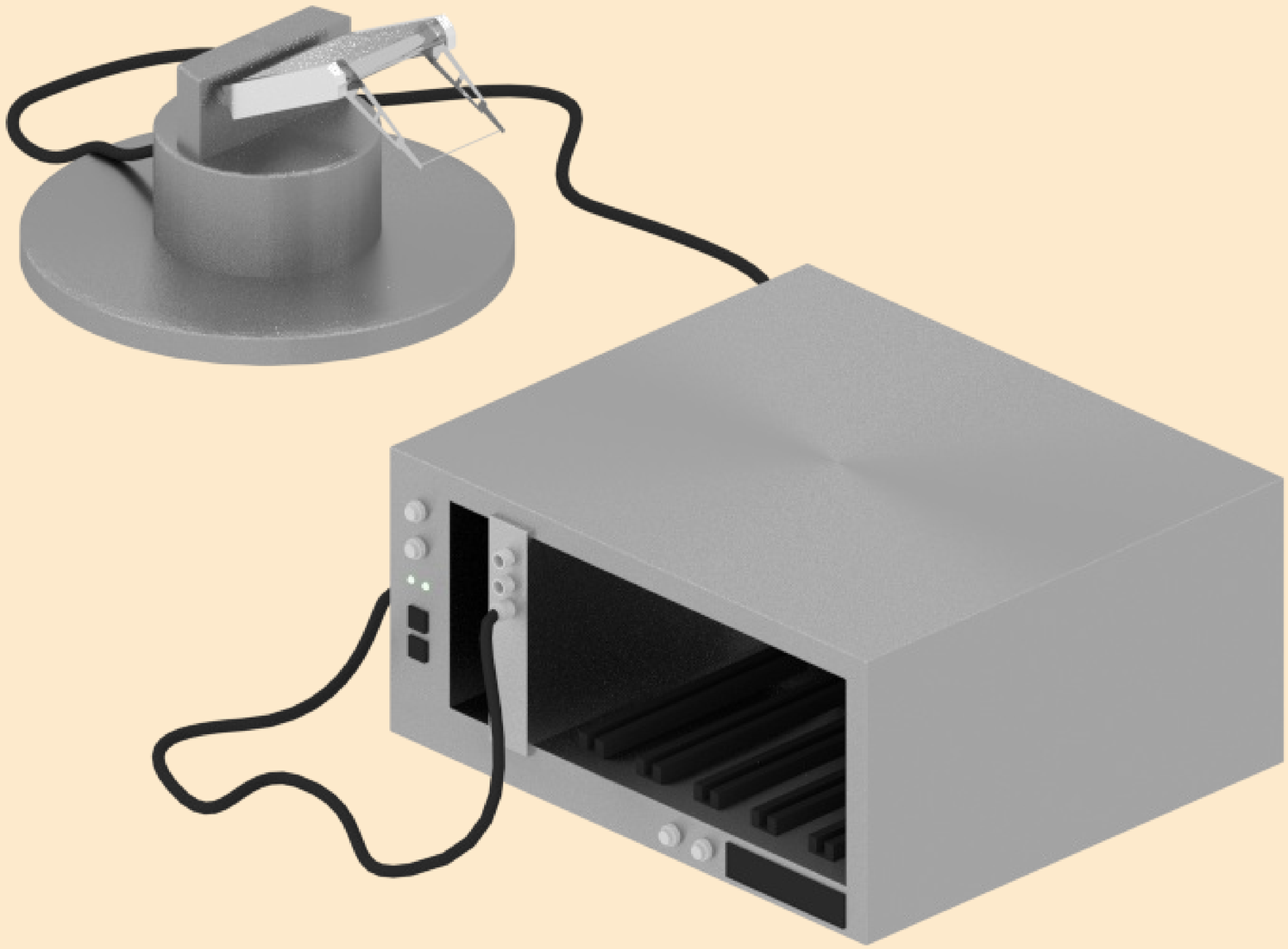
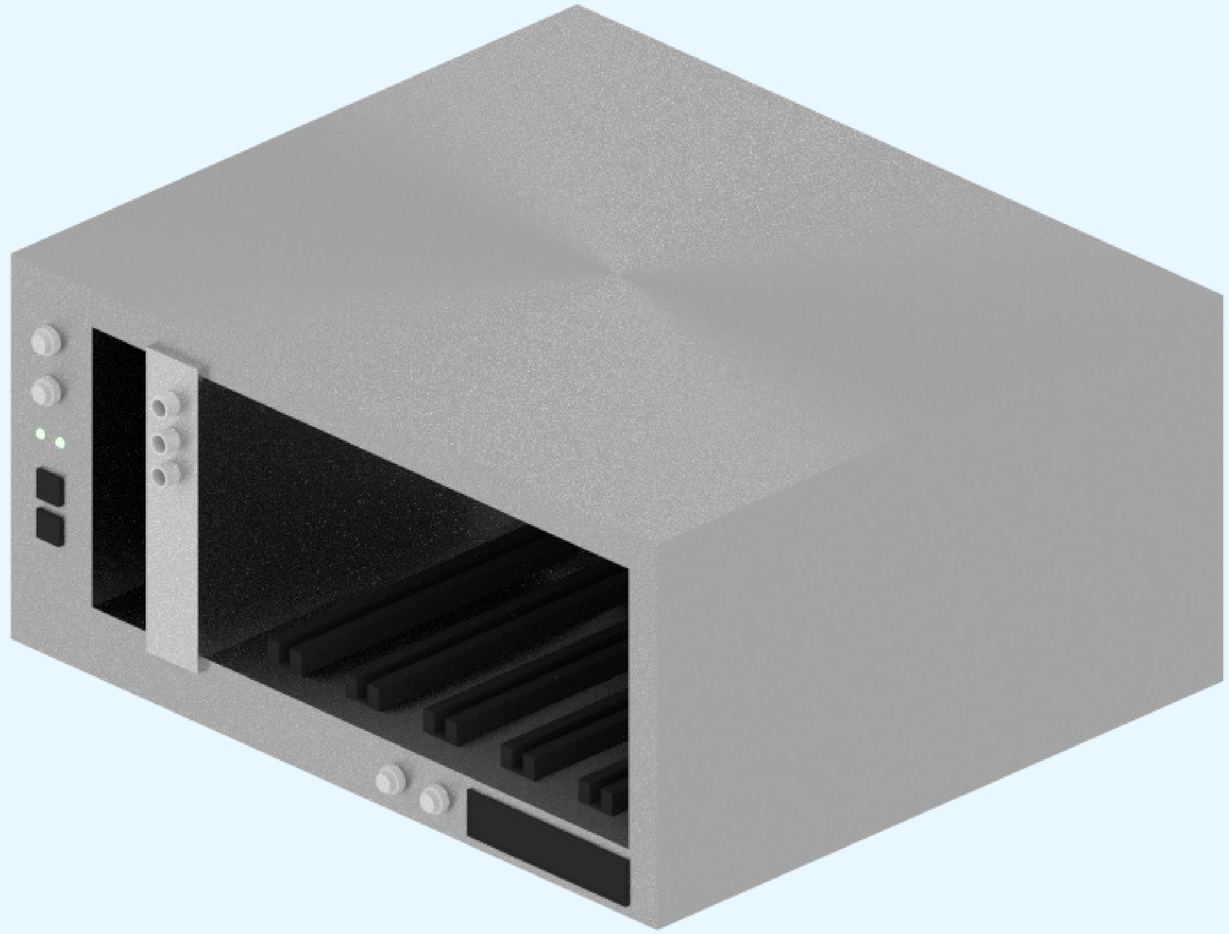
FRONT END COMPUTER

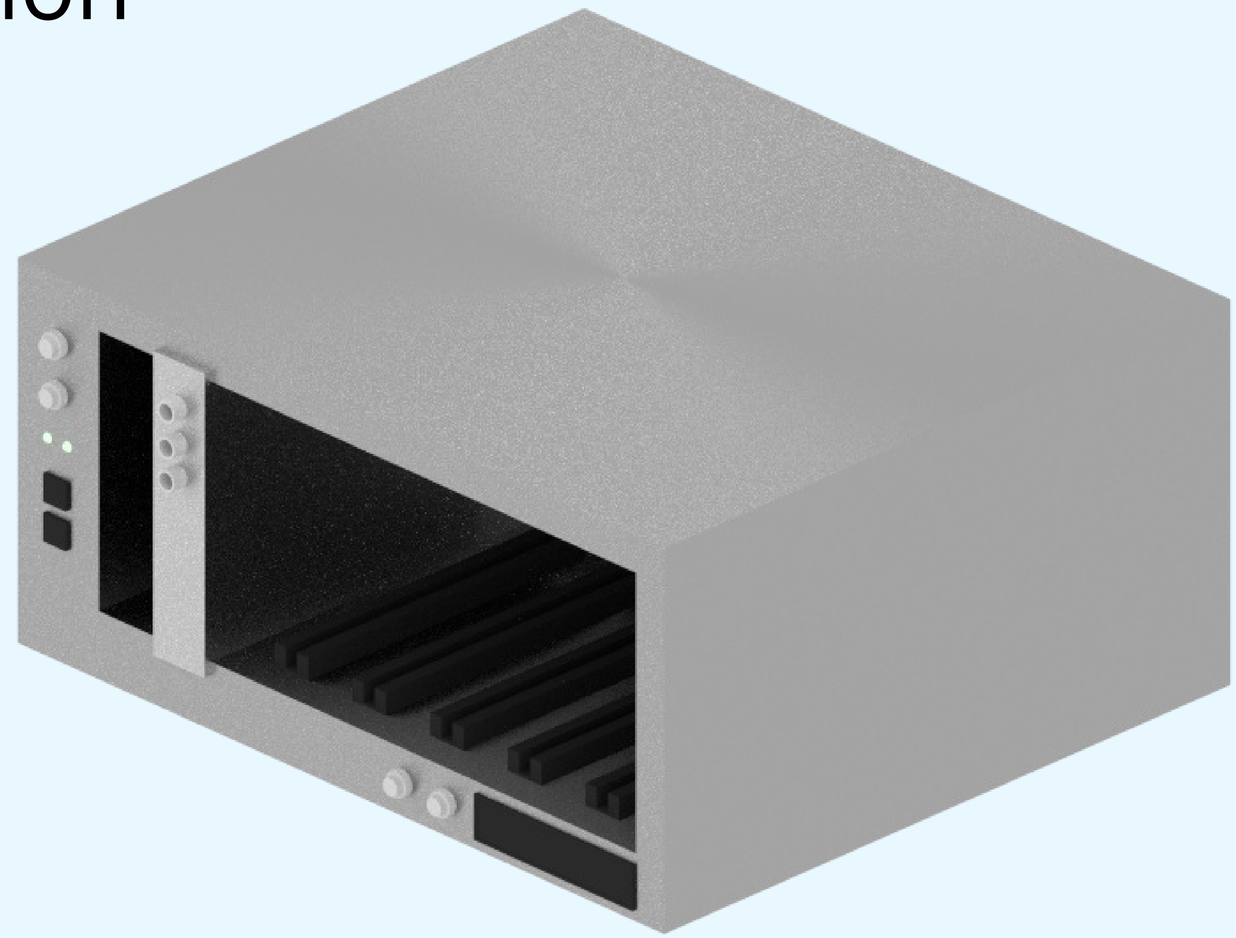


F.E.C.



F.E.C.

- Control DB configuration
- System configuration



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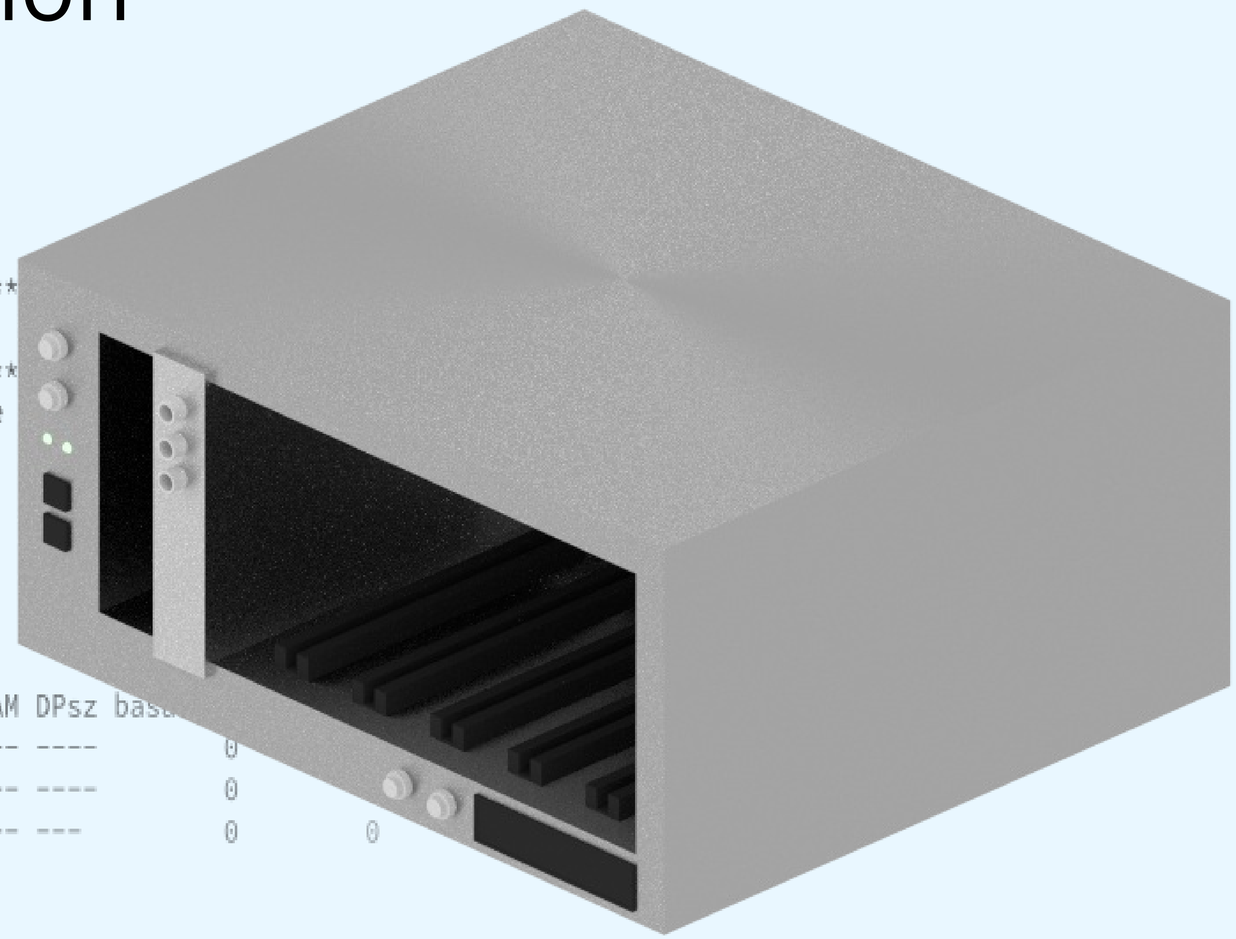
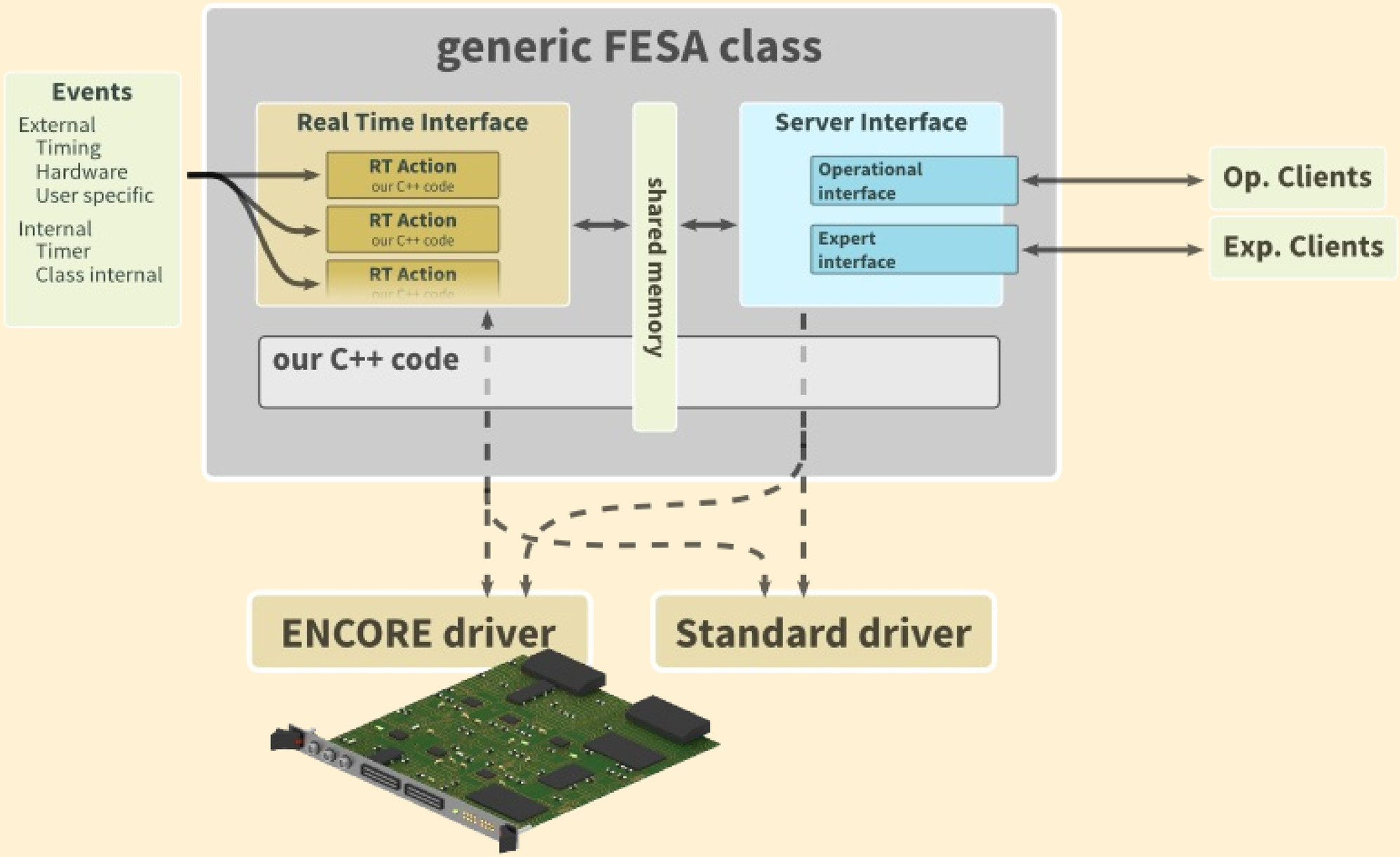


```
#*************************************************************************
# $Id: transfer.ref,v 1.21 2013/10/23 13:19:30 anag Exp $
#*************************************************************************
# WARNING: File generated from database. Can be overwritten at any time

# Host        cfv-865-bidev6

#   sl ss lun module-type         vendor device  subv  subdev
#@#  1  0   0 CTRP                 10dc   0300   10b5   9030

#   ln mln bus mtno module-type      lu W AM DPsz basaddr1   range1 W AM DPsz bas
#+#  1   0 PCI  502 CTRP              0 N -- DP16        0        0 N -- ----        0
#+#  2   0 VME 2279 MEN-A20           0 N -- DP16        0        0 N -- ----        0
#+#  3   0 VME 2408 BI_ADCSTEP        0 N ST DP32   300000   100000 N -- ---         0        0


#% mkdir -p /nfs/cs-ccr-nfs6/vol21; /bin/mount  -o intr,rsize=8192,wsize=8192  cs-ccr-nfs6:/vol21 /nfs/cs-ccr-nfs6/vol21

# Restore DataTable for GM equipment
#% dtrest >/dev/con 2>&1

# Install data used by ioconfig library
#% ioconfigInstall  >/dev/con 2>&1

#% cd /usr/local/drivers/ctr; ctrinstall
##% cd /usr/local/drivers/bi_adc36; install_bi_adc36.sh
#% cd /usr/local/drivers/bi_adcstep; install_bi_adcstep.sh
```

FESA

How does it work?



SPECIFICATIONS

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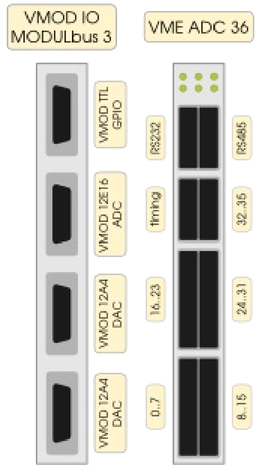
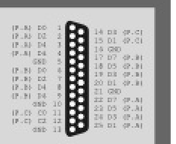
Hardware specifications



MODULbus 3
VMOD IO

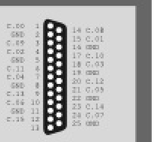
VMOD-TTL

20 bit TTL I/O
Single 4 bit and double 8 bit I/O



VMOD-12E16

16 single analog input 12bit resolution
167 kHz sampling rate max.
+/-10V,+/-5V,0-10V,0-5V iputs



VMOD-12A4

4 channel analog output 12bit resolution
100 MHz sampling rate max.
+/-10V,+/-5V,0-10V,0-5V outputs

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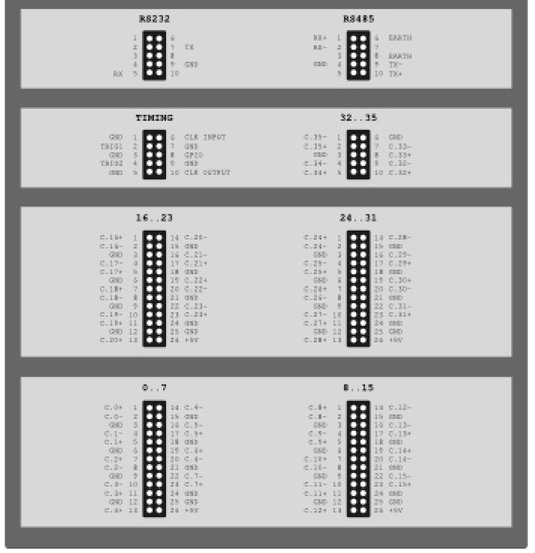
4 channel analog output 12bit resolution
100 MHz sampling rate max.
+/-10V,+/-5V,0-10V,0-5V outputs

VME ADC 36

36 input at 16 bit resolution
250 kS/s per channel
2x (digital) trigger input
+/-5V, +/- 10V input
Adjustable gain



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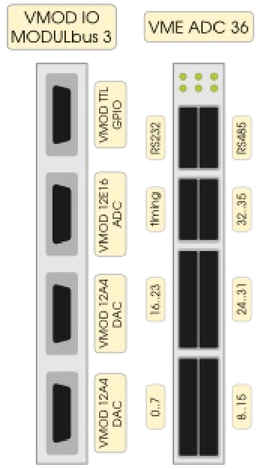

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VMOD IO

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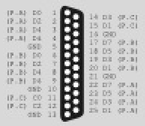
20 bit TTL I/O
Single 4 bit and double 8 bit I/O



VMOD-12E16

16 single analog input 12bit resolution
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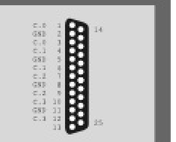
+/-10V,+/-5V,0-10V,0-5V iputs

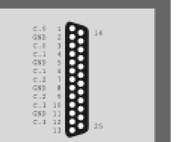
VMOD-12A4

4 channel analog output 12bit resolution
100 MHz sampling rate max.
+/-10V,+/-5V,0-10V,0-5V outputs



VMOD-12A4

4 channel analog output 12bit resolution
100 MHz sampling rate max.
+/-10V,+/-5V,0-10V,0-5V outputs



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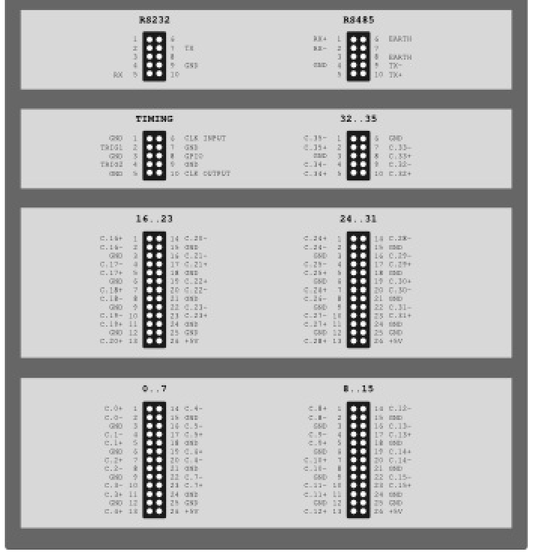
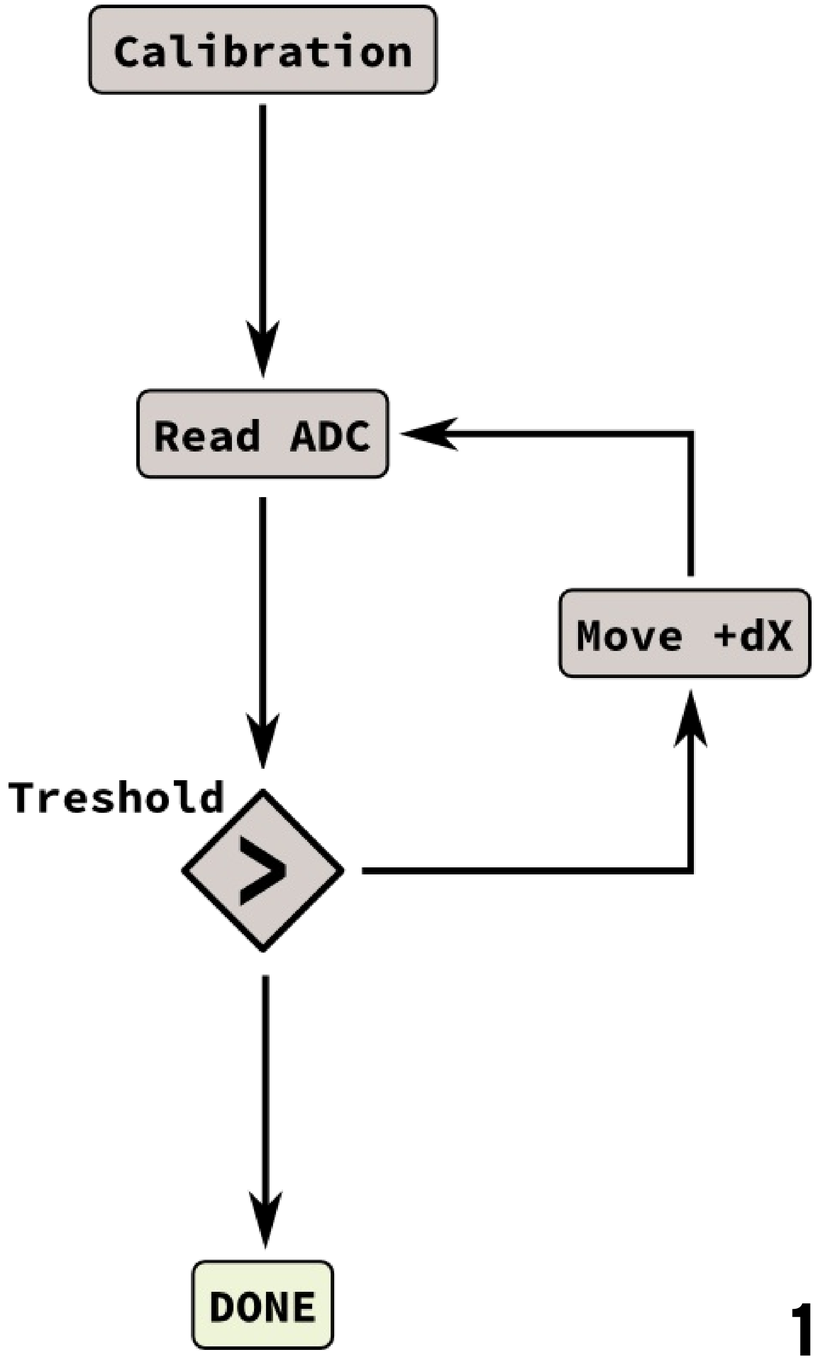
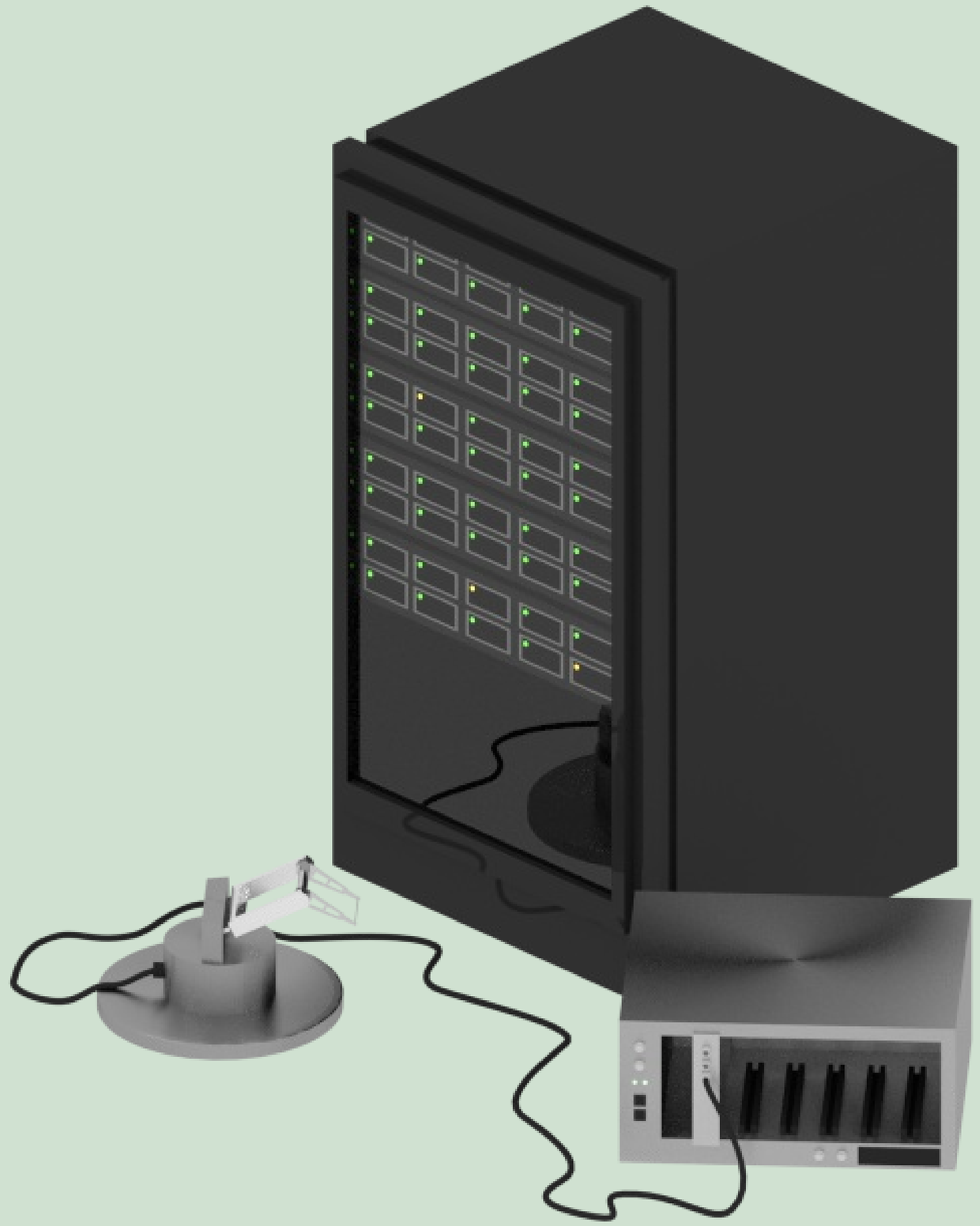
Adjustable gain



Functional specifications

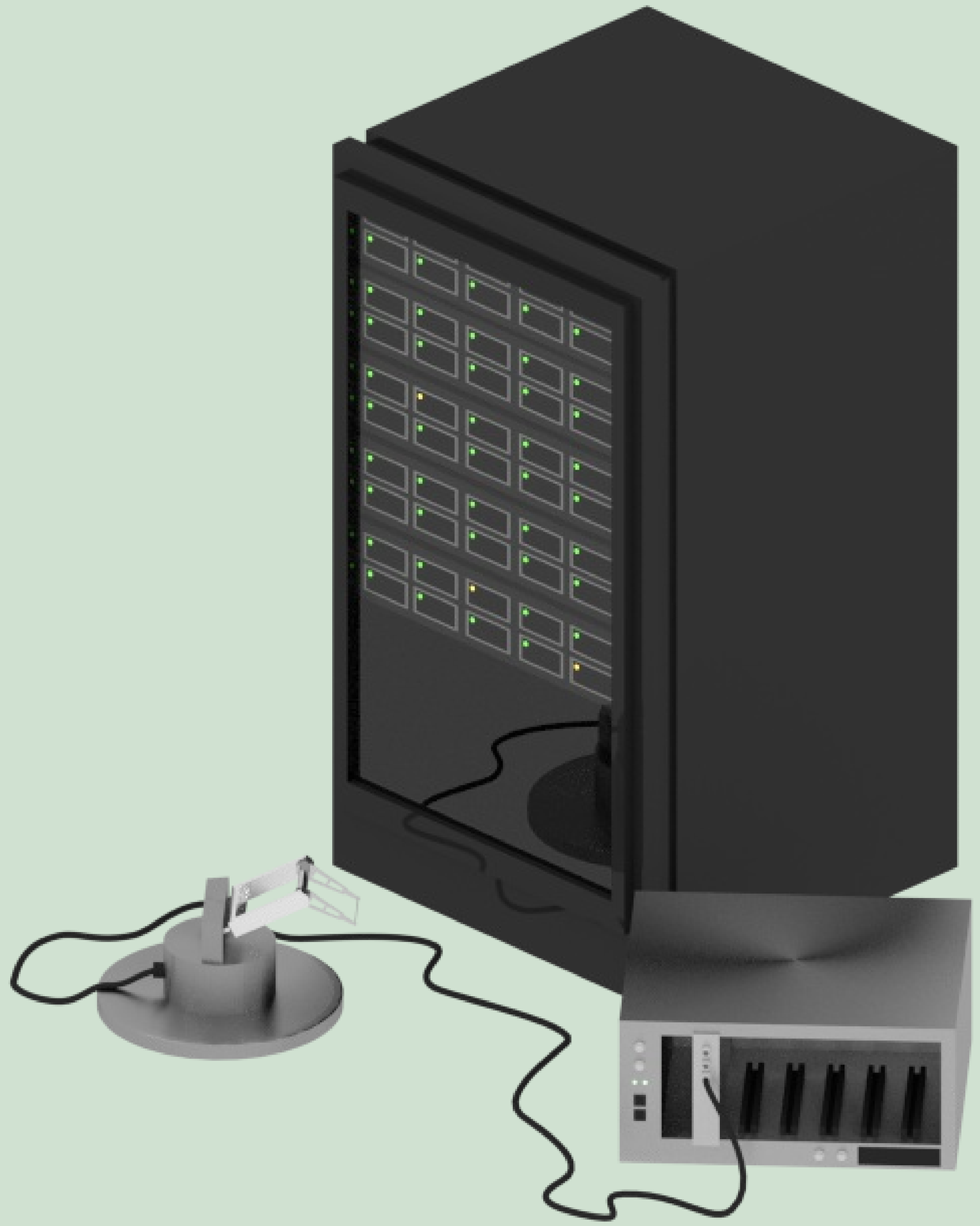


FESA CLASS DEVELOPMENT WORKFLOW



FESA CLASS DEVELOPMENT WORKFLOW

- Design
  - Expert level
  - Operational level
- Development
- Deployment and testing



BI CLIENTS AND TOOLS

BI SPECIFIC APPLICATIONS

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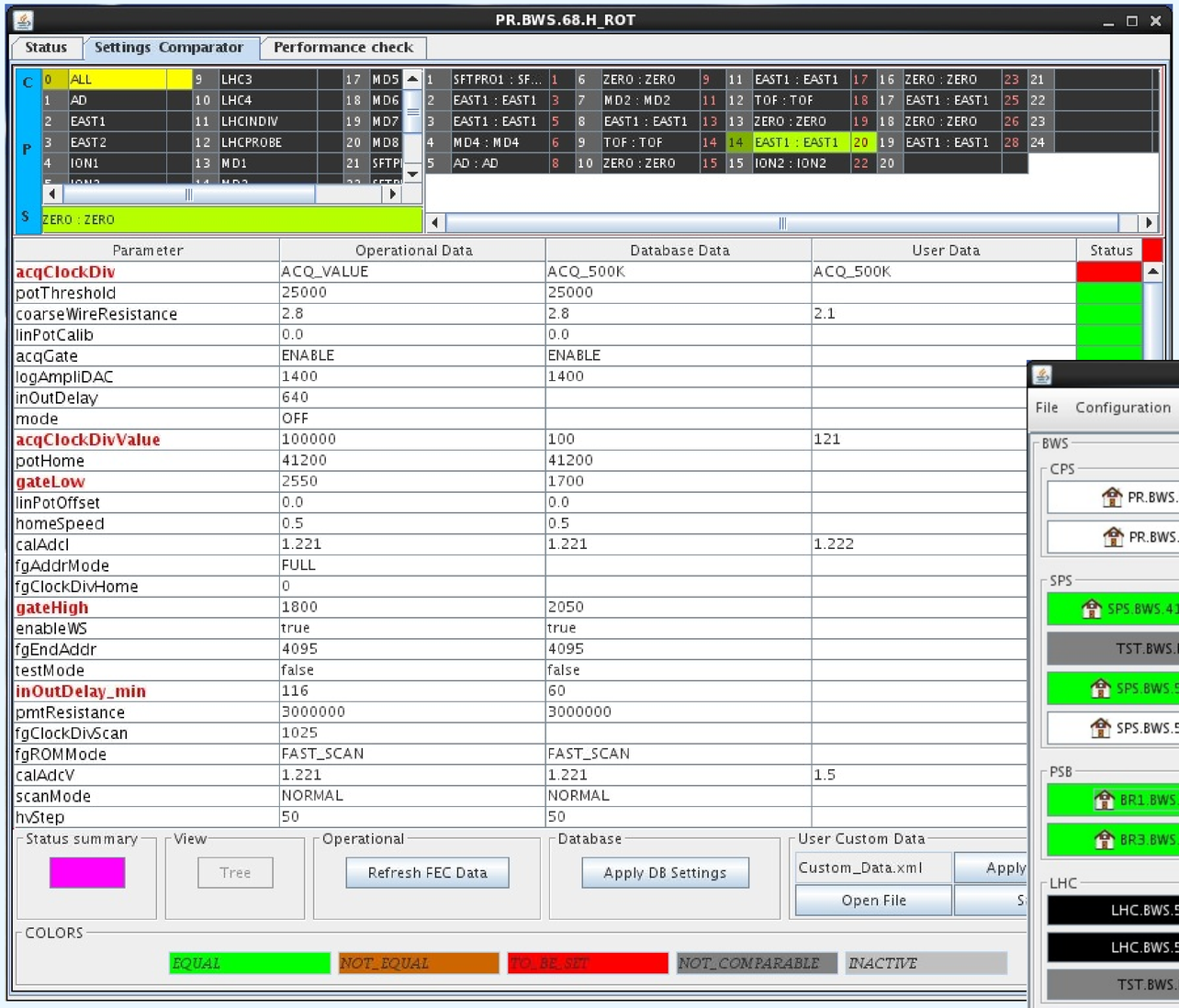
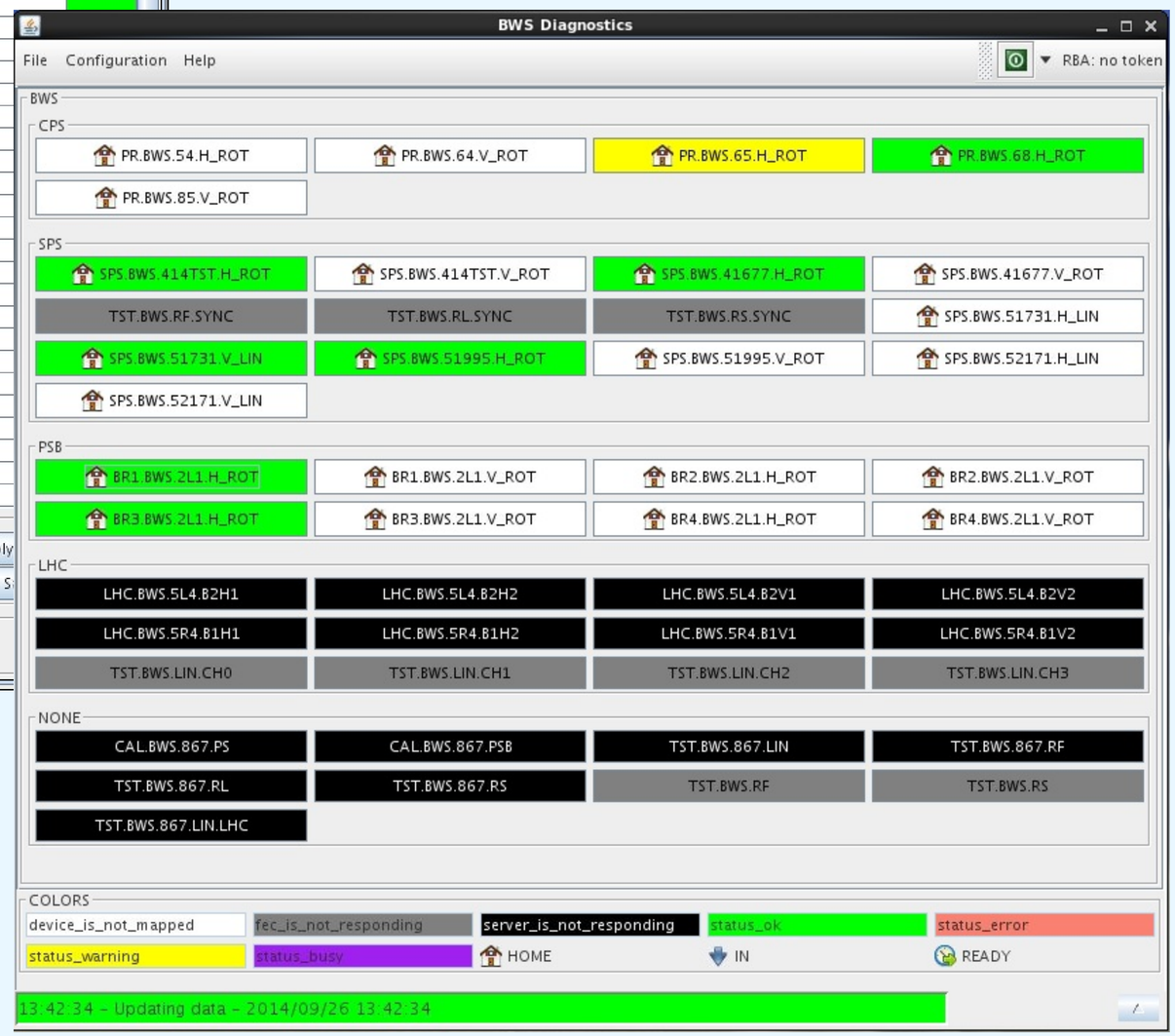
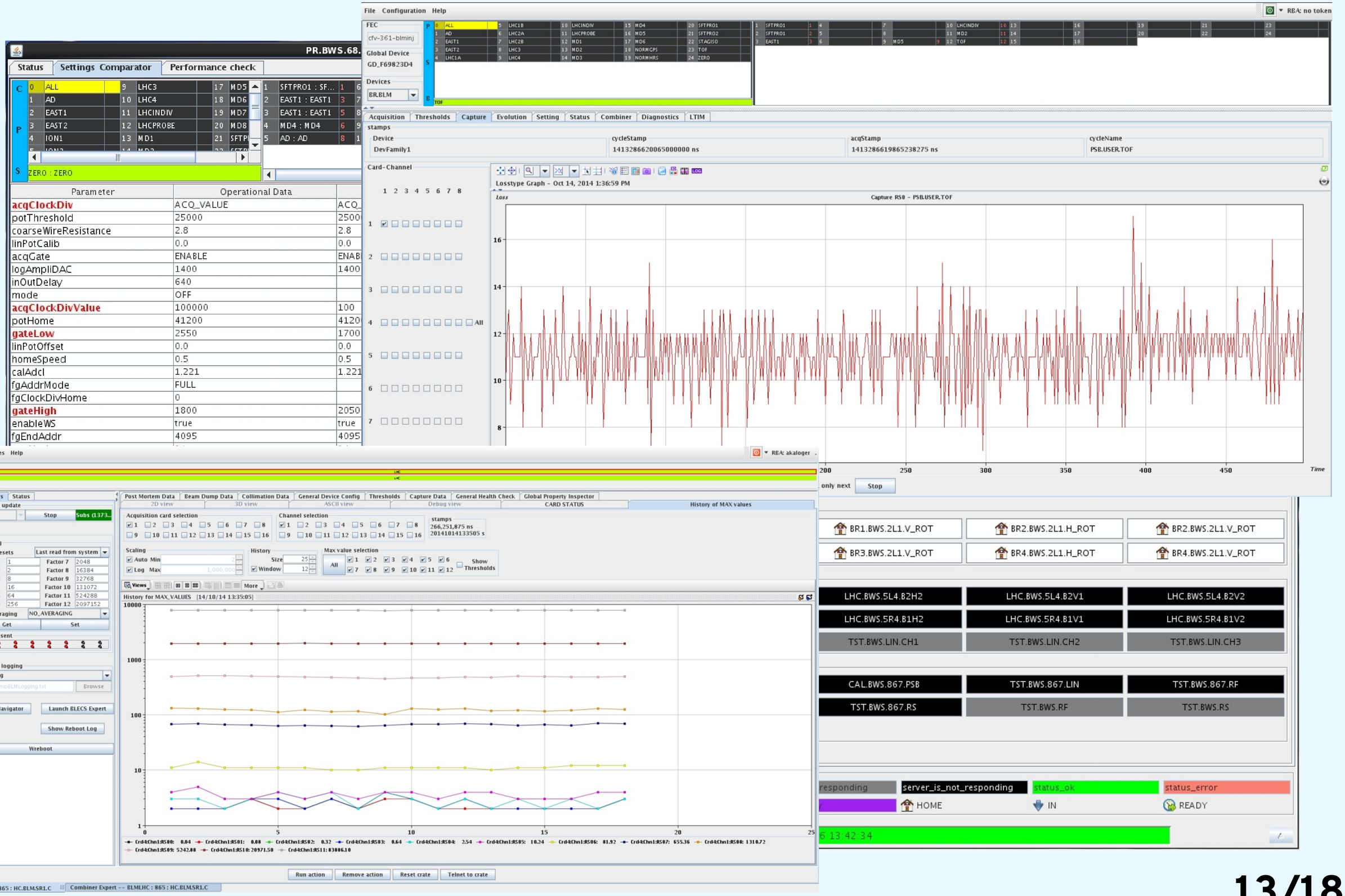




BI SPECIFIC APPLICATIONS



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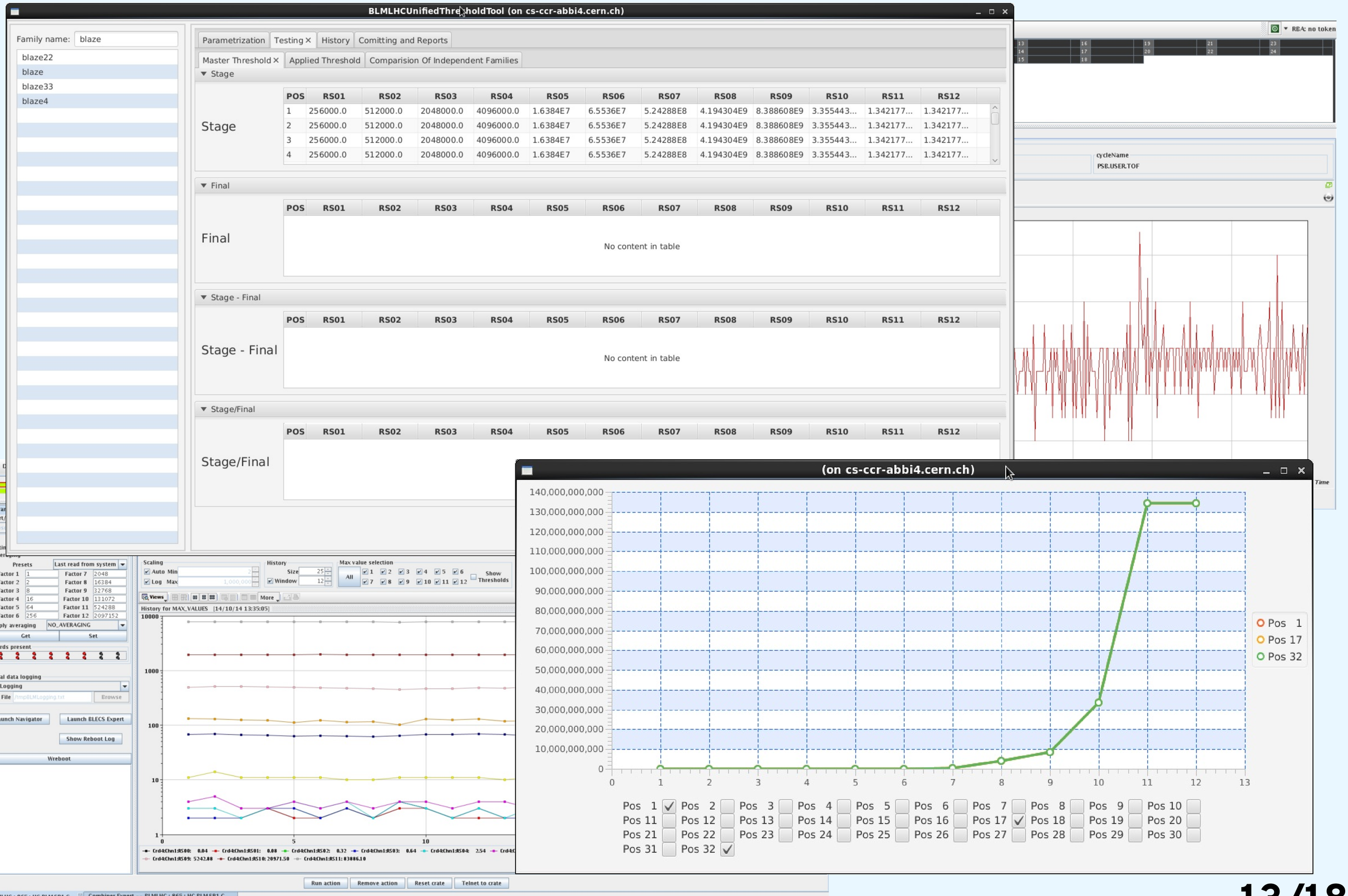

BI GENERIC APPLICATIONS

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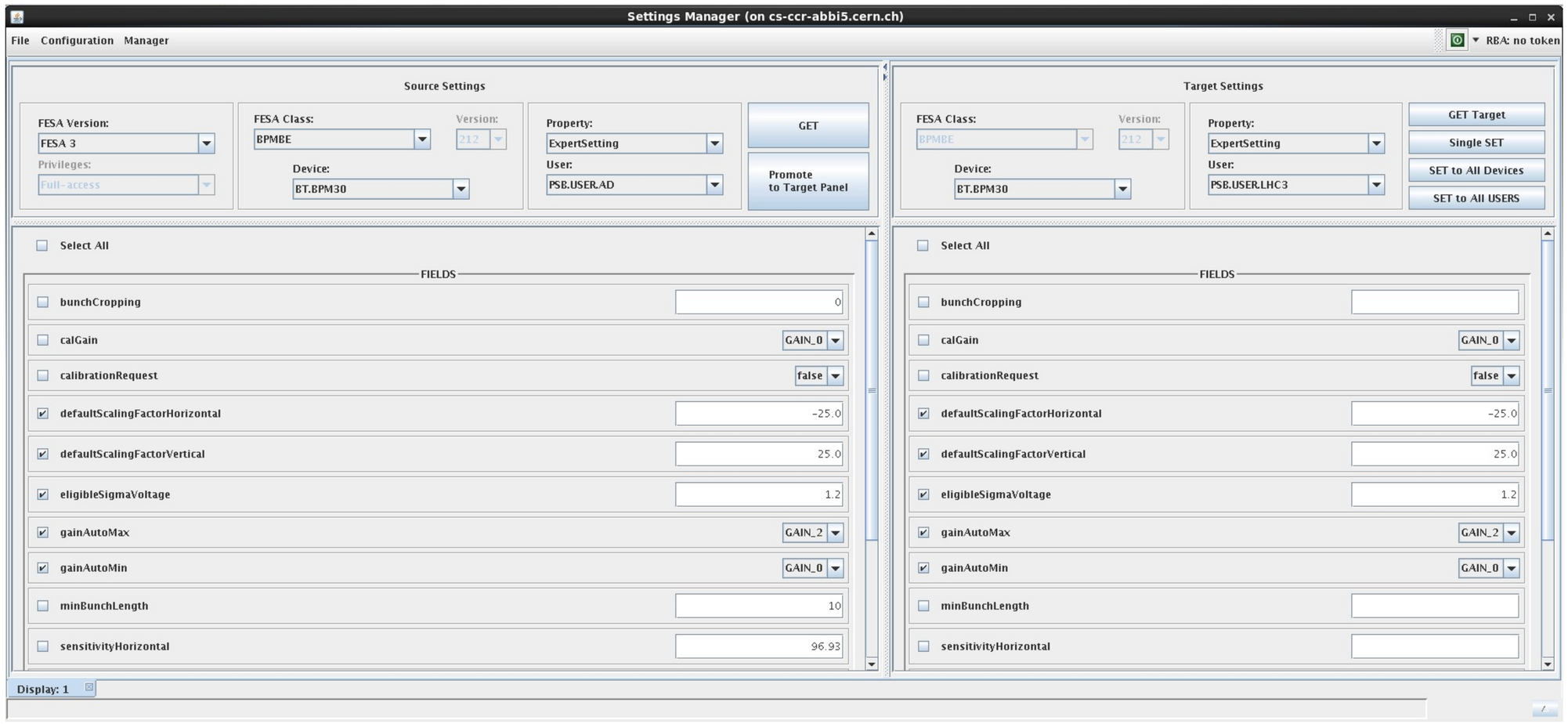

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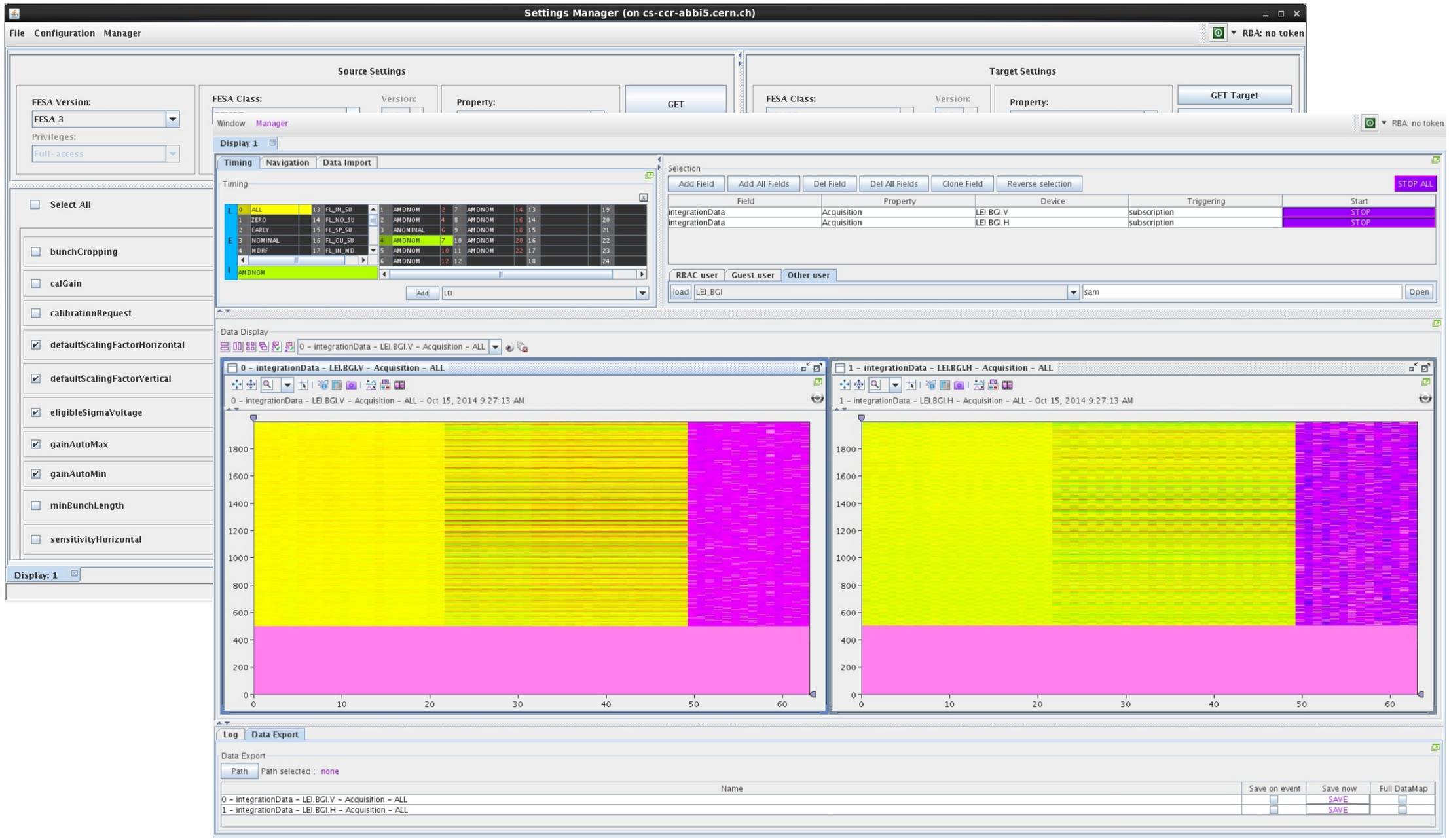


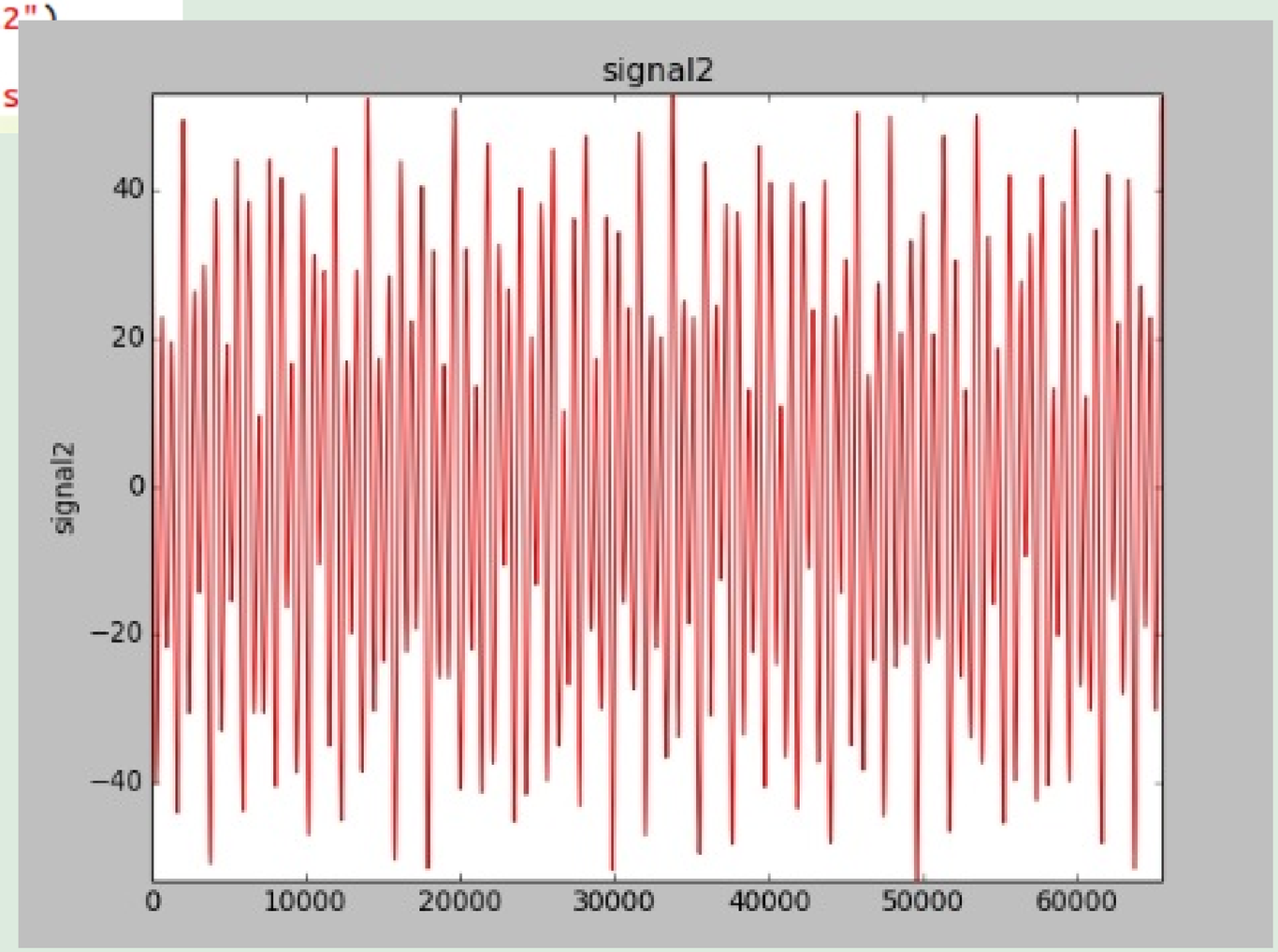
OTHER TOOLS

OTHER TOOLS

```
import pica

api = pica.Pica()
id_sub = api.subscribe(device_name="ADEMLTest1",
                       property_name="SignalAcquisition",
                       cycle_name="ADE.USER.ADE")
init_fig = pica.initiate_figure()
while True:
    delta_ms1 = api.getFreshData(0, id_sub)
    api.print_data(id_sub)
    signal2 = api.get_field_data(id_sub, "signal2")
    pica.update_figure(init_fig, signal2,
                       ylabel="signal2", title="s
```

MathStub



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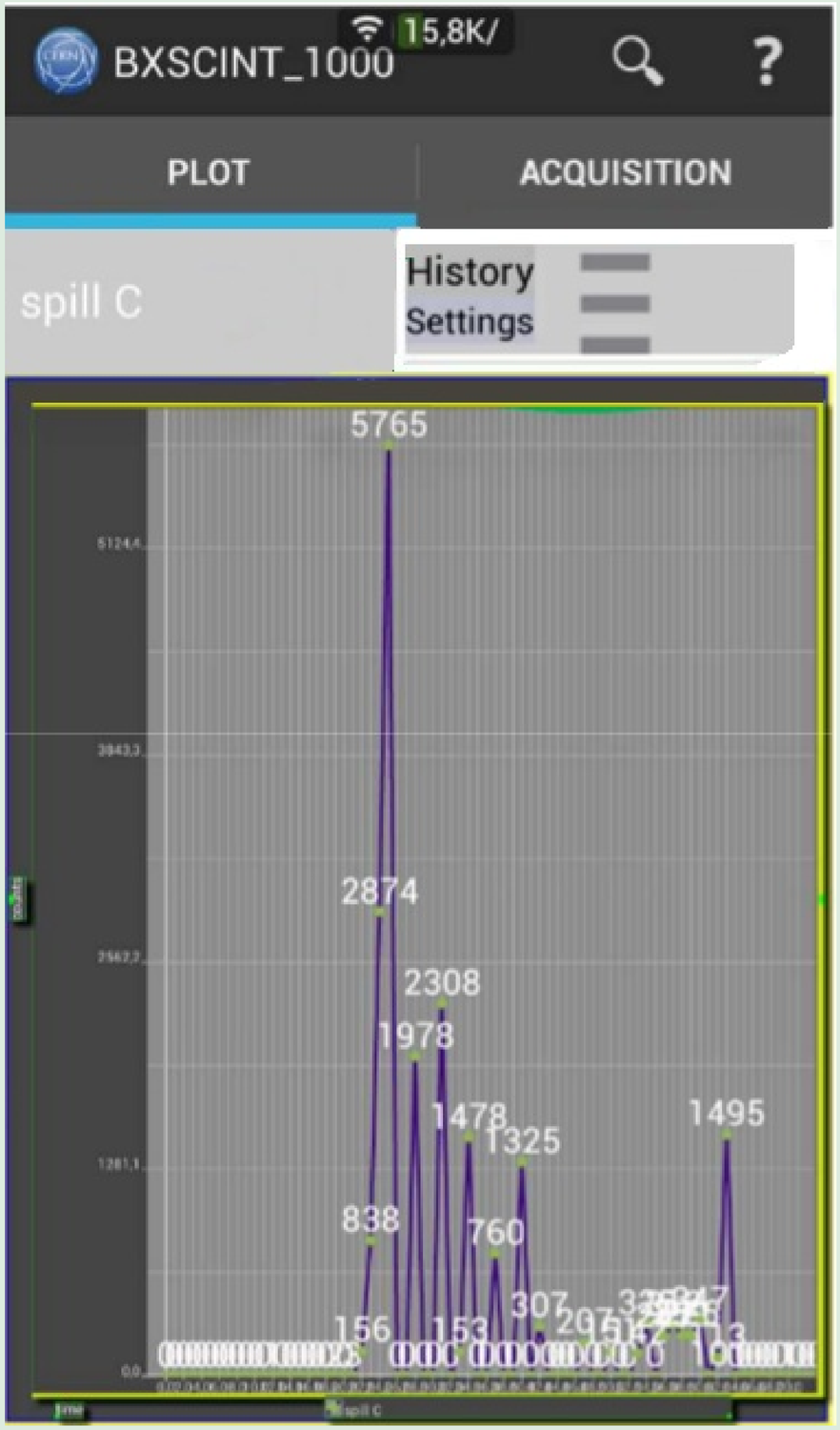


BXSCINTS.xml

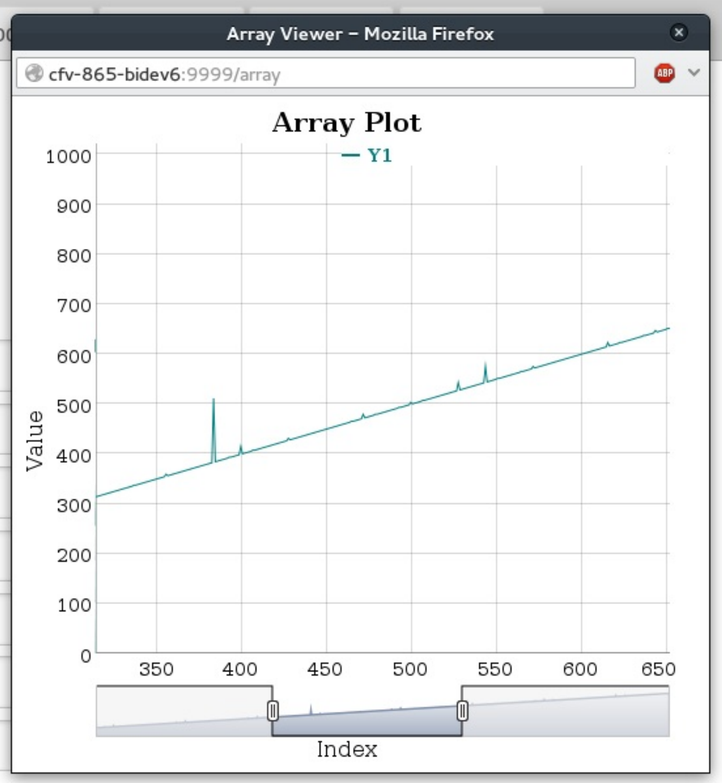
Data	File
BXSCINT_1000	hv: -2,00 || counts: 000866
BXSCINT_1001	hv: -1,74 || counts: 000591
BXSCINT_1002	hv: -1,80 || counts: 001938
BXSCINT_1003	hv: -1,80 || counts: 000000
BXSCINT_0100	hv: -1,76 || counts: 000000
BXSCINT_0101	hv: -1,96 || counts: 000000
BXSCINT_0102	hv: -1,75 || counts: 000000
BXSCINT_0103	hv: -1,82 || counts: 000001
BXSCINT_0104	hv: -1,92 || counts: 000000
BXSCINT_0200	hv: -1,99 || counts: 000031
BXSCINT_0201	hv: -1,75 || counts: 000000
BXSCINT_0202	hv: -0,11 || counts: 000000
BXSCINT_0203	hv: -1,81 || counts: 000001
BXSCINT_0204	hv: -0,11 || counts: 000000

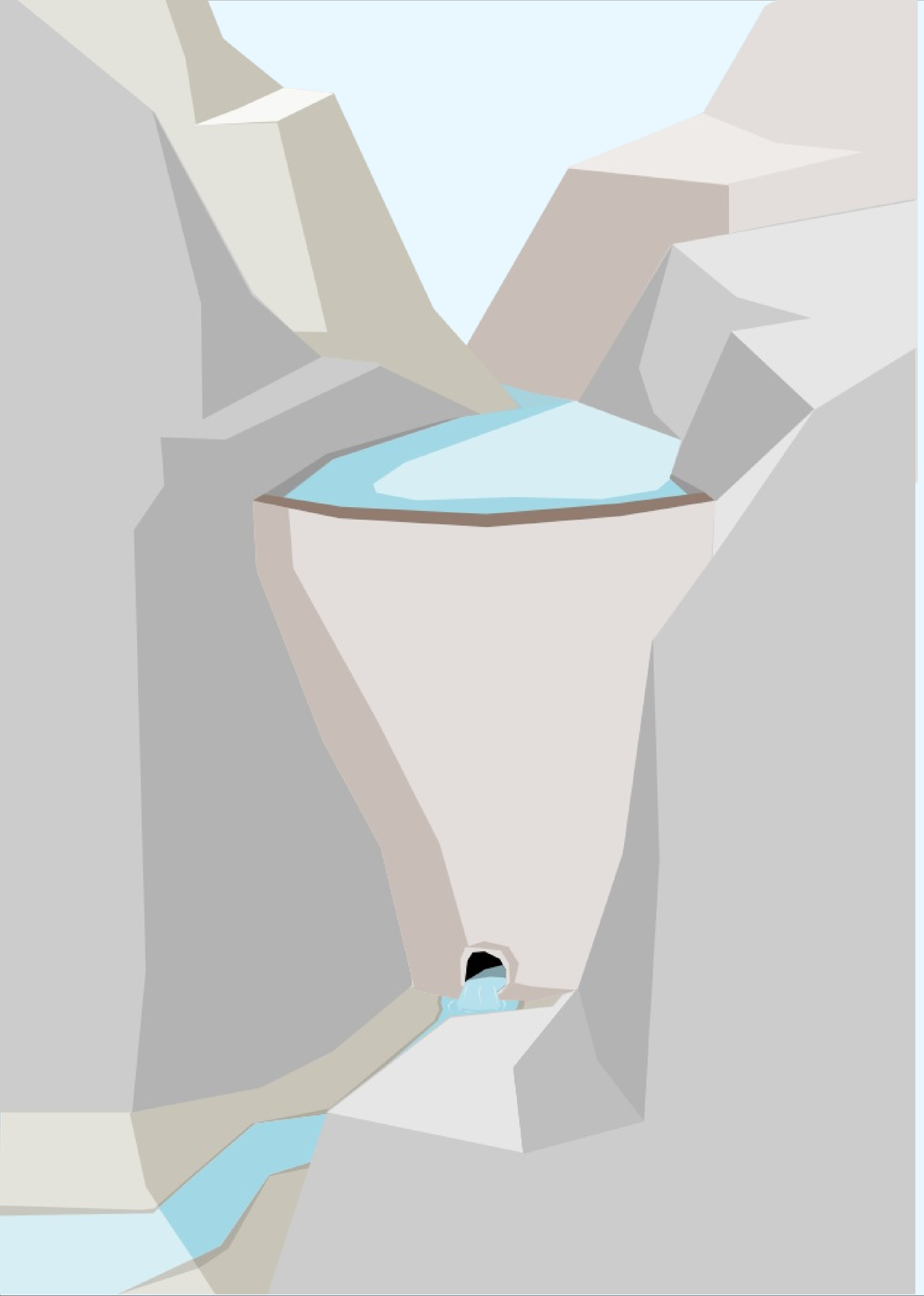
OTHER TOOLS

LUN 0 open get close **Driver** : bi_adcstep | **Host** : cfv-865-bidev6 hexadecimal

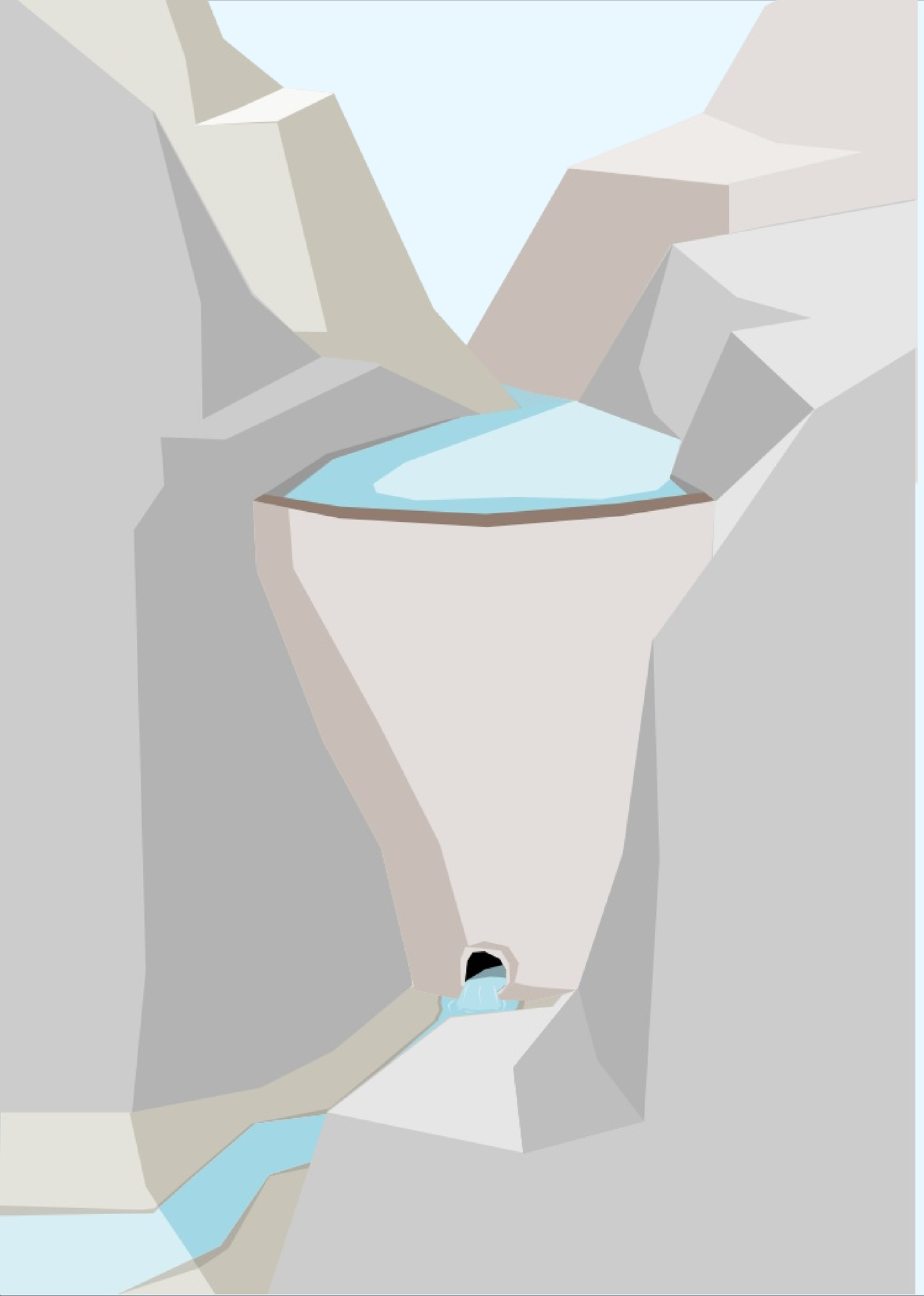
Module 0 | Module 1 | Module 2 | Module 3 | Module 4 | Mo

channelStatus1	0x128	get		
channelReset1	0	set		
stpPosCounter1	0x0	get		
stpResetCount1	0	set		
stpStepToMove1	0xa	get	0	
stpMovDirection1	0x0	get	0	
stpStartSpeed1	0x0	get	0	
stpCruiseSpeed1	0x0	get	0	
stpAcceleration1	0x0	get	0	
stpTriggerMode1	0x0	get	0	
stpTrail1	0x0	get	0	
stpStartMove1	0	set		
stpStopMove1	0	set		
stpEndSwichConf1	0x0	get	0	set
stpPowerConf1	0x0	get	0	set
adcNofSamples1	0x1	get	0	set
adcStartIndex1	0xc1	get	0	set
adcFreeRun1	0x0	get	0	set
adcTriggerMode1	0x0	get	0	set
adcStartAcq1	0	set		



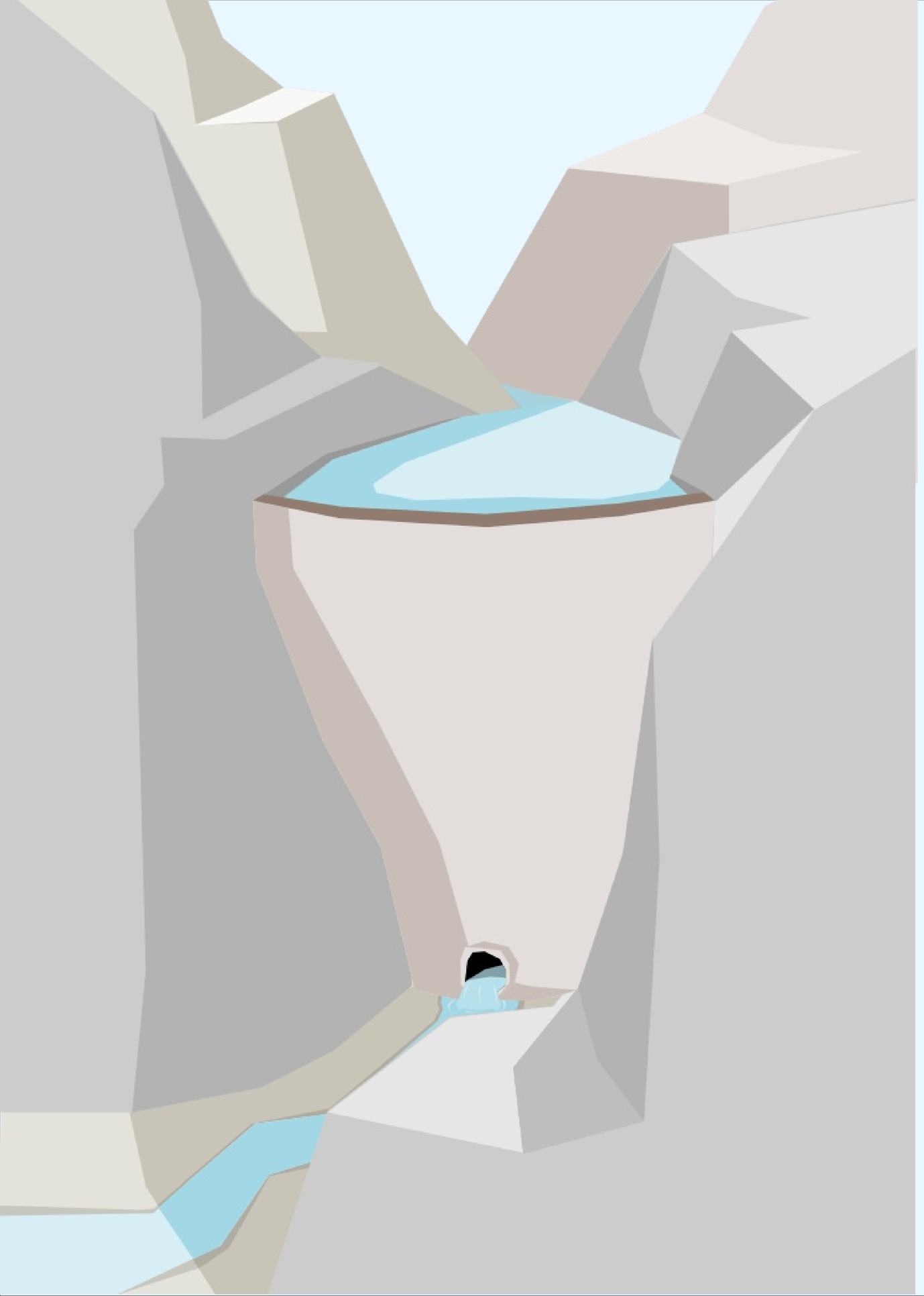


CONSTRAINTS



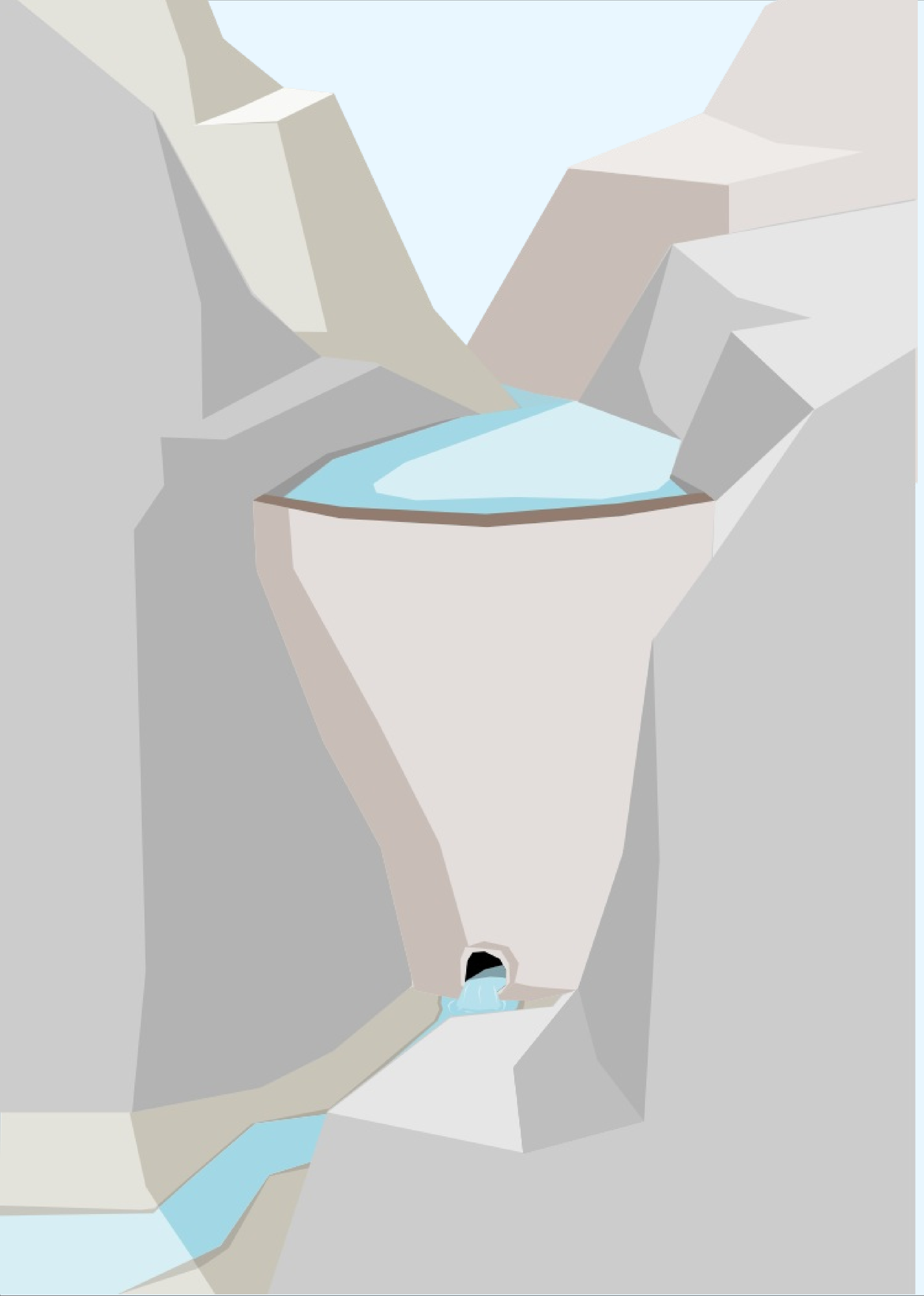
CONSTRAINTS

- Tools and languages



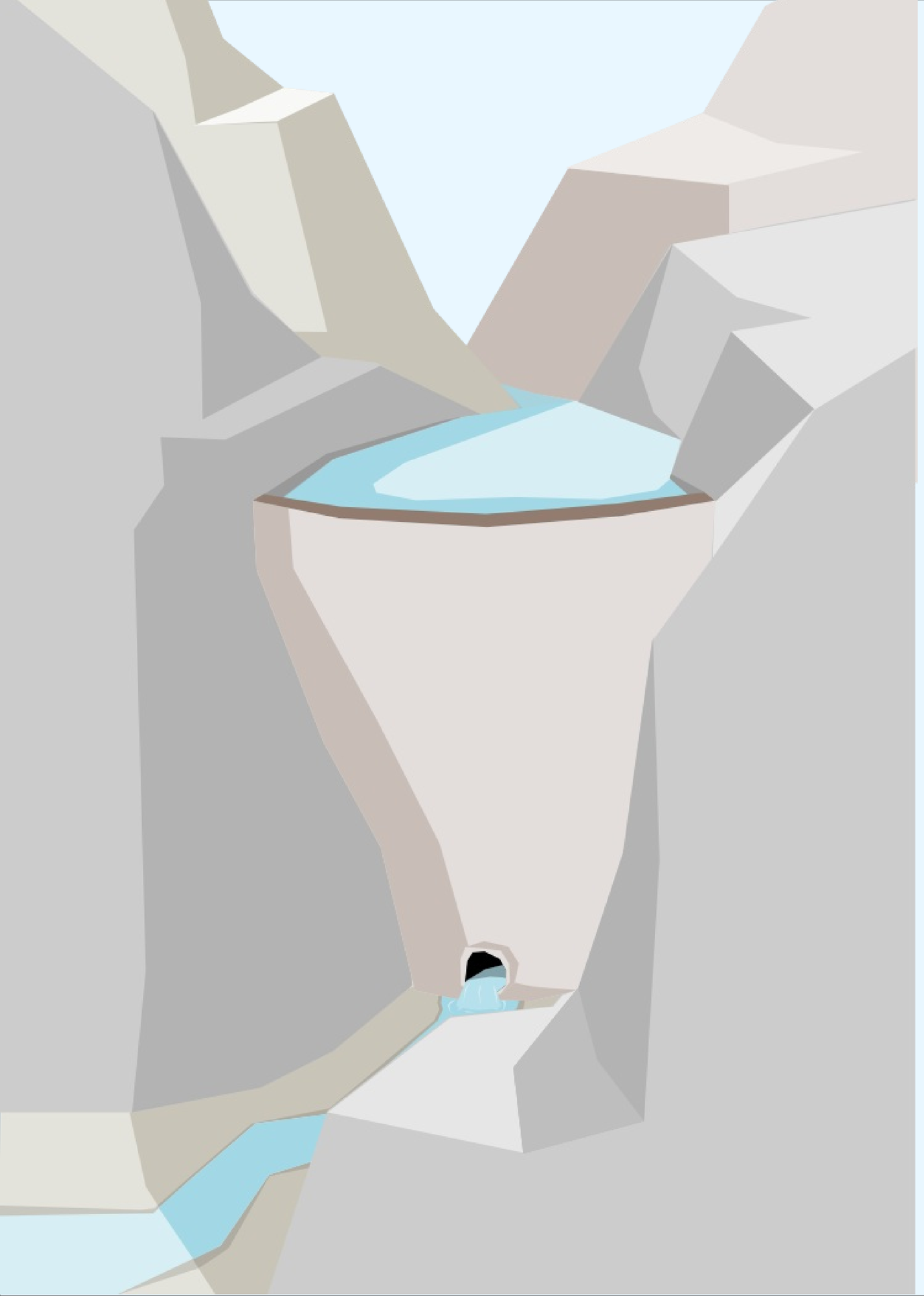
CONSTRAINTS

- Tools and languages
- Version and updates



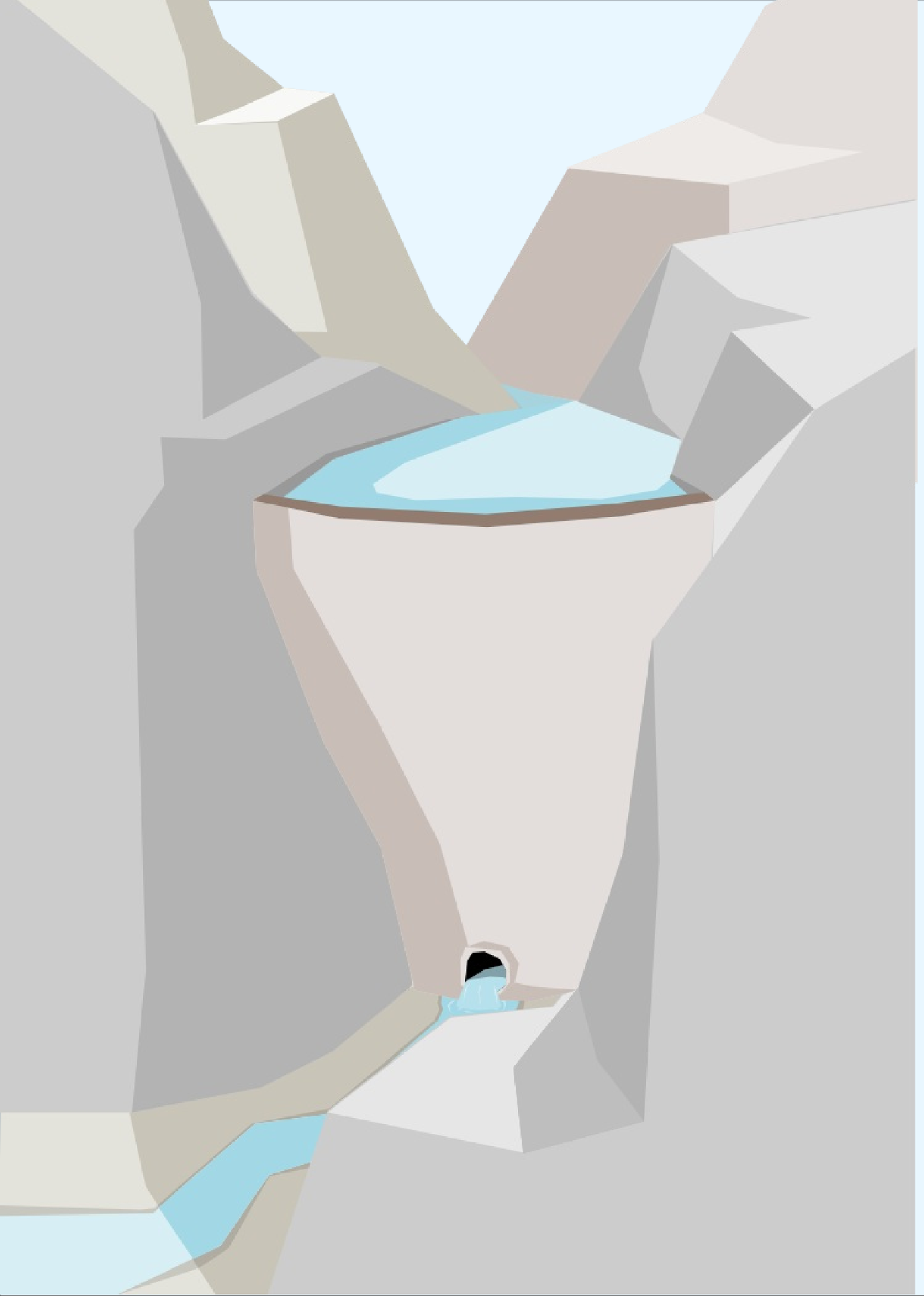
CONSTRAINTS

- Tools and languages
- Version and updates
- Hardware platforms



CONSTRAINTS

- Tools and languages
- Version and updates
- Hardware platform
- Dependence on the ACS



CONSTRAINTS

- Tools and languages
- Version and updates
- Hardware platform
- Dependence on the ACS

We can not do whatever we want (or you want)

SOME NUMBERS FOR BI FESA CLASSES

More than **100 FESA** classes

All FESA 2 classes under updating to **FESA 3**

~ 250 FECs under our responsibility

more than 100 Expert Applications and Tools

Challenges

Multitude of devices

Multiple infrastructures

Under developing specifications

Operational and Expert needs

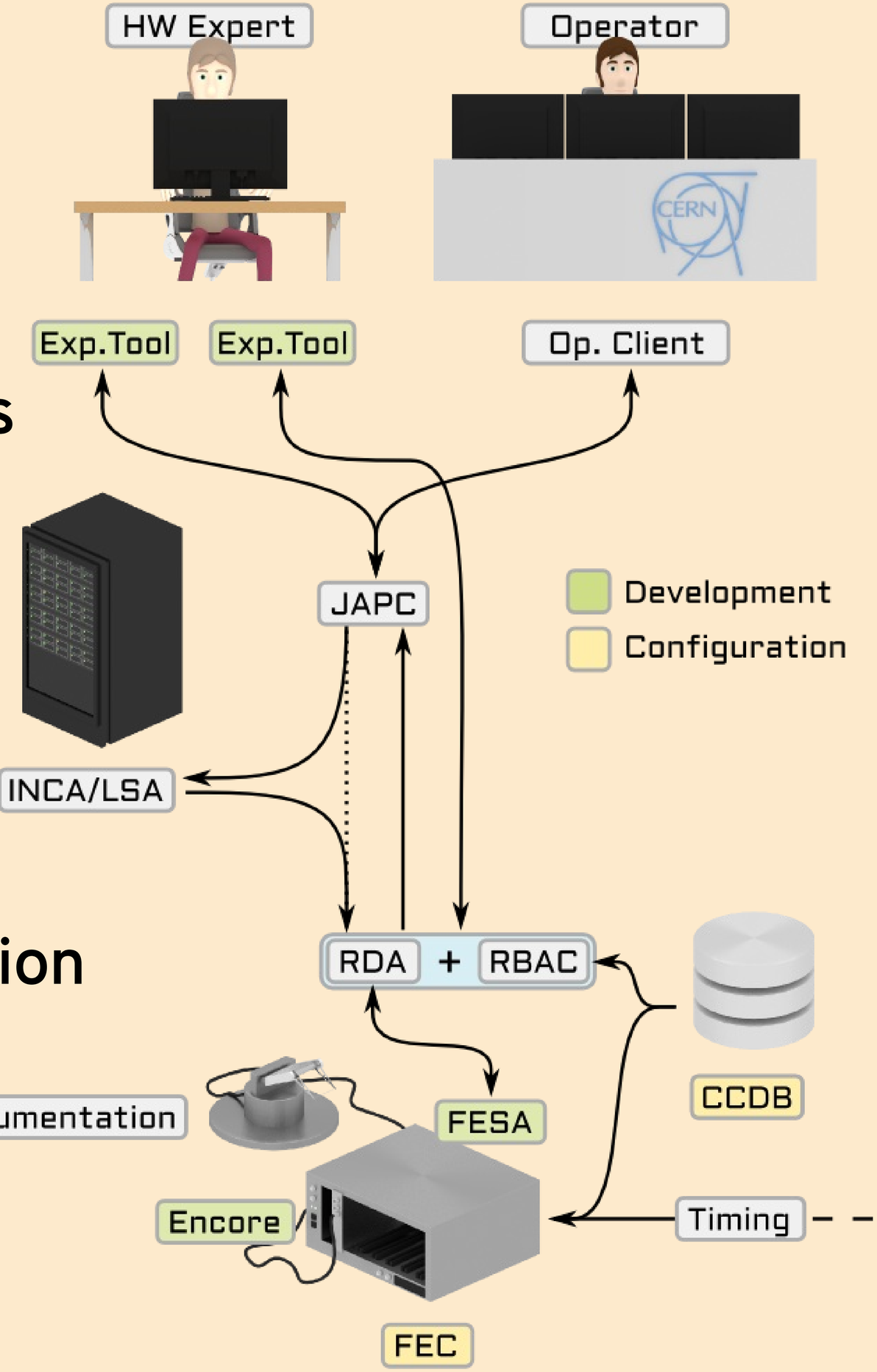
Constraints

Hardware maintenance

Software maintenance

Software and Hardware migration

Tools and dependencies



THANK YOU FOR YOUR ATTENTION

ANY QUESTIONS?