

## Detector Simulation On Modern Coprocessors

The recent prevalence of hardware architectures of many-core or accelerated processors opens opportunities for concurrent programming models taking advantages of both SIMD and SIMT architectures. The Geant Vector Prototype has been designed both to exploit the vector capability of main stream CPUs and to take advantage of Coprocessors including NVidia's GPU and Intel Xeon Phi. The characteristics of each of those architectures are very different in term of the vectorization depth, parallelization need to achieve optimal performance or memory access latency and speed. Between each platforms the number of individual tasks to be processed 'at once' for efficient use of the hardware varies sometimes by an order of magnitude. The granularity of the code executed may also need to be dynamically adjusted. An additional challenge is to avoid the code duplication often inherent to supporting heterogeneous platforms. We will present the challenges, solutions and resulting performance of running an end to end detector simulation concurrently on a main stream CPU and a coprocessor and detail the broker implementation bridging the disparity between the two architectures. The impacts of task decomposition, vectorization, efficient sampling techniques and data look-up using track level parallelism for the physics process will be also evaluated on vector and massively parallel architectures.

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