INTEROFFICE MEMORANDUM

TO: MEMBERS OF BI-TB
FROM: HERMANN SCHMICKLER, RHODRI JONES
SUBJECT: THE CUNNING PLAN OF VFC DEVELOPMENTS
DATE: AUGUST 27, 2014
CC: [NAME]

Dear all,

For the further development of the BI-VFC board we agreed on the following milestones over the next 15 months.

The overall aim is to have the basic module ready for large scale MOPOS production and a version with FMC digitiser ready for the LHC fast BCT and the LHC diamond BLMs before the WS2015/2016. To reach this goal the following decisions were taken:

Time scale : Until end of September 2014

1) Continue testing the series delivered by NORCOTT in June 2014 and implement all issues and changes as they appear.

2) Request NORCOTT to implement all bug fixes in the production documents of the current version to archive a fully bug free version.

    a. Keeping the power supply PCB as a piggy back card.

    b. Inserting an ECL repeater chip which will make the card compatible with the BST and the white rabbit timing systems.

    Further changes will be discussed and decided under the lead of Andrea

3) Request NORCOTT to produce the production documents for a new version which in addition to all bug fixes and modification for the current version (summarized in 2) also replaces the SRAM by DDR.

4) Place an order for 10 new DDR version modules from NORCOTT

5) Procure a 500 MHz (14 bit) at least 2 channel AC or DC coupled ADC daughterboard. Responsibility: BI-PI

Time scale : Until end of 2014

1) Obtain the final production documentation for the DDR version from NORCOTT and transfer this into the CERN design environment. The process has been checked and does not represent major obstacles.

2) Implement and test the data acquisition through the 500 MHz ADC FMC onto the VFC. Responsibility: BI-PI; manpower to be defined between Rhodri and Lars.

    a. In case of long delivery times for the 500 MHz ADC FMC the decision may be taken to start development using the already available 320 MHz ADC FMC mezzanine. In this case the validation of the 500MHz ADC FMC is delayed until early 2014.

Time scale : Until Autumn 2015

3) Using the 500 MHz ADC FMC add the application specific FPGA software required for the diamond BLM (responsibility of BL section) and fast BCT (responsibility of PI section) projects.